Commercial and Industrial DDR4 4Gb SDRAM

Features

- **Data Integrity**
  - Auto Self Refresh (ASR) by DRAM built-in TS
  - Auto Refresh and Self Refresh Modes
- **DRAM Access Bandwidth**
  - Separated IO gating structures by Bank Groups
  - Self Refresh Abort
  - Fine Granularity Refresh
- **Signal Synchronization**
  - Write Leveling via MR settings[1]
  - Read Leveling via MPR
- **Reliability & Error Handling**
  - Command/Address Parity
  - Databus Write CRC
  - MPR readout
  - Boundary Scan (X16)
  - Post Package Repair
- **Signal Integrity**
  - Internal VREFDQ Training
  - Read Preamble Training
  - Gear Down Mode
  - Per DRAM Addressability
  - Configurable DS for system compatibility
  - Configurable On-Die Termination
  - Data bus inversion (DBI)
  - ZQ Calibration for DS/ODT impedance accuracy via external ZQ pad (240 Ω ± 1%)
- **Power Saving & Efficiency**
  - POD with VDDQ termination
  - Command/Address Latency (CAL)
  - Maximum Power Saving
  - Low-power Auto Self Refresh (LPASR)

Programmable Functions

- **Output Driver Impedance (34/48)**
- **CAS Write Latency (9/10/11/12/14/16/18)**
- **Additive Latency (0/CL-1/CL-2)**
- **$\overline{CS}$ to Command Address Latency (3/4/5/6/8)**
- **Command Address Parity Latency (4/5)**
- **Write Recovery Time (10/12/14/16/18/20/24)**
- **Burst Type (Sequential/Interleaved)**
- **RTT_PARK (34/40/48/60/80/120/240)**
- **RTT_NOM (34/40/48/60/80/120/240)**
- **RTT_WR (80/120/240)**
- **Read Preamble (1T/2T)**
- **Write Preamble (1T/2T)**
- **Burst Length (BL8/BC4/BC4 or 8 on the fly)**
- **LPASR (Manual: Normal/Reduced/Extended, Auto:TS)**

Options

- **Speed Grade (CL-TRCD-TRP) [2]**
  - 2666 Mbps / 19-19-19
- **Temperature Range (T_c) [5]**
  - Commercial Grade : 0℃~95℃
  - Industrial Grade (-I) : -40℃~95℃
  - Quasi Industrial Grade (-T) : -40℃~95℃
  - k
- **VDD/VDDQ/VPP**
  - 1.2V / 1.2V / 2.5V

- **Package information**

Lead-free RoHS compliance and Halogen-free

TFBGA Package	Dimension (mm)	Ball pitch (mm)
78-Ball	7.50 x 10.50	0.80
96-Ball	7.50 x 13.00	0.80

- **Density and Addressing**

Organization	1024Mbx4	512Mb x 8	256Mb x 16
Banks	4 (BA[1:0])	4 (BA[1:0])	4 (BA[1:0])
Bank Groups	4 (BG[1:0])	4 (BG[1:0])	2 (BG[0])
Row Address	A[15:0]	A[14:0]	A[14:0]
Column	1K (A[9:0])	1K (A[9:0])	1K (A[9:0])
Page Size	512B	1KB	2KB
tREFI [3]	Tc≦85℃:7.8μs, Tc>85℃:3.9μs		
tRFC [4]	260ns		

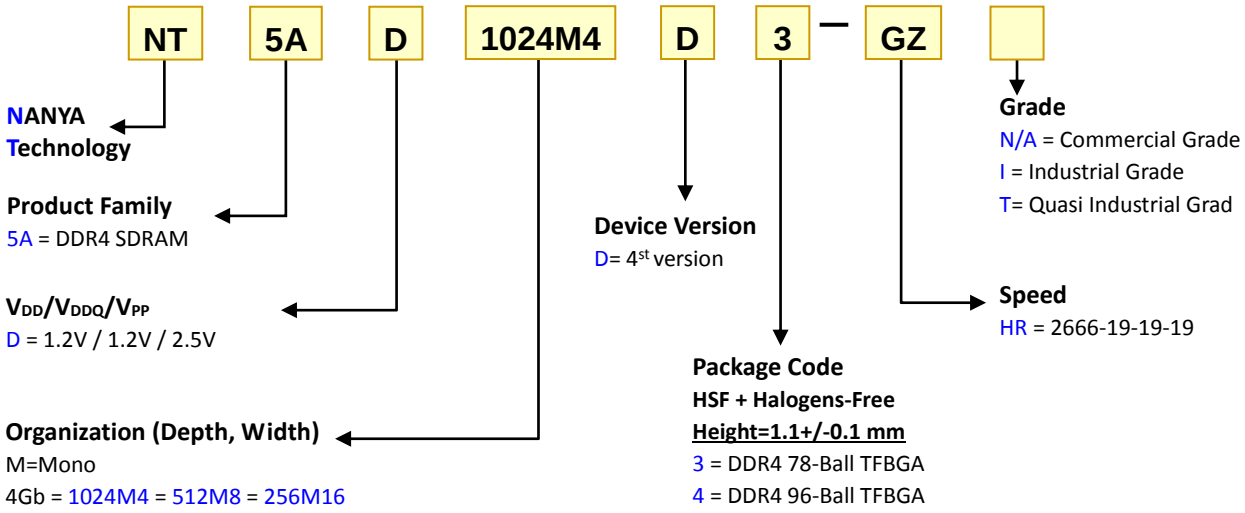
NOTE 1 Write Leveling feedback should be given on all data bits in parallel.
NOTE 2 For the same organization and voltage, the timing specification of high speed bin is backward compatible with low speed bin.
NOTE 3 Violating tREFI is not guaranteed.
NOTE 4 Violating tRFC is not guaranteed.
NOTE 5 When operate above 95℃,AC/DC will be derated.

Ordering Information

Organization	Part Number	Package	VDD/VDDQ/VPP	Speed		
				Clock (MHz)	Data Rate (Mb/s)	CL-tRCD-tRP
DDR4 Commercial Grade						
1024M x 4	**NT5AD1024M4D3-HR**	78-Ball	1.2V/1.2V/2.5V	1333	DDR4-2666	19-19-19
512M x 8	**NT5AD512M8D3-HR**	78-Ball	1.2V/1.2V/2.5V	1333	DDR4-2666	19-19-19
256M x 16	**NT5AD256M16D4-HR**	96-Ball	1.2V/1.2V/2.5V	1333	DDR4-2666	19-19-19
DDR4 Industrial Grade[1]						
512M x 8	**NT5AD512M8D3-HRI**	78-Ball	1.2V/1.2V/2.5V	1333	DDR4-2666	19-19-19
256M x 16	**NT5AD256M16D4-HRI**	96-Ball	1.2V/1.2V/2.5V	1333	DDR4-2666	19-19-19
DDR4 Quasi Industrial Grade[1]						
512M x 8	**NT5AD512M8D3-HRT**	78-Ball	1.2V/1.2V/2.5V	1333	DDR4-2666	19-19-19
256M x 16	**NT5AD256M16D4-HRT**	96-Ball	1.2V/1.2V/2.5V	1333	DDR4-2666	19-19-19

Note 1 Please confirm with NTC for the available schedule.

NANYA Consumer Component Part Numbering Guide



Operating frequency

The backward compatibility of each frequency is listed in the following table. If an application operates at specific frequency which is not defined herein but within the highest and the lowest frequencies, then the comparative loose specifications to DRAM must be adopted from the neighboring defined frequency. Please confirm with NTC when the operating frequency is slower than the defined frequency.

Frequency[MHz]	1333	1200	1066	933	800		Unit
CL[nCK]	19	17	15	13	12	11	
CL with read DBI [nCK]	22	20	18	15	NA	13	
VDD[V]	1.2	1.2	1.2	1.2	1.2		
NT5AD1024M4D3-HR	2666	2400	2133	1866	1600		Mbps
NT5AD512M8D3-HR(I/T)							
NT5AD256M16D4-HR(I/T)							

Notes: Any part number also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but has been verified

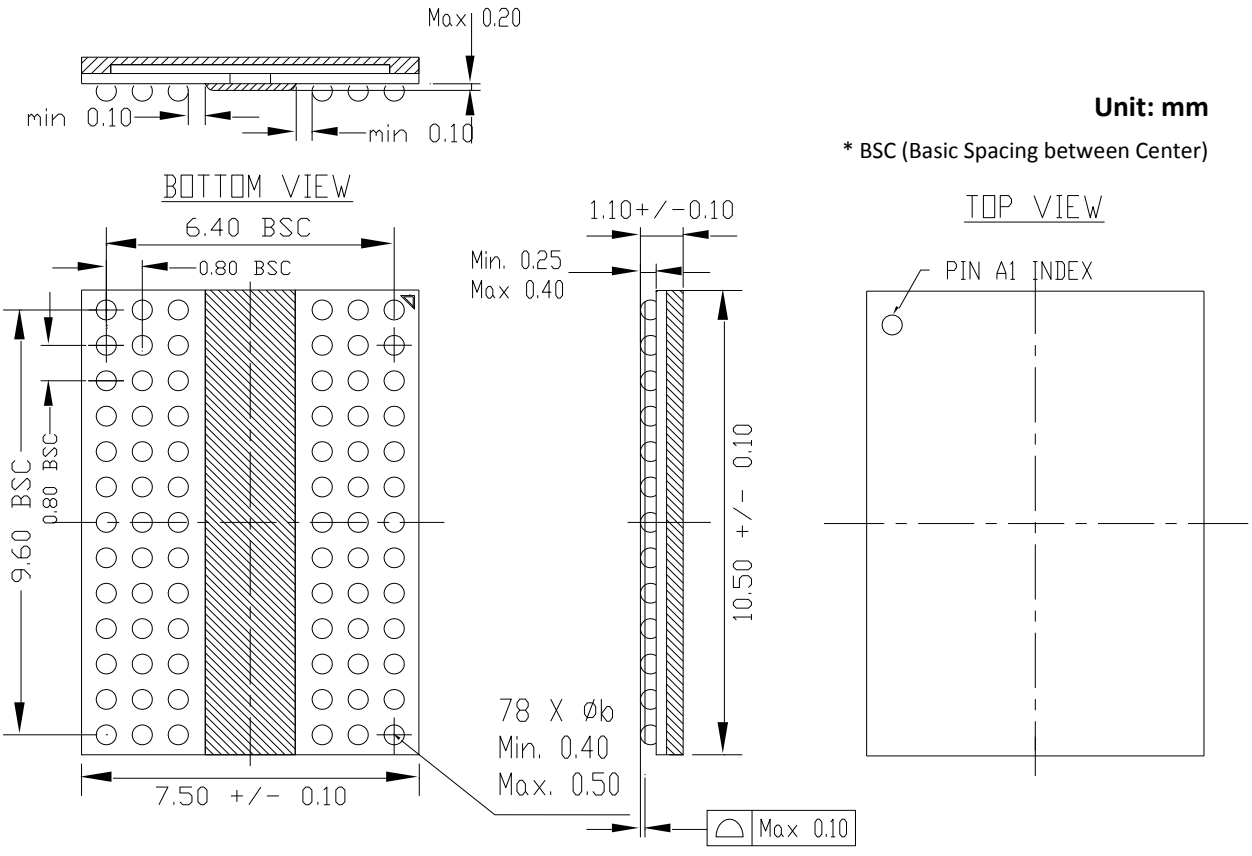
Ball Configuration – 78 Ball TFBGA Package (X4)

<TOP View>

See the balls through the package

	1	2	3	4 5 6	7	8	9	
A	VDD	VSSQ	$\overline{TDQS}$		DM/$\overline{DBI}$/TDQS	VSSQ	VSS	A
B	VPP	VDDQ	$\overline{DQS}$		DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS		VDD	VSS	VDDQ	C
D	VSSQ	NC	DQ2		DQ3	NC	VSSQ	D
E	VSS	VDDQ	NC		NC	VDDQ	VSS	E
F	VDD	NC	ODT		CK	CK	VDD	F
G	VSS	NC	CKE		$\overline{CS}$	NC	TEN	G
H	VDD	$\overline{WE}$/A14	$\overline{ACT}$		$\overline{CAS}$/A15	$\overline{RAS}$/A16	VSS	H
J	VREFCA	BG0	A10/AP		A12/$\overline{BC}$	BG1	VDD	J
K	VSS	BA0	A4		A3	BA1	VSS	K
L	$\overline{RESET}$	A6	A0		A1	A5	$\overline{ALERT}$	L
M	VDD	A8	A2		A9	A7	VPP	M
N	VSS	A11	PAR		NC	A13	VDD	N
	1	2	3	4 5 6	7	8	9	

Package Outline Drawing



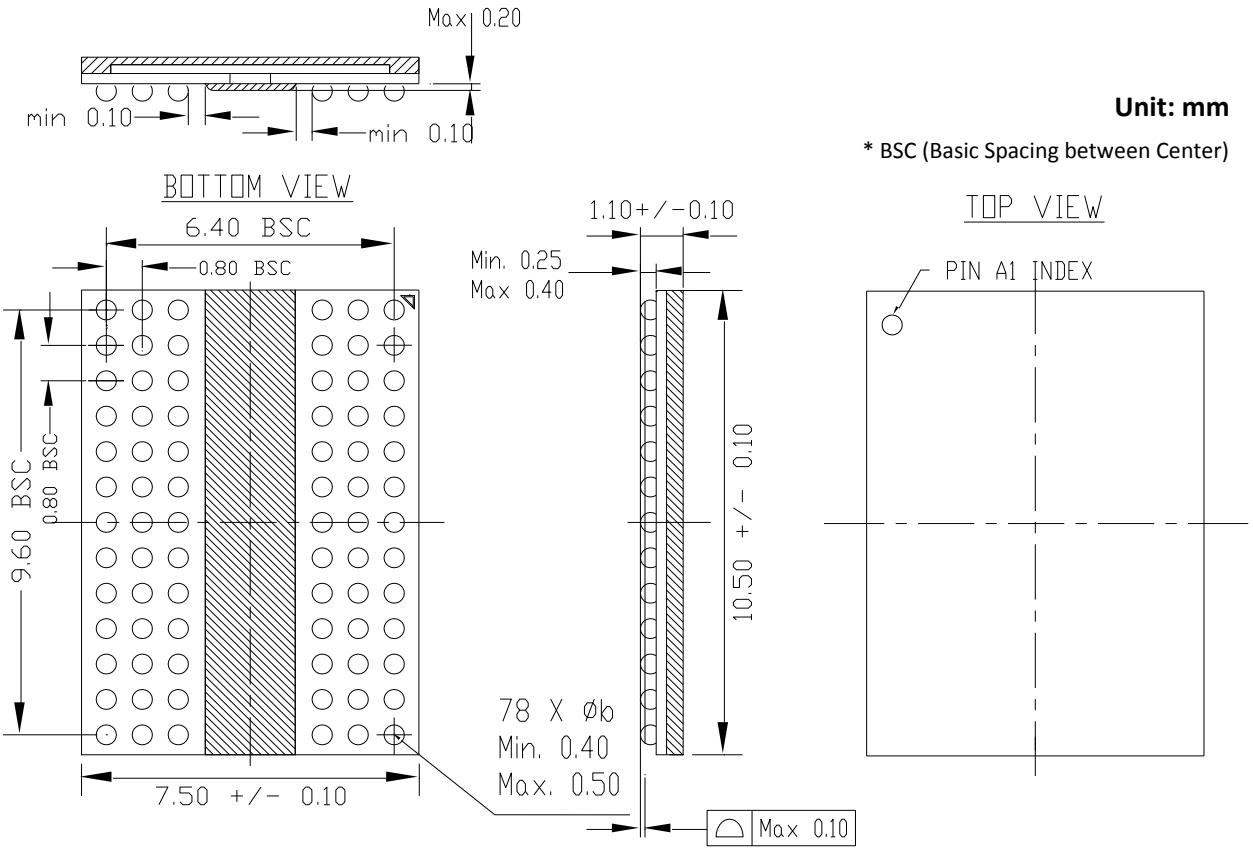
Ball Configuration – 78 Ball TFBGA Package (X8)

<TOP View>

See the balls through the package

	1	2	3	4 5 6	7	8	9	
A	VDD	VSSQ	$\overline{TDQS}$		$\overline{DM}/\overline{DBI}/TDQS$	VSSQ	VSS	A
B	VPP	VDDQ	$\overline{DQS}$		DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS		VDD	VSS	VDDQ	C
D	VSSQ	DQ4	DQ2		DQ3	DQ5	VSSQ	D
E	VSS	VDDQ	DQ6		DQ7	VDDQ	VSS	E
F	VDD	NC	ODT		CK	CK	VDD	F
G	VSS	NC	CKE		$\overline{CS}$	NC	TEN	G
H	VDD	$\overline{WE}$/A14	$\overline{ACT}$		$\overline{CAS}$/A15	$\overline{RAS}$/A16	VSS	H
J	VREFCA	BG0	A10/AP		A12/$\overline{BC}$	BG1	VDD	J
K	VSS	BA0	A4		A3	BA1	VSS	K
L	$\overline{RESET}$	A6	A0		A1	A5	$\overline{ALERT}$	L
M	VDD	A8	A2		A9	A7	VPP	M
N	VSS	A11	PAR		NC	A13	VDD	N
	1	2	3	4 5 6	7	8	9	

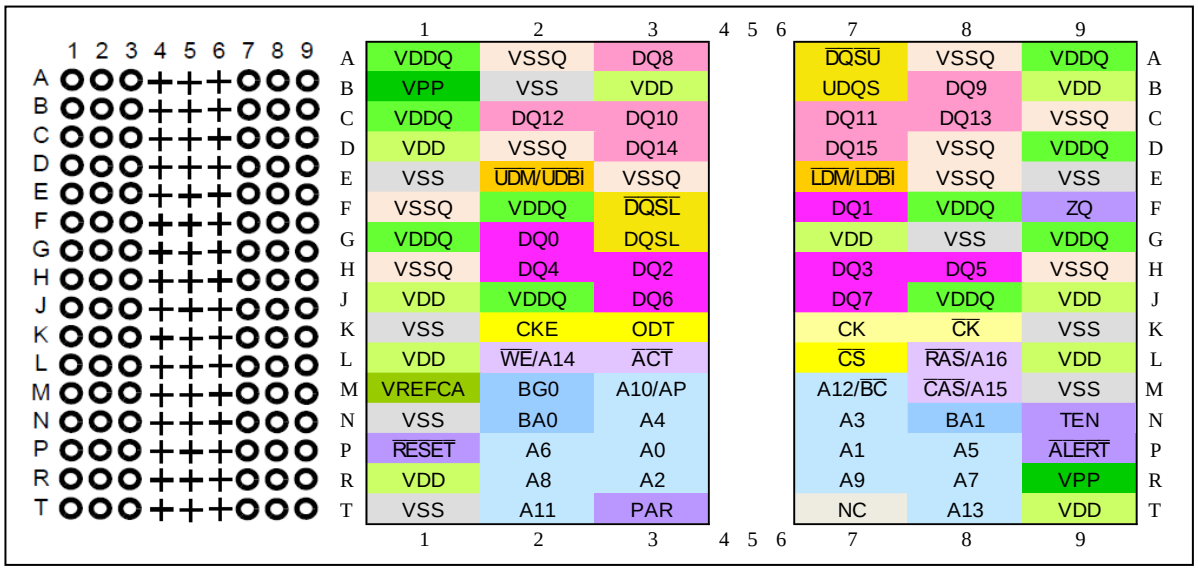
Package Outline Drawing



Ball Configuration – 96 Ball TFBGA Package (X16)

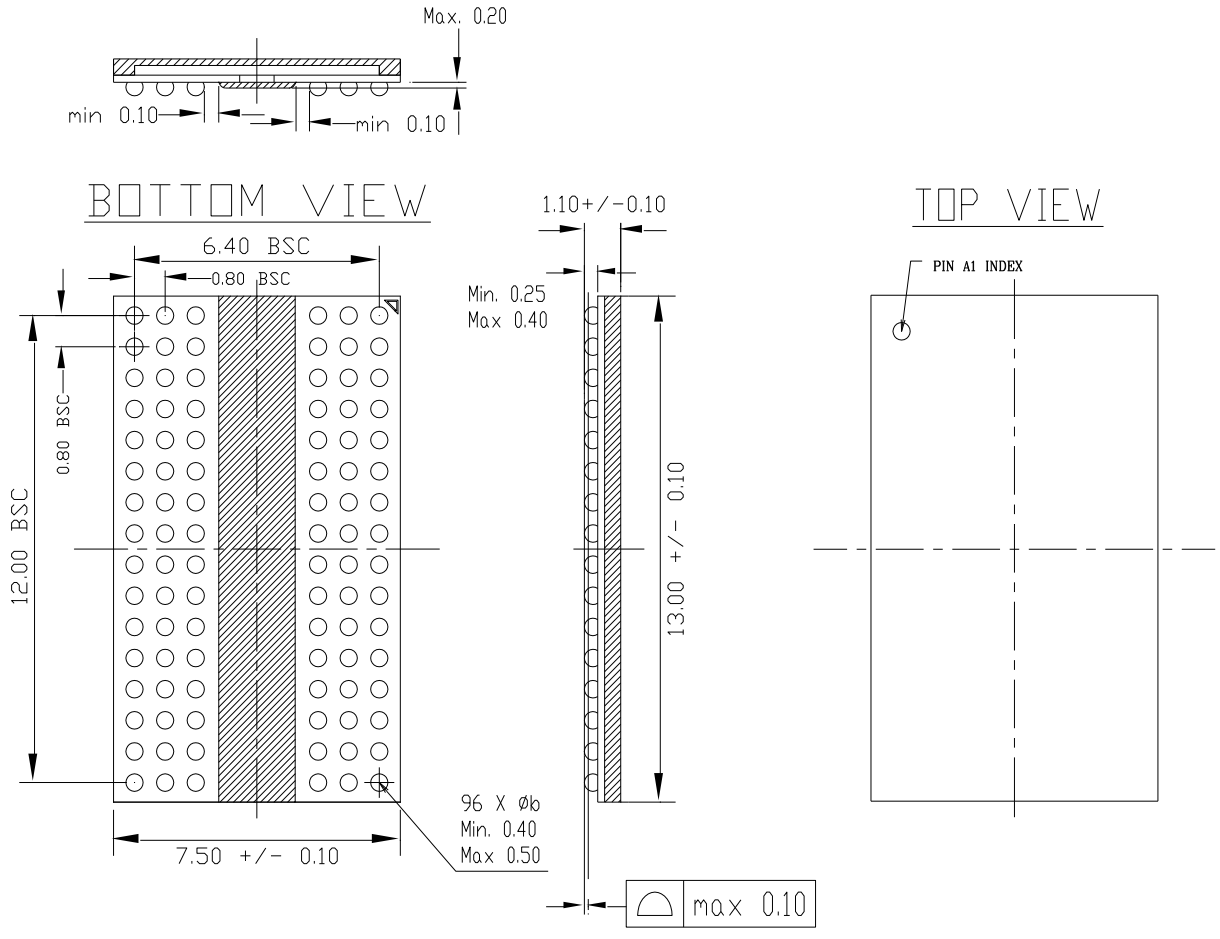
<TOP View>

See the balls through the package



	1	2	3	4	5	6	7	8	9	
A	VDDQ	VSSQ	DQ8				$\overline{DQSU}$	VSSQ	VDDQ	A
B	VPP	VSS	VDD				UDQS	DQ9	VDD	B
C	VDDQ	DQ12	DQ10				DQ11	DQ13	VSSQ	C
D	VDD	VSSQ	DQ14				DQ15	VSSQ	VDDQ	D
E	VSS	$\overline{UDM}$/UDBI	VSSQ				$\overline{LDM}$/LDBI	VSSQ	VSS	E
F	VSSQ	VDDQ	$\overline{DQSL}$				DQ1	VDDQ	ZQ	F
G	VDDQ	DQ0	DQSL				VDD	VSS	VDDQ	G
H	VSSQ	DQ4	DQ2				DQ3	DQ5	VSSQ	H
J	VDD	VDDQ	DQ6				DQ7	VDDQ	VDD	J
K	VSS	CKE	ODT				CK	$\overline{CK}$	VSS	K
L	VDD	$\overline{WE}$/A14	$\overline{ACT}$				$\overline{CS}$	$\overline{RAS}$/A16	VDD	L
M	VREFCA	BG0	A10/AP				A12/$\overline{BC}$	$\overline{CAS}$/A15	VSS	M
N	VSS	BA0	A4				A3	BA1	TEN	N
P	$\overline{RESET}$	A6	A0				A1	A5	$\overline{ALERT}$	P
R	VDD	A8	A2				A9	A7	VPP	R
T	VSS	A11	PAR				NC	A13	VDD	T

Packge Outline Drawing



Ball Descriptions

Symbol	Type	Description
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$.
CKE	Input	**Clock Enable:** CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit and for Self-Refresh entry. CKE is asynchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during Power Down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external rank selection on systems with multiple ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When ODT is enabled, on-die termination (RTT) is applied only to each DQ, DQS, $\overline{DQS}$, $\overline{DM}$/$\overline{DBI}$/TDQS, and $\overline{TDQS}$ signal for x4, x8 configurations (when the TDQS function is enabled via mode register). For the x16 configuration, RTT is applied to each DQ, DQSU, $\overline{DQSU}$, DQSL, $\overline{DQSL}$, $\overline{UDM}$, and $\overline{LDM}$ signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
BA[1:0]	Input	**Bank Address Inputs:** Define the bank (within a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MRS cycle.
BG[1:0]	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0.
$\overline{ACT}$	Input	**Command input:** $\overline{ACT}$ defines the Activation command being entered along with $\overline{CS}$. The input into $\overline{RAS}$/A16, $\overline{CAS}$/A15 and $\overline{WE}$/A14 will be considered as Row Address A16, A15 and A14
$\overline{RAS}$/A16 $\overline{CAS}$/A15 $\overline{WE}$/A14	Input	**Command Inputs:** $\overline{RAS}$/A16, $\overline{CAS}$/A15 and $\overline{WE}$/A14 (along with $\overline{CS}$) define the command being entered. Those pins have multi-function. For example, for activation with $\overline{ACT}$ Low, those are Addressing like A16,A15 and A14 but for non-activation command with $\overline{ACT}$ High, those are Command pins for Read, Write and other command defined in command truth table.
A10/AP	Input	**Auto precharge:** A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12/$\overline{BC}$	Input	**Burst Chop:** Burst chop: A12/$\overline{BC}$ is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = no burst chop; LOW = burst-chopped).
For x4, A[16:0] For x8,x16 A[15:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP, A12/$\overline{BC}$, $\overline{WE}$/A14, $\overline{CAS}$/A15, $\overline{RAS}$/A16, have additional functions; see individual entries in this table). The address inputs also provide the op-code during the MODE REGISTER SET command. A16 is used on some 8Gb.

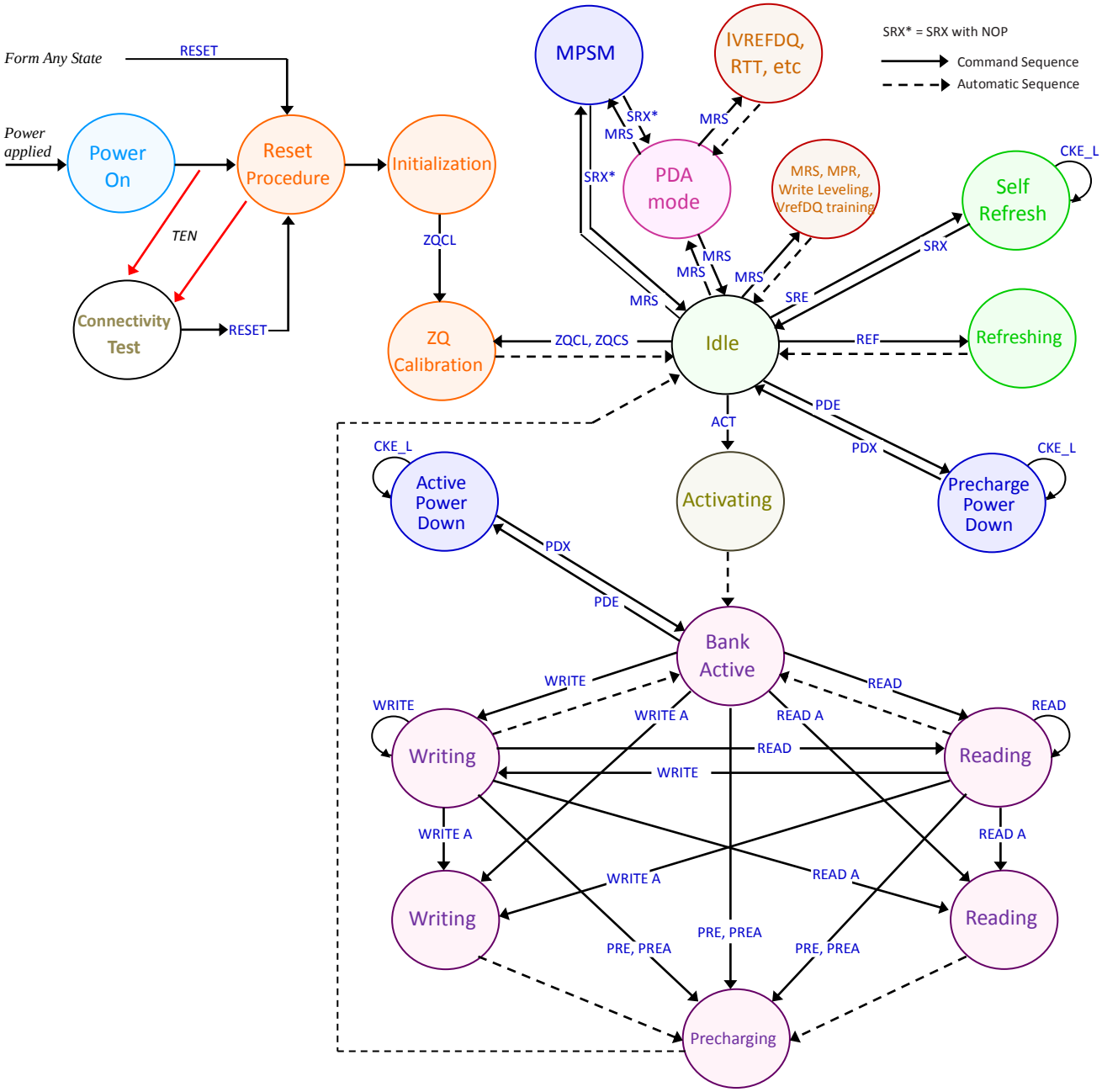
Symbol	Type	Description
PAR	Input	**Parity for command and address:** DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with $\overline{ACT}$,$\overline{RAS}$/A16,$\overline{CAS}$/A15,$\overline{WE}$/A14, A12/$\overline{BC}$,A10/AP, A17-A0, BA0-BA1, BG0-BG1 Command and address inputs shall have parity check performed when commands are latched via the rising edge of CK and when $\overline{CS}$ is low.
DQ	Input/output	**Data input/output:** Bidirectional data bus. DQ represents DQ [3:0], DQ [7:0], and DQ [15:0] for the x4, x8, and x16 configurations, respectively. If Write CRC is enabled via Mode register, then the Write CRC code is added at the end of Data Burst. Either anyone or all DQ0, DQ1, DQ2, and DQ3 is used as monitoring of internal Vref level during test via Mode Register Setting MR4 A4=High, training times change when enabled. During this mode, RTT value should be set to Hi-Z. This measurement is for verification purposes and is NOT an external voltage supply pin.
DQS/$\overline{DQS}$ DQSL/$\overline{DQSL}$ DQSU/$\overline{DQSU}$	Input/output	**Data Strobe:** Output with READ data, input with WRITE data. Edge-aligned with READ data, centered-aligned with WRITE data. For the x16, DQSL corresponds to the data on DQ [7:0]; DQSU corresponds to the data on DQ [15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ [3:0] and DQ [7:0] respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
TDQS/$\overline{TDQS}$	Output	**Termination Data Strobe:** TDQS/$\overline{TDQS}$ is applicable for X8 DRAMs only. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. When enabled via Mode Register A11=1 in MR1, DRAM will enable the same R_{TT} termination resistance function on TDQS/$\overline{TDQS}$ that is applied to DQS/$\overline{DQS}$. When the TDQS function is disabled via the mode register, the $\overline{DM}$/$\overline{DBI}$/TDQS pin will provide the data mask ($\overline{DM}$) function or Data Bus Inversion ($\overline{DBI}$) depending on MR5, and the $\overline{TDQS}$ pin is not used.
$\overline{DM}$ $\overline{LDM}$, $\overline{UDM}$	Input	**Input data mask:** $\overline{DM}$ is an input mask signal for write data. Input data is masked when $\overline{DM}$ is sampled LOW coincident with that input data during a write access. $\overline{DM}$ is sampled on both edges of DQS. $\overline{DM}$ is muxed with $\overline{DBI}$ function by Mode Register A [12:10] setting in MR5. For x8 device, the function of $\overline{DM}$ or TDQS is enabled by Mode Register A11 setting in MR1. $\overline{DBI}$ is an input/output identifying whether to store/output the true or inverted data. If $\overline{DBI}$ is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if $\overline{DBI}$ is HIGH. DM is not supported in X4.
$\overline{DBI}$ $\overline{UDBI}$, $\overline{LDBI}$	Input/output	**DBI input/output:** Data bus inversion. $\overline{DBI}$ is an input/output signal used for data bus inversion in the x8 configuration. $\overline{UDBI}$ and $\overline{LDBI}$ are used in the x16 configuration; $\overline{UDBI}$ is associated with DQ [15:8], and $\overline{LDBI}$ is associated with DQ [7:0]. The DBI feature is not supported on x4 configurations. $\overline{DBI}$ can be configured for both READ (output) and WRITE (input) operations depending on the mode register settings. The DM, DBI, and TDQS functions are enabled by mode register settings. See Data Bus Inversion (DBI).
$\overline{ALERT}$	Output	**Alert output:** It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then $\overline{ALERT}$ goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then $\overline{ALERT}$ goes LOW for relatively long period until ongoing DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, open-drain $\overline{ALERT}$ Pin must be bounded to VDD on board.
TEN	Input	**Connectivity test mode:** Connectivity Test Mode is active when TEN is HIGH, and inactive when TEN is LOW. TEN must be LOW during normal operation. TEN is a CMOS rail-to-rail signal with AC HIGH and LOW at 80% and 20% of VDD (960mV for DC HIGH and 240mV for DC LOW). Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
ZQ	Reference	**Reference pin for ZQ calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to VSSQ.
$\overline{RESET}$	Input	**Active Low Asynchronous Reset:** Reset is active when $\overline{RESET}$ is LOW, and inactive when $\overline{RESET}$ is HIGH. $\overline{RESET}$ must be HIGH during normal operation. $\overline{RESET}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD, i.e. 0.96V for DC high and 0.24V for DC low.

Symbol	Type	Description
VPP	Supply	**DRAM activating power supply:** 2.5V (2.375V min , 2.75V max)
VDD	Supply	**Power Supply:** 1.2V ± 0.06V
VDDQ	Supply	**DQ Power Supply:** 1.2V ± 0.06V
VSS	Supply	**Ground**
VSSQ	Supply	**DQ Ground**
VREFCA	Supply	**Reference voltage for CA**
NC	-	**No Connect:** No internal electrical connection is present.
NF	-	**No function:** May have internal connection present, but has no function.
RFU	-	Reserved for future use.

NOTE Input only pins (BG0-BG1, BA0-BA1, A0-A17, $\overline{ACT}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14, $\overline{CS}$, CKE, ODT, and $\overline{RESET}$) do not supply termination.

Functional Description

Simplified State Diagram



Abbr.	Function	Abbr.	Function	Abbr.	Function
ACT	Active	Read	RD, RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	Precharge All	Write	WR, WRS4, WRS8 with/without CRC	SRE	Self-Refresh entry
RESET	Start RESET Procedure	Write A	WRA, WRAS4, WRAS8 with/without CRC	SRX	Self-Refresh exit
ZQCS	ZQ Calibration Short	TEN	Boundary Scan Mode Enable	MPR	Multi-Purpose Register
ZQCL	ZQ Calibration Long	REF	Refresh, Fine granularity Refresh	MRS	Mode Register Set

Basic Functionality

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen-banks, 4 bank group with 4 banks for each bank group for x8 and eight-banks, 2 bank group with 4 banks for each bankgroup for x16 DRAM. The DDR4 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A15 select the row; refer to Addressing section for more details. The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR4 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

RESET and Initialization Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values for the following MR settings are defined:

Default MR settings for power-up and reset initialization

MR functions	MR bits	Value
Gear-down mode	MR3 A[3]=0	1/2 Rate
Per DRAM Addressability	MR3 A[4]=0	Disable
Max Power Saving Mode	MR4 A[1]=0	Disable
$\overline{CS}$ to Command/Address Latency	MR4 A[8:6]=000	Disable
CA Parity Latency Mode	MR5 A[2:0]=000	Disable
Hard Post Package Repair Mode	MR4 A[13]=0	Disable
Soft Post Package Repair Mode	MR4 A[5]=0	Disable

Power-Up and Initialization Sequence

The following sequence (Step 1-15) is required for power-up and initialization:

1) Apply power ($\overline{RESET}$ and TEN are recommended to be maintained below 0.2 × VDD; all other inputs may be undefined). $\overline{RESET}$ needs to be maintained below 0.2 x VDD for minimum 200µs with stable power and TEN needs to be maintained below 0.2 x VDD for minimum 700µs with stable power. CKE is pulled "LOW" any time before $\overline{RESET}$ is being deasserted (MIN time 10ns). The power voltage ramp time between 300mV to VDD min must be no greater than 200ms, and during the ramp, VDD ≥ VDDQ and (VDD-VDDQ) < 0.3Volts. VPP must ramp at the same time or earlier than VDD, and VPP must be equal to or higher than VDD at all times.

   During power-up, either of the following conditions may exist and must be met:

   • Condition A
   – VDD and VDDQ are driven from a single-power converter output, AND
   – The voltage levels on all balls other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.
   – VTT is limited to 0.76V MAX when the power ramp is finished, AND
   – VREFCA tracks VDD/2.

   • Condition B
   – Apply VDD without any slope reversal before or at the same time as VDDQ.
   – Apply VDDQ without any slope reversal before or at the same time as VTT and VREFCA.
   – Apply VPP without any slope reversal before or at the same time as VDD.
   – The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

2) After $\overline{RESET}$ is de-asserted, wait for another 500µs until CKE becomes active.
   During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.

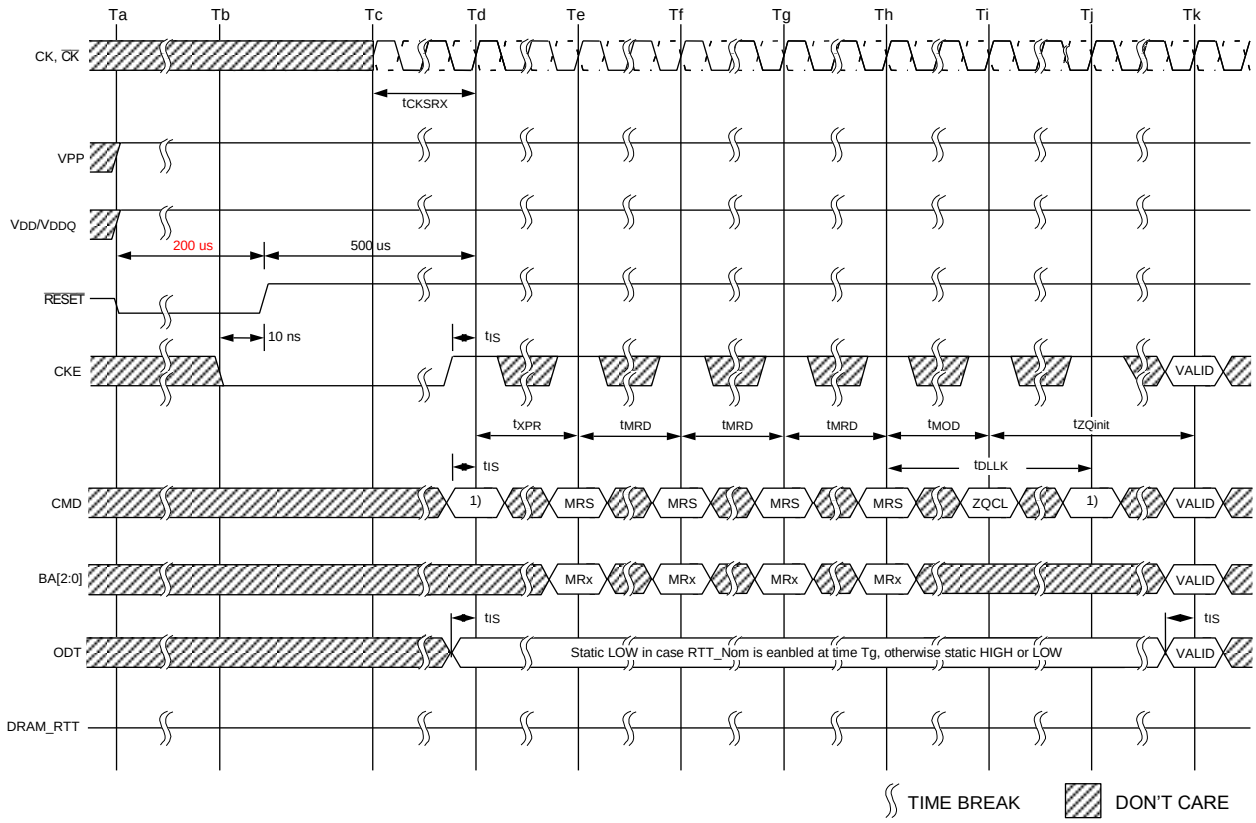
3) Clocks (CK, $\overline{CK}$) need to be started and stabilized for at least 10ns or 5 tCK (whichever is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding setup time to clock (tIS) must be met. Also a DESELECT command must be registered (with tIS setup time to clock) at clock edge Td. Once the CKE is registered "HIGH" after RESET, CKE needs to be continuously registered "HIGH" until the initialization sequence is finished, including expiration of tDLLK and tZQINIT.

4) The DDR4 SDRAM keeps its ODT in High-Impedance state as long as $\overline{RESET}$ is asserted. Further, the SDRAM keeps its ODT in High-Impedance state after $\overline{RESET}$ deassertion until CKE is registered HIGH. The ODT input signal may be in an undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power-up initialization sequence is

finished, including the expiration of tDLLK and tZQINIT.

5) After CKE is registered HIGH, wait a minimum of RESET CKE EXIT time, tXPR, before issuing the first MRS command to load mode register (tXPR = MAX (tXS; 5 × tCK).
6) Issue MRS command to load MR3 with all application settings, wait tMRD.
7) Issue MRS command to load MR6 with all application settings, wait tMRD.
8) Issue MRS command to load MR5 with all application settings, wait tMRD.
9) Issue MRS command to load MR4 with all application settings, wait tMRD.
10) Issue MRS command to load MR2 with all application settings, wait tMRD.
11) Issue MRS command to load MR1 with all application settings, wait tMRD.
12) Issue MRS command to load MR0 with all application settings, wait tMOD.
13) Issue a ZQCL command to starting ZQ calibration.
14) Wait for both tDLLK and tZQINIT completed.
15) The DDR4 SDRAM is now ready for read/write training (include Vref training and Write leveling).

RESET and Initialization Sequence at Power-On Ramping



NOTE 1 From the time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
NOTE 2 MRS commands must be issued to all mode registers that have defined settings.

VDD Slew rate at Power-up Initialization Sequence

VDD Slew Rate

Symbol	Min	Max	Units	NOTE
VDD_sl	0.004	600	V/ms	1,2
VDD_ona		200	ms	3

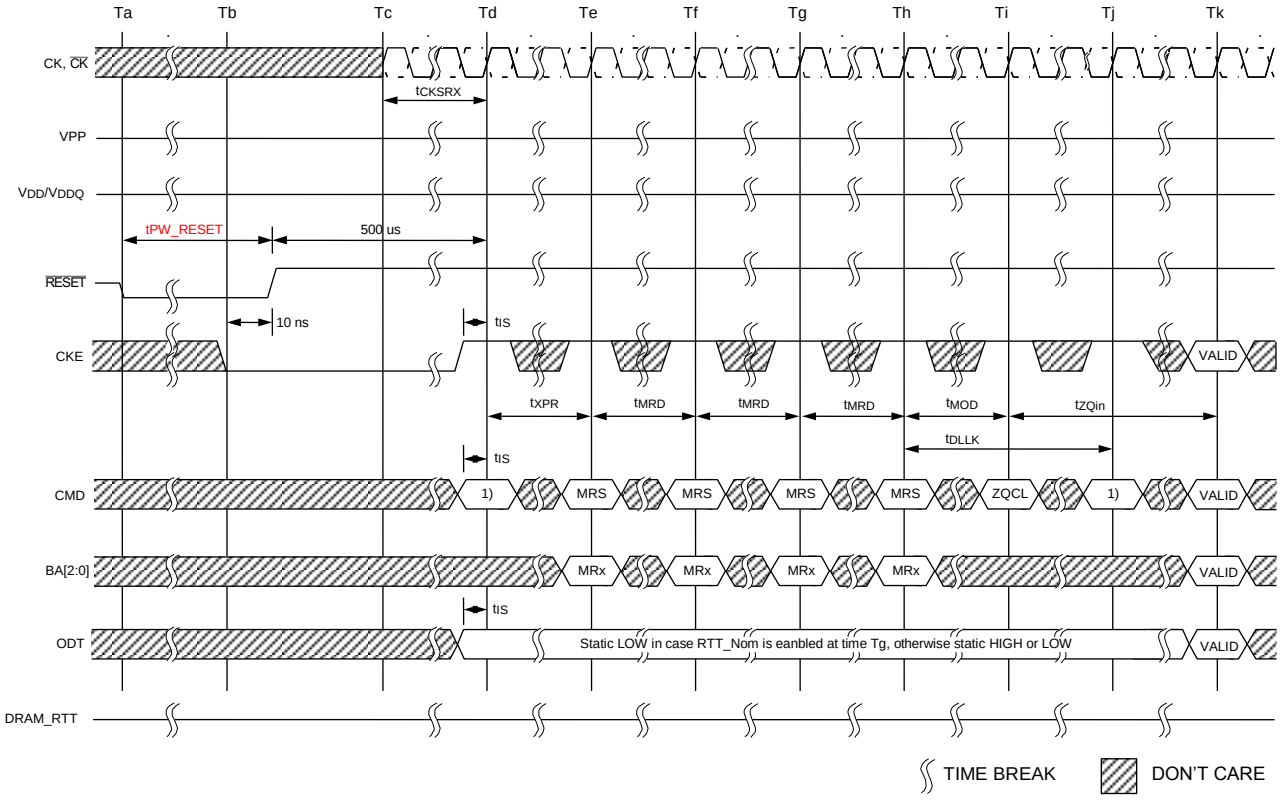
NOTE 1 Measurement made between 300mV and 80% VDD minimum.
NOTE 2 20 MHz bandlimited measurement
NOTE 3 Maximum time to ramp VDD from 300 mV to VDD minimum.

RESET Initialization with Stable Power Sequence

The following sequence is required for $\overline{\text{RESET}}$ at no power interruption initialization:

1. Assert $\overline{\text{RESET}}$ below 0.2 × VDD anytime when reset is needed (all other inputs may be undefined). $\overline{\text{RESET}}$ needs to be maintained for minimum tPW_RESET. CKE is pulled LOW before $\overline{\text{RESET}}$ being de-asserted (MIN time 10ns).
2. Follow Steps 2 to 10 in the Reset and Initialization Sequence at Power-on Ramping procedure.
3. The reset sequence is now completed, DDR4 SDRAM is ready for Read/Write training (include Vref training and Write leveling)

RESET Procedure at Power Stable



NOTE 1 From the time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
NOTE 2 MRS commands must be issued to all mode registers that have defined settings.

Register Definition

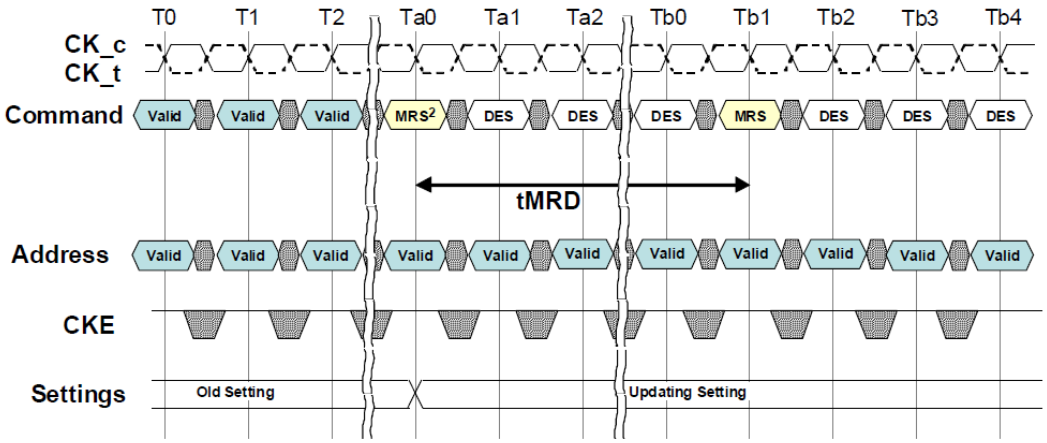
Programming the mode registers

For application flexibility, various functions, features, and modes are programmable in seven Mode Registers, provided by the DDR4 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. The mode registers are divided into various fields depending on the functionality and/or modes. As not all the Mode Registers (MR#) have default values defined, contents of Mode Registers must be initialized and/or re-initialized, i.e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents. MRS Commands can be issued only when DRAM is at idle state. The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands.

tMRD Timing

Some of the Mode Register setting affect to address/command/control input functionality. These case, next MRS command can be allowed when the function updating by current MRS command completed.

The MRS commands which do not apply tMRD timing to next MRS command are listed in note 2 of the following figure. These MRS command input cases have unique MR setting procedure, so refer to individual function description.



NOTE 1 This timing diagram depicts C/A Parity Mode "Disabled" case.

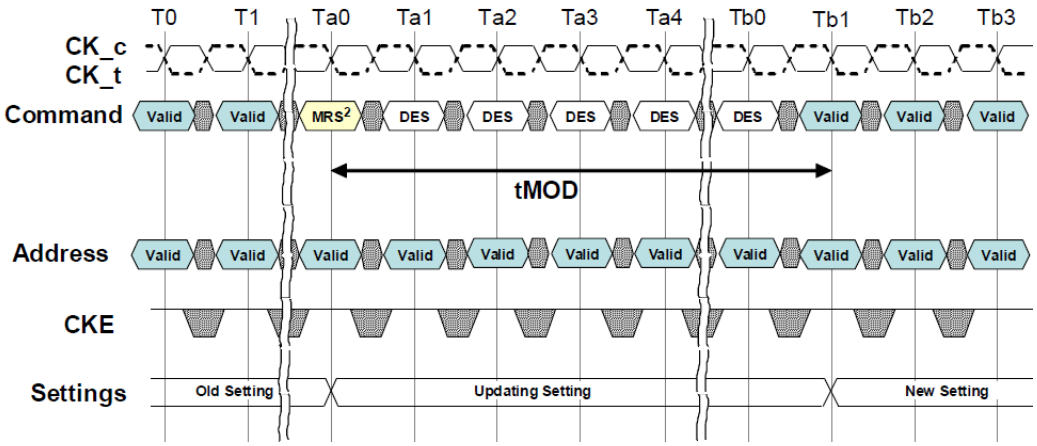
NOTE 2 tMRD applies to all MRS commands with the following exceptions:

- Geardown Mode
- C/A Parity Latency Mode
- CS to Command/Address Latency Mode
- Per DRAM Addressability Mode
- VrefDQ training value, VrefDQ training mode, and VrefDQ Training Range

tMOD Timing

The MRS command to nonMRS command delay, tMOD, is required for the DRAM to update features, except DLL RESET, and is the minimum time required from an MRS command to a nonMRS command, excluding DES.

Some of the mode register setting cases, function updating takes longer than tMOD. The MRS commands which do not apply tMOD timing to next valid command excluding DES is listed in note 2 of the following figure. These MRS command input cases have unique MR setting procedure, so refer to individual function description.



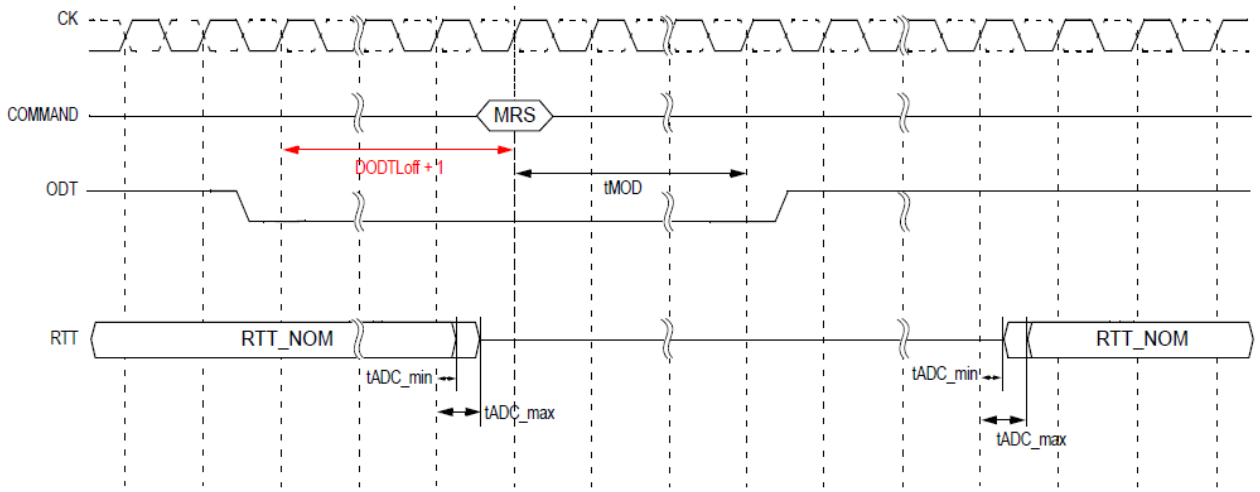
NOTE 1 This timing diagram depicts C/A Parity Mode "Disabled" case.

NOTE 2 List of MRS commands exception that do not apply to tMOD.

- DLL Enable, DLL Reset
- VrefDQ training value, internal Vref monitor, VrefDQ training mode, and VrefDQ Training Range
- Geardown Mode
- Per DRAM Addressability Mode
- Maximum Power Saving Mode
- CA Parity Mode

ODT Status at MRS affecting ODT turn-on/off timing

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e., all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. For MRS command, If RTT_Nom function is intended to change (enable to disable and vice versa) or already enabled in DRAM MR, ODT signal must be registered Low ensuring RTT_NOM is in an off state prior to MRS command affecting RTT_NOM turn-on and off timing. Refer to note2 of the following figure for this type of MRS. The ODT signal may be registered high after tMOD has expired. ODT signal is a don't care during MRS command if DRAM RTT_Nom function is disabled in the mode register prior and after an MRS command.



NOTE 1 This timing diagram shows CA Parity Latency mode is "Disable" case.

NOTE 2 When an MRS command mentioned in this note affects RTT_NOM turn on timings, RTT_NOM turn off timings and RTT_NOM value, this means the MR register value changes. The ODT signal should set to be low for at least DODTLoff +1 clock before their affecting MRS command is issued and remain low until tMOD expires. The following MR registers affects RTT_NOM turn on timings, RTT_NOM turn off timings and RTT_NOM value and it requires ODT to be low when an MRS command change the MR register value. If there are no change the MR register value that correspond to commands mentioned in this note, then ODT signal is not require to be low.

- DLL control for precharge power down
- Additive latency and CAS read latency
- DLL enable and disable
- CAS write latency
- CA Parity mode
- Gear Down mode
- RTT_NOM

Mode Register

MR0

Address	Operating Mode	Description
BG[1]	RFU	0 = must be programmed to 0 during MRS
BG[0], BA[1:0]	MR Select	BG0 / BA1 / BA0 / MR Select **0 / 0 / 0 / MR0** 0 / 0 / 1 / MR1 0 / 1 / 0 / MR2 0 / 1 / 1 / MR3 1 / 0 / 0 / MR4 1 / 0 / 1 / MR5 1 / 1 / 0 / MR6 1 / 1 / 1 / RCW[1]
A[17]	RFU	0 = must be programmed to 0 during MRS
A[13][5], A[11:9]	WR and RTP[2,3]	See table: Write Recovery and Read to Precharge
A[8]	DLL Reset	0 = No 1 = Yes
A[7]	TM	0 = Normal 1 = Test
A[12, 6:4, 2]	CAS Latency[4]	See Table: CAS Latency
A[3]	Read Burst Type	0 = Sequential 1 = Interleave
A[1:0]	Burst Length	00 = 8 (Fixed) Abbreviated BL8 01 = BC4 or 8 (on the fly) Abbreviated BC4OTF or BL8OTF 10 = BC4 (Fixed) Abbreviated BC4 11 = Reserved

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA [1:0] =111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 2 WR (write recovery for autoprecharge) min in clock cycles is calculated by following rounding algorithm. The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.

NOTE 3 The table shows the encodings for Write Recovery and internal Read command to Precharge command delay. For actual Write recovery timing, please refer to AC timing table.

NOTE 4 The table only shows the encodings for a given CAS Latency. For actual supported CAS Latency, please refer to speed bin tables for each frequency. CAS Latency controlled by A12 is optional for 4Gb device.

NOTE 5 A13 for WR and RTP setting is optional for 4Gb.

Write Recovery and Read to Precharge (cycles)

A13	A11	A10	A9	WR	RTP
0	0	0	0	10	5
0	0	0	1	12	6
0	0	1	0	14	7
0	0	1	1	16	8
0	1	0	0	18	9
0	1	0	1	20	10
0	1	1	0	24	12
0	1	1	1	22	11
1	0	0	0	26	13
1	0	0	1	RFU	RFU
1	0	1	0	RFU	RFU
1	0	1	1	RFU	RFU
1	1	0	0	RFU	RFU
1	1	0	1	RFU	RFU
1	1	1	0	RFU	RFU
1	1	1	1	RFU	RFU

CAS Latency

A12	A6	A5	A4	A2	CAS Latency
0	0	0	0	0	Reserved
0	0	0	0	1	Reserved
0	0	0	1	0	**11**
0	0	0	1	1	**12**
0	0	1	0	0	**13**
0	0	1	0	1	Reserved
0	0	1	1	0	**15**
0	0	1	1	1	Reserved
0	1	0	0	0	**18**(1)
0	1	0	0	1	**20**(1)
0	1	0	1	0	**22**(1)
0	1	0	1	1	Reserved
0	1	1	0	0	Reserved
0	1	1	0	1	**17**
0	1	1	1	0	**19**
0	1	1	1	1	Reserved
1	0	0	0	0	Reserved
1	0	0	0	1	Reserved
1	0	0	1	0	Reserved
1	0	0	1	1	Reserved
1	0	1	0	0	Reserved
1	0	1	0	1	Reserved
1	0	1	1	0	Reserved
1	0	1	1	1	Reserved
1	1	0	0	0	Reserved

Note 1: this CL setting is related to read DBI usage only and please check “Speed bin” section and have a proper corresponding option to use.

MR1

Address	Operating Mode	Description
BG[1]	RFU	0 = must be programmed to 0 during MRS
BG[0], BA[1:0]	MR Select	<table><tr><th>BG0</th><th>BA1</th><th>BA0</th><th>MR Select</th></tr><tr><td>0</td><td>0</td><td>0</td><td>MR0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>MR1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>MR2</td></tr><tr><td>0</td><td>1</td><td>1</td><td>MR3</td></tr><tr><td>1</td><td>0</td><td>0</td><td>MR4</td></tr><tr><td>1</td><td>0</td><td>1</td><td>MR5</td></tr><tr><td>1</td><td>1</td><td>0</td><td>MR6</td></tr><tr><td>1</td><td>1</td><td>1</td><td>RCW[3]</td></tr></table>
A[17]	RFU	0 = must be programmed to 0 during MRS
A[13]	RFU	0 = must be programmed to 0 during MRS
A[12]	Qoff[1]	0 = Output buffer enable 1 = Output buffer disable
A[11]	TDQS enable	0 = Disable 1 = Enable
A[10:8]	RTT_NOM	See Table: RTT_NOM
A[7]	Write Leveling Enable	0 = Disable 1 = Enable
A[6:5]	RFU	0 = must be programmed to 0 during MRS
A[4:3]	Additive Latency	00 = 0 (AL disabled) 01 = CL-1 10 = CL-2 11 = Reserved
A[2:1]	Output Driver Impedance Control	See Table: Output Driver Impedance Control
A[0]	DLL Enable	0 = Disable[2] 1 = Enable

NOTE 1 Outputs disabled - DQs, DQSs, $\overline{\text{DQS}}$s.

NOTE 2 States reversed to “0 as Disable” with respect to DDR4.

NOTE 3 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA [1:0] =111 and doesn’t respond. When RFU MR code setting is inputted, DRAM operation is not defined.

RTT_NOM

A10	A9	A8	RTT_NOM
0	0	0	Disabled
0	0	1	RZQ/4 (60 Ω)
0	1	0	RZQ/2 (120 Ω)
0	1	1	RZQ/6 (40 Ω)
1	0	0	RZQ/1 (240 Ω)
1	0	1	RZQ/5 (48 Ω)
1	1	0	RZQ/3 (80 Ω)
1	1	1	RZQ/7 (34 Ω)

Output Driver Impedance Control

A2	A1	ODI
0	0	RZQ/7(34 ohm)
0	1	RZQ/5(48 ohm)
1	0	RFU
1	1	RFU

MR2

Address	Operating Mode	Description
BG[1]	RFU	0 = must be programmed to 0 during MRS
BG[0], BA[1:0]	MR Select	<table><tr><th>BG0</th><th>BA1</th><th>BA0</th><th>MR Select</th></tr><tr><td>0</td><td>0</td><td>0</td><td>MR0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>MR1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>MR2</td></tr><tr><td>0</td><td>1</td><td>1</td><td>MR3</td></tr><tr><td>1</td><td>0</td><td>0</td><td>MR4</td></tr><tr><td>1</td><td>0</td><td>1</td><td>MR5</td></tr><tr><td>1</td><td>1</td><td>0</td><td>MR6</td></tr><tr><td>1</td><td>1</td><td>1</td><td>RCW[1]</td></tr></table>
A[17]	RFU	0 = must be programmed to 0 during MRS
A[13]	RFU	0 = must be programmed to 0 during MRS
A[12]	Write_CRC	0 = Disable 1 = Enable
A[11:9]	RTT_WR	See Table: RTT_WR
A[8]	RFU	0 = must be programmed to 0 during MRS
A[7:6]	Low Power Auto Self Refresh (LPASR)	00 = Manual Mode (Normal Operating Temperature Range) 01 = Manual Mode (Reduced Operating Temperature Range) 10 = Manual Mode (Extended Operating Temperature Range) 11 = ASR Mode (Auto Self Refresh)
A[5:3]	CAS Write Latency(CWL)	See Table: CWL (CAS Write Latency)
A[2:0]	RFU	0 = must be programmed to 0 during MRS

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA [1:0] =111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

RTT_WR

A11	A10	A9	RTT_WR
0	0	0	Dynamic ODT off
0	0	1	RZQ/2
0	1	0	RZQ/1
0	1	1	Hi-Z
1	0	0	RZQ/3
1	0	1	RFU
1	1	0	RFU
1	1	1	RFU

CAS Write Latency (CWL)

A5	A4	A3	CWL	Speed Grade in MT/s			
				1 tCK tWPRE		2 tCK tWPRE[1]	
				1st Set	2nd Set	1st Set	2nd Set
0	0	0	9	1600	-	-	-
0	0	1	10	1866	-	-	-
0	1	0	11	2133	1600	-	-
0	1	1	12	2400	1866	-	-
1	0	0	14	2666	2133	2400	-
1	0	1	16	-	2400	2666	2400
1	1	0	18	-	2666	-	2666
1	1	1	20	-	-	-	-

NOTE 1 The 2 tCK Write Preamble is valid for DDR4-2400/2666 Speed Grade. For the 2nd Set of 2 tCK Write Preamble, no additional CWL is needed.

MR3

Address	Operating Mode	Description
BG[1]	RFU	0 = must be programmed to 0 during MRS
BG[0], BA[1:0]	MR Select	<table><tr><th>BG0</th><th>BA1</th><th>BA0</th><th>MR Select</th></tr><tr><td>0</td><td>0</td><td>0</td><td>MR0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>MR1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>MR2</td></tr><tr><td>0</td><td>1</td><td>1</td><td>MR3</td></tr><tr><td>1</td><td>0</td><td>0</td><td>MR4</td></tr><tr><td>1</td><td>0</td><td>1</td><td>MR5</td></tr><tr><td>1</td><td>1</td><td>0</td><td>MR6</td></tr><tr><td>1</td><td>1</td><td>1</td><td>RCW[1]</td></tr></table>
A[17]	RFU	0 = must be programmed to 0 during MRS
A[13]	RFU	0 = must be programmed to 0 during MRS
A[12:11]	MPR Read Format	00 = Serial 01 = Parallel 10 = Staggered 11 = Reserved
A[10:9]	Write CMD Latency when CRC and DM are enabled	See Table: Write Command Latency when CRC and DM are both enabled
A[8:6]	Fine Granularity Refresh Mode	See Table: Fine Granularity Refresh Mode
A[5]	Temperature sensor readout[2]	0 = Disable 1 = Enable
A[4]	Per DRAM Addressability	0 = Disable 1 = Enable
A[3]	Geardown Mode	0 = 1/2 Rate 1 = 1/4 Rate
A[2]	MPR Operation	0 = Normal 1 = Dataflow from/to MPR
A[1:0]	MPR Page Selection	00 = Page0 01 = Page1 10 = Page2 11 = Page3 See Table: MPR Data Format

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA [1:0] =111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 2 Please confirm with NTC.

Fine Granularity Refresh Mode

A8	A7	A6	Fine Granularity Refresh Mode
0	0	0	Normal (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	RFU
1	0	0	RFU
1	0	1	Enable On-the-fly 1x/2x
1	1	0	Enable On-the-fly 1x/4x
1	1	1	RFU

MR3 A<10:9> Write Command Latency when CRC and DM are both enabled

A10	A9	CRC+DM Write CMD Latency	Operating Data Rate
0	0	4nCK	1600
0	1	5nCK	1866/2133/2400/2666
1	0	6nCK	RFU
1	1	RFU	RFU

NOTE 1 Write Command latency when CRC and DM are both enabled

NOTE 2 At less than or equal to 1600 then 4nCK; neither 5nCK nor 6nCK

NOTE 3 At greater than 1600 and less than or equal to 2666 then 5nCK; neither 4nCK nor 6nCK

MPR Data Format

MR3 MPR Page A[1:0]	Purpose	MPR Location BA[1:0]	MPR Bit Write Location [7:0]								Note
			7	6	5	4	3	2	1	0	
			Read Burst Order (serial mode)								
			UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7	
00 Page 0	Training Patterns	**00** = MPR0	0	1	0	1	0	1	0	1	1,2
		01 = MPR1	0	0	1	1	0	0	1	1	
		10 = MPR2	0	0	0	0	1	1	1	1	
		11 = MPR3	0	0	0	0	0	0	0	0	
01 Page 1	C/A Parity Error Log	**00** = MPR0	A7	A6	A5	A4	A3	A2	A1	A0	3,4,5,6
		01 = MPR1	$\overline{CAS}$/A15	$\overline{WE}$/A14	A13	A12	A11	A10	A9	A8	
		10 = MPR2	PAR	$\overline{ACT}$	BG1	BG0	BA1	BA0	A17[6]	$\overline{RAS}$/A16	
		11 = MPR3	CRC Error Status	CA Parity Error Status	CA Parity Latency[6]			-	-	-	
					MR5	MR5	MR5				
					A2	A1	A0				
10 Page 2	MRS Readout	**00** = MPR0	hPPR	sPPR	RTT_WR	Temperature Sensor Status[8]		CRC Write Enable	R_{TT}_WR		
			-	-	MR2	Refer to next table		MR2	MR2		
			-	-	A11			A12	A10	A9	
		01 = MPR1	Vref DQ range	Vref DQ training Value						Geardown Enable	
			MR6	MR6						MR3	
			A6	A5	A4	A3	A2	A1	A0	A3	
		10 = MPR2	CAS Latency					CAS Write Latency			
			MR0					MR2			
			A6	A5	A4	A2	A12	A5	A4	A3	
		11 = MPR3	R_{TT}_NOM			R_{TT}_PARK			Driver Impedance		
			MR1			MR5			MR1		
			A10	A9	A6	A8	A7	A6	A2	A1	
11 Page 3	Vendor use only[7]	**00** = MPR0	Don't care								7
		01 = MPR1	Don't care								
		10 = MPR2	Don't care								
		11 = MPR3	Don't care								

NOTE 1 MPRx using A7:A0 that A7 is mapped to location [7] and A0 is mapped to location [0].
NOTE 2 Training pattern be defined by MPR0-MPR3 which are default value of Page 0 read and write
NOTE 3 MPR used for C/A parity error log readout is enabled by setting A [2] in MR3
NOTE 4 For higher density of DRAM, where A [17] is not used, MPR2[1] should be treated as don't care.
NOTE 5 If a device is used in monolithic application, where C [2:0] are not used, then MPR3[2:0] should be treated as don't care.
NOTE 6 MPR3 bit 0~2 (CA parity latency) reflects the latest programmed CA parity latency values.
NOTE 7 MPR page3 is specifically assigned to DRAM. Actual encoding method is vendor specific.
NOTE 8 Please confirm with NTC.

Temperature Sensor Status

MPR0 bit A4	MPR0 bit A3	Refresh Rate Range	MR3[5]
0	0	Sub 1x refresh (>tREFI)	**MR3 bit A5=1 (Temperature sensor readout = Enabled)** DRAM updates the temperature sensor status to MPR Page 2 (MPR0 bits A [4:3]). Temperature data is guaranteed by the DRAM to be no more than 32ms old at the time of MPR Read of the Temperature Sensor Status bits. **MR3 bit A5=0 (Temperature sensor readout = Disabled)** DRAM disables updates to the temperature sensor status in MPR Page 2(MPR0-bit A[4:3])
0	1	1x refresh rate (= tREFI)	
1	0	2x refresh rate (1/2 x tREFI)	
1	1	RFU	

MR4

Address	Operating Mode	Description
BG[1]	RFU	0 = must be programmed to 0 during MRS
BG[0], BA[1:0]	MR Select	<table><tr><th>BG0</th><th>BA1</th><th>BA0</th><th>MR Select</th></tr><tr><td>0</td><td>0</td><td>0</td><td>MR0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>MR1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>MR2</td></tr><tr><td>0</td><td>1</td><td>1</td><td>MR3</td></tr><tr><td>1</td><td>0</td><td>0</td><td>MR4</td></tr><tr><td>1</td><td>0</td><td>1</td><td>MR5</td></tr><tr><td>1</td><td>1</td><td>0</td><td>MR6</td></tr><tr><td>1</td><td>1</td><td>1</td><td>RCW[1]</td></tr></table>
A[17]	RFU	0 = must be programmed to 0 during MRS
A[13]	hPPR	0 = Disable 1 = Enable
A[12]	Write Preamble	0 = 1 nCK 1 = 2 nCK
A[11]	Read Preamble	0 = 1 nCK 1 = 2 nCK
A[10]	Read Preamble Taring Mode	0 = Disable 1 = Enable
A[9]	Self Refresh Abort	0 = Disable 1 = Enable
A[8:6]	CS to CMD/ADDR Latency Mode (Cycles)	See Table: CS to CMD/ADDR Latency Mode Setting
A[5]	sPPR	0 = Disable 1 = Enable
A[4]	Internal Vref Monitor	0 = Disable 1 = Enable
A[3]	Temperature Controlled Refresh Mode	0 = Disable 1 = Enable
A[2]	Temperature Controlled Refresh Range	0 = Normal 1 = Extended
A[1]	Maximum Power Down Mode	0 = Disable 1 = Enable
A[0]	RFU	0 = must be programmed to 0 during MRS

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA [1:0] =111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

CS to CMD / ADDR Latency Mode Setting

A8	A7	A6	CAL
0	0	0	Disabled
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	8
1	1	0	Reserved
1	1	1	Reserved

MR5

Address	Operating Mode	Description
BG[1]	RFU	0 = must be programmed to 0 during MRS
BG[0], BA[1:0]	MR Select	<table><tr><th>BG0</th><th>BA1</th><th>BA0</th><th>MR Select</th></tr><tr><td>0</td><td>0</td><td>0</td><td>MR0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>MR1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>MR2</td></tr><tr><td>0</td><td>1</td><td>1</td><td>MR3</td></tr><tr><td>1</td><td>0</td><td>0</td><td>MR4</td></tr><tr><td>1</td><td>0</td><td>1</td><td>MR5</td></tr><tr><td>1</td><td>1</td><td>0</td><td>MR6</td></tr><tr><td>1</td><td>1</td><td>1</td><td>RCW[1]</td></tr></table>
A[17]	RFU	0 = must be programmed to 0 during MRS
A[13]	RFU	0 = must be programmed to 0 during MRS
A[12]	Read DBI	0 = Disable 1 = Enable
A[11]	Write DBI	0 = Disable 1 = Enable
A[10]	Data Mask	0 = Disable 1 = Enable
A[9]	CA Parity Persistent Error	0 = Disable 1 = Enable
A[8:6]	RTT_PARK	See Table: RTT_PARK
A[5]	ODT Input Buffer during Power Down Mode	0 = ODT input buffer is activated 1 = ODT input buffer is deactivated
A[4]	C/A Parity Error Status	0 = Clear 1 = Error
A[3]	CRC Error Clear	0 = Clear 1 = Error
A[2:0]	C/A Parity Latency Mode	See Table: C/A Parity Latency Mode

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA [1:0] =111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 2 When RTT_NOM Disable is set in MR1, A5 of MR5 will be ignored.

RTT_PARK

A8	A7	A6	RTT_PARK
0	0	0	RTT_PARK Disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

C/A Parity Latency Mode

A2	A1	A0	CA Parity Latency	Speed Bin
0	0	0	Disabled	
0	0	1	4	1600/1866/2133
0	1	0	5	2400/2666
0	1	1	6	RFU
1	0	0	8	RFU
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

NOTE 1 Parity latency must be programmed according to timing parameters by speed grade table.

MR6

Address	Operating Mode	Description
BG[1]	RFU	0 = must be programmed to 0 during MRS
BG[0], BA[1:0]	MR Select	BG0 / BA1 / BA0 / MR Select 0 / 0 / 0 / MR0 0 / 0 / 1 / MR1 0 / 1 / 0 / MR2 0 / 1 / 1 / MR3 1 / 0 / 0 / MR4 1 / 0 / 1 / MR5 **1 / 1 / 0 / MR6** 1 / 1 / 1 / RCW[1]
A[17]	RFU	0 = must be programmed to 0 during MRS
A[13]	RFU	0 = must be programmed to 0 during MRS
A[12:10]	tCCD_L	See Table: tCCD_L & tDLLK
A[9:8]	RFU	0 = must be programmed to 0 during MRS
A[7]	VrefDQ Training Enable	0 = Disable (Normal Operation Mode) 1 = Enable(Training Mode)
A[6]	VrefDQ Training Range	0 = Range 1 1 = Range 2
A[5:0]	VrefDQ Training Value	See Table: VrefDQ Training Values

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA [1:0] =111 and doesn't respond.

tCCD_L & tDLLK

A12	A11	A10	tCCD_L.min(nCK)	tDLLK.min(nCK)	Note
0	0	0	Reserved	-	-
0	0	1	5	597	1600Mbps ≦ Data rate ≦ 1866Mbps (1600/1866Mbps)
0	1	0	6	768	1866Mbps < Data rate ≦ 2400Mbps (2133/2400Mbps)
0	1	1	7	1024	2400Mbps < Data rate ≦ 2666Mbps (2666 Mbps)
1	0	0	8		2666Mbps < Data rate ≦ 3200Mbps (2933/3200 Mbps)
1	0	1	Reserved	-	-
1	1	0			-
1	1	1			-

NOTE 1 tCCD_L/tDLLK should be programmed according to the value defined in AC parameter table per operating frequency.

VrefDQ Training Values

MR6 [5:0]	Range 1 MR6 A6=0	Range 2 MR6 A6=1	MR6 [5:0]	Range 1 MR6 A6=0	Range 2 MR6 A6=1	MR6 [5:0]	Range 1 MR6 A6=0	Range 2 MR6 A6=1	MR6 [5:0]	Range 1 MR6 A6=0	Range 2 MR6 A6=1
000000	60.00%	45.00%	001101	68.45%	53.45%	011010	76.90%	61.90%	100111	85.35%	70.35%
000001	60.65%	45.65%	001110	69.10%	54.10%	011011	77.55%	62.55%	101000	86.00%	71.00%
000010	61.30%	46.30%	001111	69.75%	54.75%	011100	78.20%	63.20%	101001	86.65%	71.65%
000011	61.95%	46.95%	010000	70.40%	55.40%	011101	78.85%	63.85%	101010	87.30%	72.30%
000100	62.60%	47.60%	010001	71.05%	56.05%	011110	79.50%	64.50%	101011	87.95%	72.95%
000101	63.25%	48.25%	010010	71.70%	56.70%	011111	80.15%	65.15%	101100	88.60%	73.60%
000110	63.90%	48.90%	010011	72.35%	57.35%	100000	80.80%	65.80%	101101	89.25%	74.25%
000111	64.55%	49.55%	010100	73.00%	58.00%	100001	81.45%	66.45%	101110	89.90%	74.90%
001000	65.20%	50.20%	010101	73.65%	58.65%	100010	82.10%	67.10%	101111	90.55%	75.55%
001001	65.85%	50.85%	010110	74.30%	59.30%	100011	82.75%	67.75%	110000	91.20%	76.20%
001010	66.50%	51.50%	010111	74.95%	59.95%	100100	83.40%	68.40%	110001	91.85%	76.85%
001011	67.15%	52.15%	011000	75.60%	60.60%	100101	84.05%	69.05%	110010	92.50%	77.50%
001100	67.80%	52.80%	011001	76.25%	61.25%	100110	84.70%	69.70%	110011 to 111111	Reserved	Reserved

MR7 DRAM: Ignore

The DDR4 SDRAM shall ignore any access to MR7 for all DDR4 SDRAM. Any bit setting within MR7 may not take any effect in the DDR4 SDRAM.

DDR4 SDRAM Command Description and Operation

Command Truth Table

Note 1,2,3 and 4 apply to the entire Command truth table.
Note 5 applies to all Read/Write commands.
BG = Bank Group Address; BA = Bank Address; RA =Row Address; CA = Column Address;$\overline{BC}$ = Burst Chop;
X = Don't Care; V = Valid H or L

Symbol	Function		CKE		$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ /A16	$\overline{CAS}$ /A15	$\overline{WE}$ /A14	BG [1:0]	BA [1:0]	A12 /$\overline{BC}$	A [13,11]	A10 /AP	A [9:0]	Notes
			Prev.	Pres.												
MRS	Mode Register Set		H	H	L	H	L	L	L	BG	BA	OP code				12
REF	REFRESH		H	H	L	H	L	L	H	V	V	V	V	V	V	
SRE	Self Refresh Entry		H	L	L	H	L	L	H	V	V	V	V	V	V	7,9
SRX	Self Refresh Exit		L	H	H	X	X	X	X	X	X	X	X	X	X	7,8,9,10
					L	H	H	H	H	V	V	V	V	V	V	
PRE	Single-Bank Precharge		H	H	L	H	L	H	L	BG	BA	V	V	L	V	
PREA	Precharge All Banks		H	H	L	H	L	H	L	V	V	V	V	H	V	
RFU	Reserved For Future Use		H	H	L	H	L	H	H	RFU						
ACT	Bank Active		H	H	L	L	Row Address(RA)			BG	BA	Row Address (RA)				
WR	WRITE	Fixed BL8 or BC4	H	H	L	H	H	L	L	BG	BA	V	V	L	CA	
WRS4		BC4,on the fly	H	H	L	H	H	L	L	BG	BA	L	V	L	CA	
WRS8		BL8,on the fly	H	H	L	H	H	L	L	BG	BA	H	V	L	CA	
WRA	WRITE with auto precharge	Fixed BL8 or BC4	H	H	L	H	H	L	L	BG	BA	V	V	H	CA	
WRAS4		BC4,on the fly	H	H	L	H	H	L	L	BG	BA	L	V	H	CA	
WRAS8		BL8,on the fly	H	H	L	H	H	L	L	BG	BA	H	V	H	CA	
RD	READ	Fixed BL8 or BC4	H	H	L	H	H	L	H	BG	BA	V	V	L	CA	
RDS4		BC4,on the fly	H	H	L	H	H	L	H	BG	BA	L	V	L	CA	
RDS8		BL8,on the fly	H	H	L	H	H	L	H	BG	BA	H	V	L	CA	
RDA	READ with auto precharge	Fixed BL8 or BC4	H	H	L	H	H	L	H	BG	BA	V	V	H	CA	
RDAS4		BC4,on the fly	H	H	L	H	H	L	H	BG	BA	L	V	H	CA	
RDAS8		BL8,on the fly	H	H	L	H	H	L	H	BG	BA	H	V	H	CA	
NOP	No Operation		H	H	L	H	H	H	H	V	V	V	V	V	V	10
DES	Device Deselected		H	H	H	X	X	X	X	X	X	X	X	X	X	
PDE	Power Down Entry		H	L	H	X	X	X	X	X	X	X	X	X	X	6
PDX	Power Down Exit		L	H	H	X	X	X	X	X	X	X	X	X	X	6
ZQCL	ZQ Calibration Long		H	H	L	H	H	H	L	V	V	V	V	H	V	
ZQCS	ZQ Calibration Short		H	H	L	H	H	H	L	V	V	V	V	L	V	

NOTE 1 All DDR4 SDRAM commands are defined by states of $\overline{CS}$, $\overline{ACT}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14 and CKE at the rising edge of the clock. The MSB of BG, BA, RA and CA are device density and configuration dependent. When $\overline{ACT}$ = H; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as command pins $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ respectively. When $\overline{ACT}$= L; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as address pins A16, A15, and A14 respectively.

NOTE 2 $\overline{RESET}$ is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.

NOTE 3 Bank Group addresses (BG) and Bank addresses (BA) determine which bank within a bank group to be operated upon. For MRS commands the BG and BA selects the specific Mode Register location.

NOTE 4 "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".

NOTE 5 Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.

NOTE 6 The Power Down Mode does not perform any refresh operation.

NOTE 7 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

NOTE 8 Controller guarantees self refresh exit to be synchronous.

NOTE 9 VPP and VREF(VrefCA) must be maintained during Self Refresh operation.

NOTE 10 The No Operation command should be used in cases when the DDR4 SDRAM is in Gear Down Mode and Max Power Saving Mode Exit

NOTE 11 Refer to the CKE Truth Table for more detail with CKE transition.

NOTE 12 During a MRS command A17 is Reserved for Future Use and is device density and configuration dependent.

CKE Truth Table

Current State[2]	CKE		Command (N)[3] $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$	Action(N)[3]	Notes
	Previous Cycle[1] (N-1)	Present Cycle[1] (N)			
Power Down	L	L	X	Maintain power down	14, 15
	L	H	DESELECT	Power down exit	11, 14
Self Refresh	L	L	X	Maintain self refresh	15, 16
	L	H	DESELECT	Self refresh exit	8, 12, 16
Bank(s) Active	H	L	DESELECT	Active power down entry	11, 13, 14
Reading	H	L	DESELECT	Power down entry	11, 13, 14, 17
Writing	H	L	DESELECT	Power down entry	11, 13, 14, 17
Precharging	H	L	DESELECT	Power down entry	11, 13, 14, 17
Refreshing	H	L	DESELECT	Precharge power down entry	11
All Banks idle	H	L	DESELECT	Precharge power down entry	11,13, 14, 18
	H	L	REFRESH	Self refresh	9, 13, 18
For more details with all signals See “Command Truth Table”.					10

NOTE 1 CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.

NOTE 2 Current state is defined as the state of the DDR4 SDRAM immediately prior to clock edge N.

NOTE 3 COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.

NOTE 4 All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.

NOTE 6 During any CKE transition (registration of CKE H->L or CKE L->H), the CKE level must be maintained until 1nCK prior to tCKEmin being satisfied (at which time CKE may transition again).

NOTE 7 DESELECT and NOP are defined in the Command Truth Table.

NOTE 8 On Self-Refresh Exit DESELECT commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.

NOTE 9 Self-Refresh mode can only be entered from the All Banks Idle state.

NOTE 10 Must be a legal command as defined in the Command Truth Table.

NOTE 11 Valid commands for Power-Down Entry and Exit are DESELECT only.

NOTE 12 Valid commands for Self-Refresh Exit are DESELECT only except for Gear Down mode and Max Power Saving exit. NOP is allowed for these 2 modes.

NOTE 13 Self-Refresh cannot be entered during Read or Write operations. For a detailed list of restrictions, see “Self-Refresh Operation” and “Power-Down Modes”.

NOTE 14 The Power-Down does not perform any refresh operations.

NOTE 15 “X” means “don’t care “(including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.

NOTE 16 VPP and VREF(VrefCA) must be maintained during Self-Refresh operation.

NOTE 17 If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.

NOTE 18 ‘Idle state’ is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP, etc).

Burst Length, Type, and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in the following: Burst Type and Burst Order table. The burst type is selected via A3 of Mode Register MR0. The burst length is defined by A0-A1 of Mode Register MR0. Burst length options include fixed BC4, fixed BL8, and on-the-fly (OTF), which allows BC4 or BL8 to be selected coincident with the registration of a READ or WRITE command via A12/$\overline{BC}$.

Burst Length	READ/ WRITE	Starting Column Address			Burst Type (Decimal)															Notes
					Sequential								Interleaved							
		A2	A1	A0	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	
BC4	READ	0	0	0	0	1	2	3	T	T	T	T	0	1	2	3	T	T	T	T	1,2,3
		0	0	1	1	2	3	0	T	T	T	T	1	0	3	2	T	T	T	T	1,2,3
		0	1	0	2	3	0	1	T	T	T	T	2	3	0	1	T	T	T	T	1,2,3
		0	1	1	3	0	1	2	T	T	T	T	3	2	1	0	T	T	T	T	1,2,3
		1	0	0	4	5	6	7	T	T	T	T	4	5	6	7	T	T	T	T	1,2,3
		1	0	1	5	6	7	4	T	T	T	T	5	4	7	6	T	T	T	T	1,2,3
		1	1	0	6	7	4	5	T	T	T	T	6	7	4	5	T	T	T	T	1,2,3
		1	1	1	7	4	5	6	T	T	T	T	7	6	5	4	T	T	T	T	1,2,3
	WRITE	0	V	V	0	1	2	3	X	X	X	X	0	1	2	3	X	X	X	X	1,2,4,5
		1	V	V	4	5	6	7	X	X	X	X	4	5	6	7	X	X	X	X	1,2,4,5
BL8	READ	0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	2
		0	0	1	1	2	3	0	5	6	7	4	1	0	3	2	5	4	7	6	2
		0	1	0	2	3	0	1	6	7	4	5	2	3	0	1	6	7	4	5	2
		0	1	1	3	0	1	2	7	4	5	6	3	2	1	0	7	6	5	4	2
		1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	2
		1	0	1	5	6	7	4	1	2	3	0	5	4	7	6	1	0	3	2	2
		1	1	0	6	7	4	5	2	3	0	1	6	7	4	5	2	3	0	1	2
		1	1	1	7	4	5	6	3	0	1	2	7	6	5	4	3	2	1	0	2
	WRITE	V	V	V	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	2,4

NOTE 1 In the case of setting burst length to BC4 (fixed) in MR0, the internal WRITE operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In the case of setting burst length to on-the-fly in MR0, the internal WRITE operation starts at the same point in time as a BL8 (even if BC4 was selected during column time using A12/$\overline{BC}$.). This means that if the on-the-fly MR0 setting is used, the starting point for tWR and tWTR will not be pulled in by two clocks as described in the BC4 (fixed) case.

NOTE 2 Bit number (B0…B7) is the value of column address CA [2:0] that causes this bit to be the first READ during a burst.

NOTE 3 T = Output driver for data and strobes are in High-Z.

NOTE 4 V = Valid logic level (0 or 1), but respective buffer input ignores level on input pins.

NOTE 5 X = "Don't Care."

BL8 Burst order with CRC Enabled

DDR4 SDRAM supports fixed write burst ordering [A2:A1: A0=0:0:0] when write CRC is enabled in BL8 (fixed)

DLL-off Mode and DLL on/off Switching procedure

DLL On/Off Switching Procedure

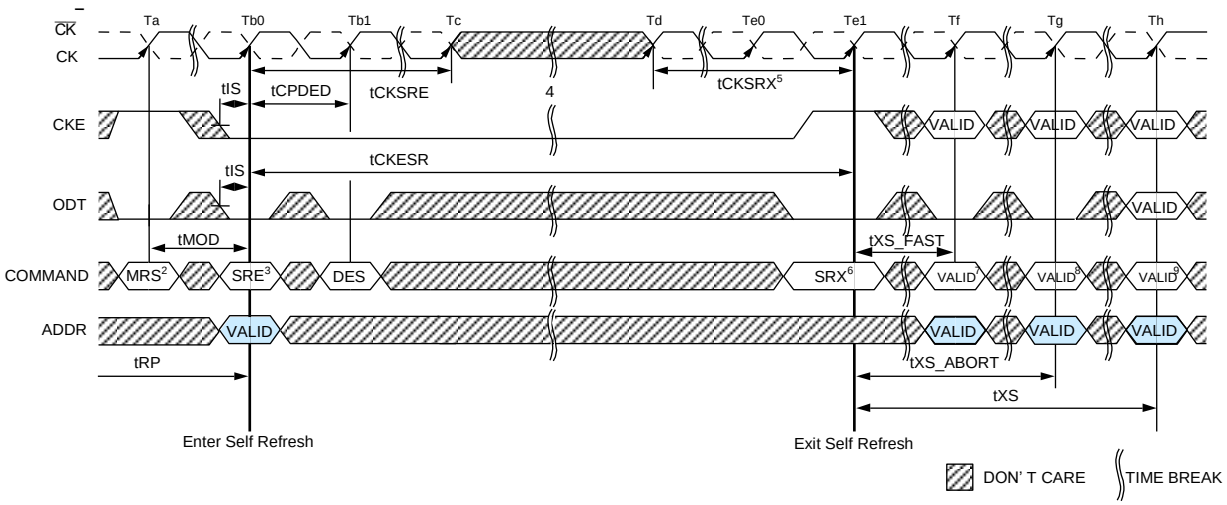
DDR4 DLL-off mode is entered by setting MR1 bit A0 to “0”; this will disable the DLL for subsequent operations until the A0 bit is set back to “1”.

DLL On to DLL Off Procedure

To switch from DLL “on” to DLL “off” requires the frequency to be changed during self refresh, as outlined in the following procedure:

1. Starting from the idle state (all banks pre-charged, all timings fulfilled, and DRAMs on-die termination resistors, RTT_NOM, must be in high impedance state before MRS to MR1 to disable the DLL.)
2. Set MR1 bit A0 to “0” to disable the DLL.
3. Wait tMOD.
4. Enter Self Refresh mode; wait until (tCKSRE) is satisfied.
5. Change frequency, following the guidelines in the “Input Clock Frequency Change” section.
6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
7. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when self refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS command are satisfied. If RTT_NOM was disabled in the mode registers when self refresh mode was entered, the ODT signal is "Don't Care."
8. Wait tXS_FASTor tXS_ABORT or tXS, and then set mode registers with appropriate values (especially an update of CL, CWL, and WR may be necessary; a ZQCL command can also be issued after tXS_FAST).
   - tXS: ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8, RD, RDS4, RDS8, RDA, RDAS4, RDAS8
   - tXS_FAST: ZQCL, ZQCS, MRS commands. For MRS commands, only CL and WR/RTP registers in MR0, the CWL register in MR2, and geardown mode in MR3 are allowed to be accessed provided the device is not in per-device addressability mode. Access to other device mode registers must satisfy tXS timing.
   - tXS_ABORT: If the MR4 bit A9 is enabled, then the DRAM aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command after a delay of tXS_ABORT. Upon exiting from self refresh, the DDR4 SDRAM requires a minimum of one extra REFRESH command before it is put back into self refresh mode. This requirement remains the same irrespective of the setting of the MRS bit for self refresh abort.
9. Wait for tMOD, and then the DRAM is ready for the next command.

DLL Switch Sequence from DLL On to DLL Off



NOTE 1 Starting with idle state. RTT in stable.

NOTE 2 Disable DLL by setting MR1 bit A0 to “0”.

NOTE 3 Enter SR.

NOTE 4 Change frequency.

NOTE 5 Clock must be stable in tCKSRX.

NOTE 6 Exit SR.

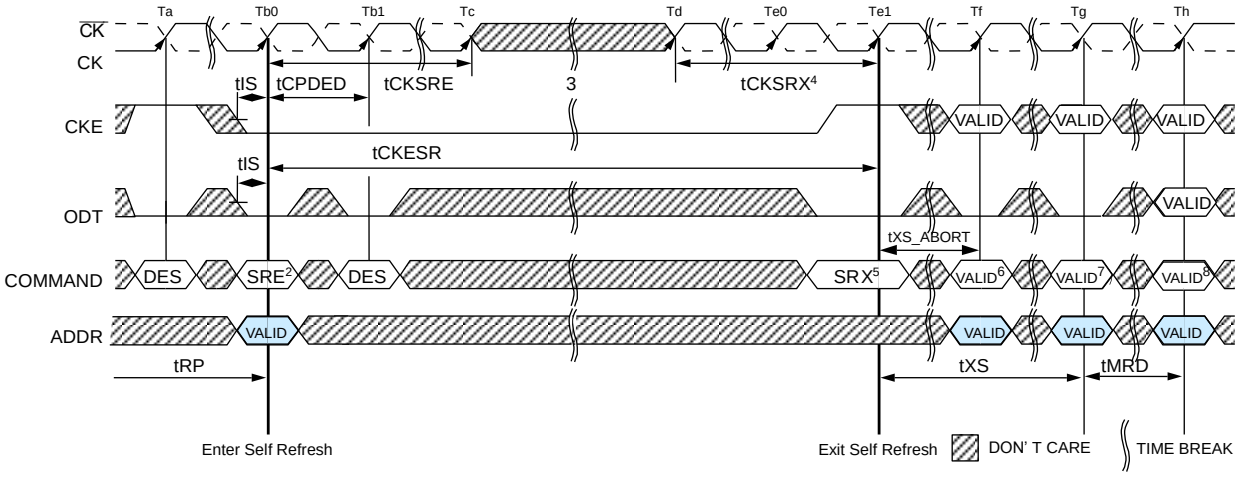
NOTE 7 Update mode registers allowed with DLL_off parameters setting.

DLL Off to DLL On Procedure

To switch from DLL off to DLL on (with required frequency change) during self refresh:

1. Starting from the idle state (all banks pre-charged, all timings fulfilled, and DRAM on-die termination resistors (RTT_NOM) must be in the high impedance state before self refresh mode is entered.)
2. Enter Self Refresh mode; wait until tCKSRE satisfied.
3. Change frequency, following the guidelines in the “Input Clock Frequency Change” section.
4. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
5. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until tDLLK timing from the subsequent DLL RESET command is satisfied. In addition, if any ODT features were enabled in the mode registers when self refresh mode was entered, the ODT signal must continuously be registered LOW until tDLLK timings from the subsequent DLL RESET command is satisfied. If RTT_NOM was disabled in the mode registers when self refresh mode was entered, the ODT signal is "Don't Care."
6. Wait tXS or tXS_ABORT, depending on bit A9 in MR4, then set MR1 bit A0 to “1” to enable the DLL.
7. Wait tMRD, then set MR0 bit A8 to “1” to start DLL Reset.
8. Wait tMRD, then set mode registers with appropriate values (especially an update of CL, CWL, and WR may be necessary. After tMOD is satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after tDLLK.)
9. Wait for tMOD, then DRAM is ready for the next command. (Remember to wait tDLLK after DLL RESET before applying any command requiring a locked DLL.) In addition, wait for tZQoper in case a ZQCL command was issued.

DLL Switch Sequence from DLL Off to DLL On



NOTE 1 Starting with idle state.
NOTE 2 Enter SR.
NOTE 3 Change frequency.
NOTE 4 Clock must be stable tCKSRX.
NOTE 5 Exit SR.
NOTE 6,7 Set DLL on by setting MR1 A0 = “1”.
NOTE 8 Start DLL reset
NOTE 9 Update rest MR register values after tDLLK (not shown in the diagram)
NOTE 10 Ready for valid command after tDLLK (not shown in the diagram)

DLL-Off Mode

DLL-off mode is entered by setting MR1 bit A0 to “0”, this will disable the DLL for subsequent operations until the A0 bit is set back to “1”. The MR1 A0 bit for DLL control can be switched either during initialization or later. Refer to “Input Clock Frequency Change” for more details.

The DLL-off Mode operations listed below are an optional feature for DDR4 SDRAM. The maximum clock frequency for DLL-off mode is specified by the parameter tCKDLL_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

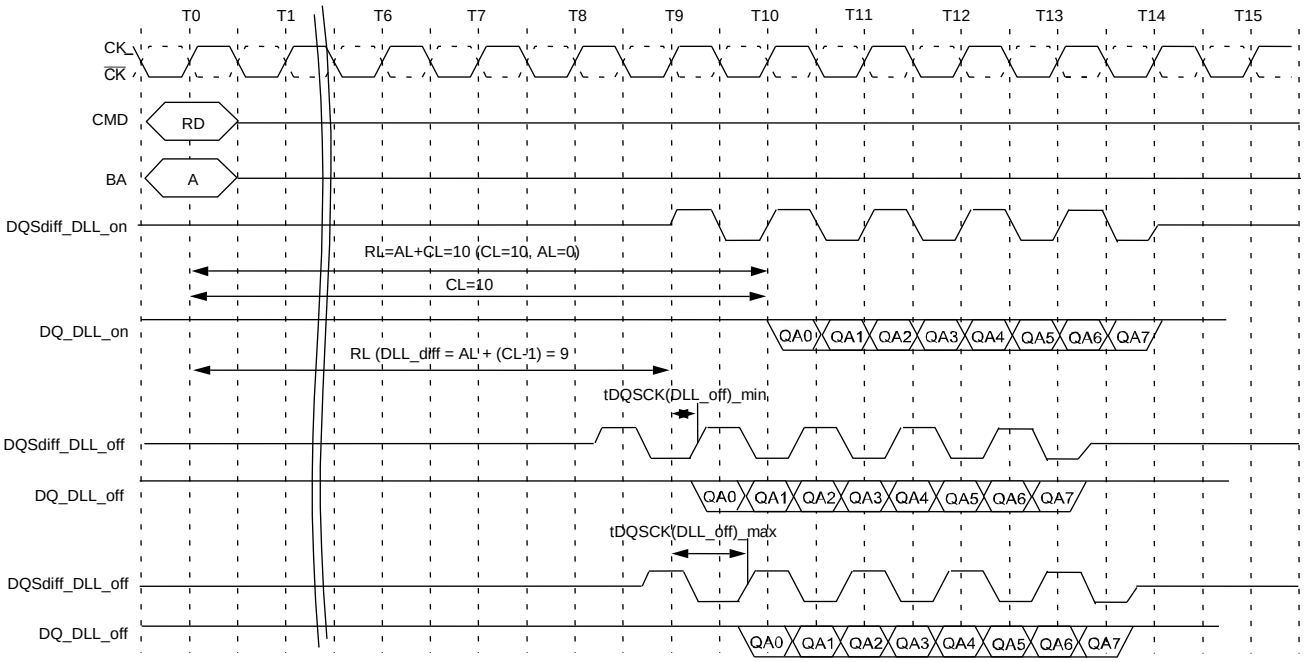
Due to latency counter and timing restrictions, only one CL value in MR0 and CWL in MR2 are supported. The DLL-off mode is only required to support setting both CL = 10 and CWL = 9.

When DLL-off Mode is enabled, use of CA Parity Mode is not allowed. DLL-off mode will affect the read data clock-to-data strobe relationship (tDQSCK), but not the data strobe-to-data relationship (tDQSQ, tQH). Special attention is needed to line up read data to the controller time domain.

Compared with DLL-on mode, where tDQSCK starts from the rising clock edge (AL + CL) cycles after the READ command, the DLL-off mode tDQSCK starts (AL + CL - 1) cycles after the READ command. Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK), and the difference between tDQSCK MIN and tDQSCK MAX is significantly larger than in DLL-on mode. The tDQSCK (DLL_off) values are vendor-specific.

READ operation at DLL-off mode

(CL=10, BL=8, PL=0)



Input Clock Frequency Change

Once the DDR4 SDRAM is initialized, the DDR4 SDRAM requires the clock to be stable during almost all states of normal operation. This means that after the clock frequency has been set and is to be in the “stable state”, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications. The input clock frequency can be changed from one stable clock rate to another stable clock rate under self refresh mode. Outside of self refresh mode, it is illegal to change the clock frequency.

Once the DDR4 SDRAM has been successfully placed in self refresh mode and tCKSRE has been satisfied, the state of the clock becomes a don’t care. Once a “don’t care”, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. When entering and exiting self refresh mode for the sole purpose of changing the clock frequency, the self refresh entry and exit specifications must still be met as outlined in “Self-Refresh Operation”.

For the new clock frequency, additional MRS commands to MR0, MR2, MR3, MR4, MR5, and MR6 may need to be issued to program appropriate CL, CWL, Gear-down mode, Read & Write Preamble, Command Address Latency (CAL Mode), Command Address Parity (CA Parity Mode), and tCCD_L/tDLLK value.

In particular, the Command Address Parity Latency (PL) must be disabled when the clock rate changes, i.e. while in Self Refresh Mode. For example, if changing the clock rate from DDR4-2133 to DDR4-2933 with CA Parity Mode enabled, MR5[2:0] must first change from PL = 4 to PL = disable prior to PL = 6. A correct procedure would be to (1) change PL = 4 to disable via MR5 [2:0], (2) enter Self Refresh Mode, (3) change clock rate from DDR4-2133 to DDR4-2933, (4) exit Self Refresh Mode, (5) Enable CA Parity Mode setting PL = 6 via MR5 [2:0].

If the MR settings that require additional clocks are updated after the clock rate has been increased, i.e. after exiting self refresh mode, the required MR settings must be updated prior to removing the DRAM from the IDLE state, unless the DRAM is RESET. If the DRAM leaves the idle state to enter self refresh mode or ZQ Calibration, the updating of the required MR settings may be deferred to after the next time the DRAM enters the IDLE state.

If MR6 is issued prior to Self Refresh Entry for new tDLLK value, then DLL will relock automatically at Self Refresh Exit. However, if MR6 is issued after Self Refresh Entry, then MR0 must be issued to reset the DLL.

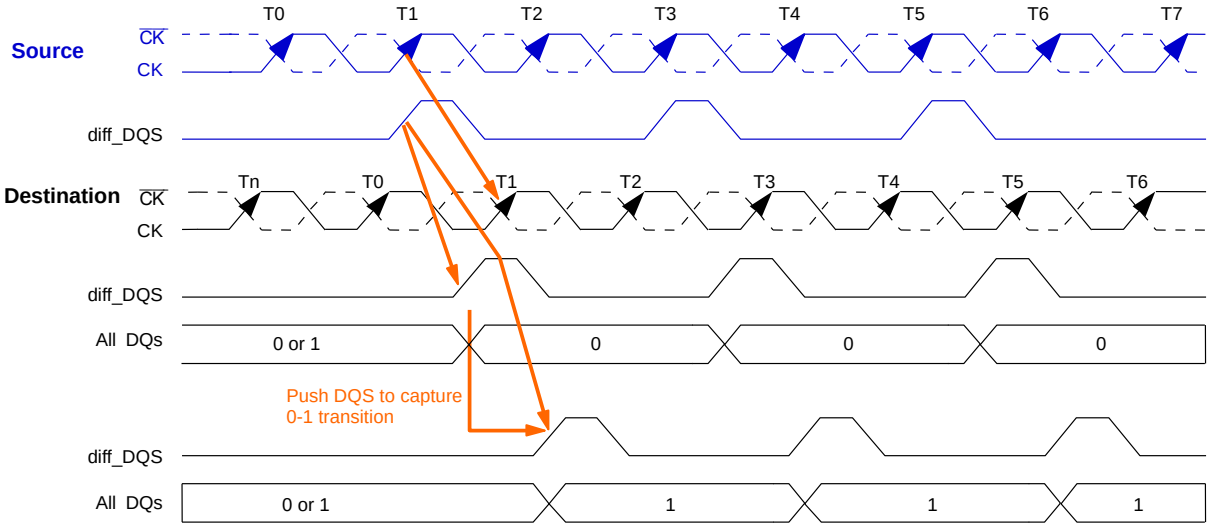
The DDR4 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL_on mode to DLL_off mode transition sequence (see DLL On/Off Switching Procedure).

Write Leveling

For better signal integrity, the DDR4 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR4 SDRAM supports a “write-leveling” feature to allow the controller to compensate for skew. This feature may not be required under some system conditions, provided the host can maintain the tDQSS, tDSS, and tDSH specifications.

The memory controller can use the write leveling feature and feedback from the DDR4 SDRAM to adjust the DQS - $\overline{DQS}$ to CK - $\overline{CK}$ relationship. The memory controller involved in the leveling must have an adjustable delay setting on DQS - $\overline{DQS}$ to align the rising edge of DQS - $\overline{DQS}$ with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK - $\overline{CK}$, sampled with the rising edge of DQS - $\overline{DQS}$, through the DQ bus. The controller repeatedly delays DQS - $\overline{DQS}$ until a transition from 0 to 1 is detected. The DQS - $\overline{DQS}$ delay established through this exercise would ensure tDQSS specification. Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS - $\overline{DQS}$ signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the “AC Timing Parameters” section in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is shown below.

Write-Leveling Concept



DQS - $\overline{DQS}$ driven by the controller during leveling mode must be terminated by the DRAM based on the ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

All data bits carry the leveling feedback to the controller across the DRAM configurations x4, x8, and x16. On a x16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS(diff_UDQS)-to-clock relationship; the lower data bits would indicate the lower diff_DQS(diff_LDQS)-to-clock relationship.

DRAM Setting for Write Leveling and DRAM Termination Function in that Mode

DRAM enters into write leveling mode if A7 in MR1 set “HIGH”, and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 is LOW (see the MR leveling table below). Note that in write leveling mode, only DQS/$\overline{\text{DQS}}$ terminations are activated and deactivated via the ODT pin, unlike normal operation (see DRAM termination table below).

MR Settings for Leveling Procedures

Function	MR1	Enable	Disable
Write Leveling enable	A7	1	0
Data output disable (Qoff)	A12	0	1

DRAM Termination Function in Leveling Mode

ODT Pin at DRAM	DQS/$\overline{\text{DQS}}$ Termination	DQ Termination
RTT_NOM with ODT HIGH	On	Off
RTT_PARK with ODT LOW	On	Off

NOTE 1 In write-leveling mode with its output buffer disabled (MR1[bit A7] = 1 with MR1[bit A12] =1) all RTT_NOM and RTT_PARK settings are allowed; in write-leveling mode with its output buffer enabled (MR1[bitA7] = 1 with MR1[bitA12] = 0) all RTT_NOM and RTT_PARK settings are allowed.

NOTE 2 Dynamic ODT function is not available in Write Leveling Mode. DRAM MR2 bits A [11:9] must be ‘000’ prior to entering Write Leveling Mode.

Procedure Description

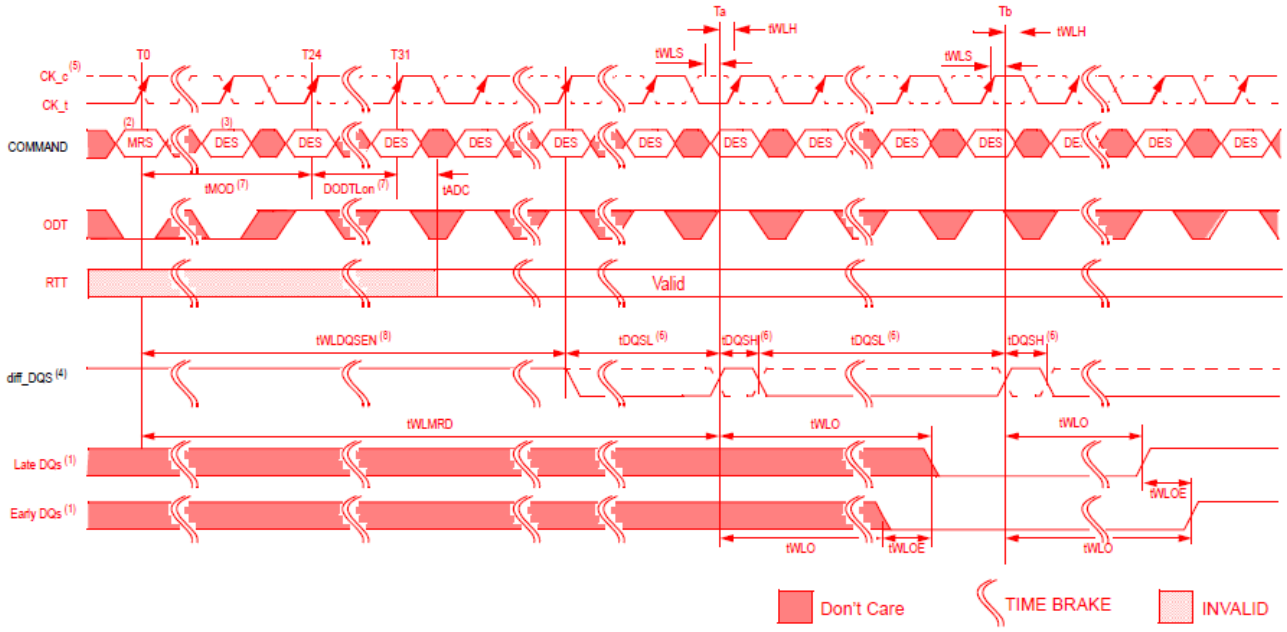
The memory controller initiates the leveling mode of all DRAM by setting bit A7 of MR1 to 1. When entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only the DESELECT commands are allowed, as well as an MRS command to change the Qoff bit (MR1[A12]) and an MRS command to exit write leveling (MR1[A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR1[A7] = 0) may also change MR1 bits of A12-A8, A2-A1. Since the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. The controller may assert ODT after tMOD, at which time the DRAM is ready to accept the ODT signal.

The controller may drive DQS LOW and $\overline{DQS}$ HIGH after a delay of tWLDQSEN, at which time the DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD, the controller provides a single DQS, $\overline{DQS}$ edge which is used by the DRAM to sample CK - $\overline{CK}$ driven from the controller. tWLMRD(max) timing is controller dependent.

DRAM samples CK - $\overline{CK}$ status with the rising edge of DQS - $\overline{DQS}$ and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits. The tWLOE period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS, $\overline{DQS}$) needed for these DQs. Controller samples incoming DQ and decides to increment or decrement DQS - $\overline{DQS}$ delay setting and launches the next DQS - $\overline{DQS}$ pulse after some time, which is controller dependent. After a 0-to-1 transition is detected, the controller locks the DQS - $\overline{DQS}$ delay setting, and write leveling is achieved for the device. The following figure shows the timing diagram and parameters for the overall write leveling procedure.

Parameter	Symbol	DDR4-1600, 1866, 2133, 2400		DDR4-2666		Units	NOTE
		Min	Max	Min	Max		
Write Leveling Output Error	tWLOE	0	2	0	2	ns	

Timing details of Write leveling sequence (DQS-$\overline{DQS}$ is capturing CK - $\overline{CK}$ low at Ta and CK - $\overline{CK}$ high at Tb)



NOTE 1 DDR4 SDRAM drives leveling feedback on all DQs

NOTE 2 MRS : Load MR1 to enter write leveling mode

NOTE 3 DES : Deselect

NOTE 4 diff_DQS is the differential data strobe (DQS-$\overline{DQS}$). Timing reference points are the zero crossings. DQS is shown with solid line, $\overline{DQS}$ is shown with dotted line

NOTE 5 CK/$\overline{CK}$: CK is shown with solid dark line, whereas $\overline{CK}$ is drawn with dotted line.

NOTE 6 DQS , $\overline{DQS}$ needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent

NOTE 7 tMOD(Min) = max(24nCK, 15ns), WL = 9 (CWL = 9, AL = 0, PL = 0), DODTLon = WL -2 = 7

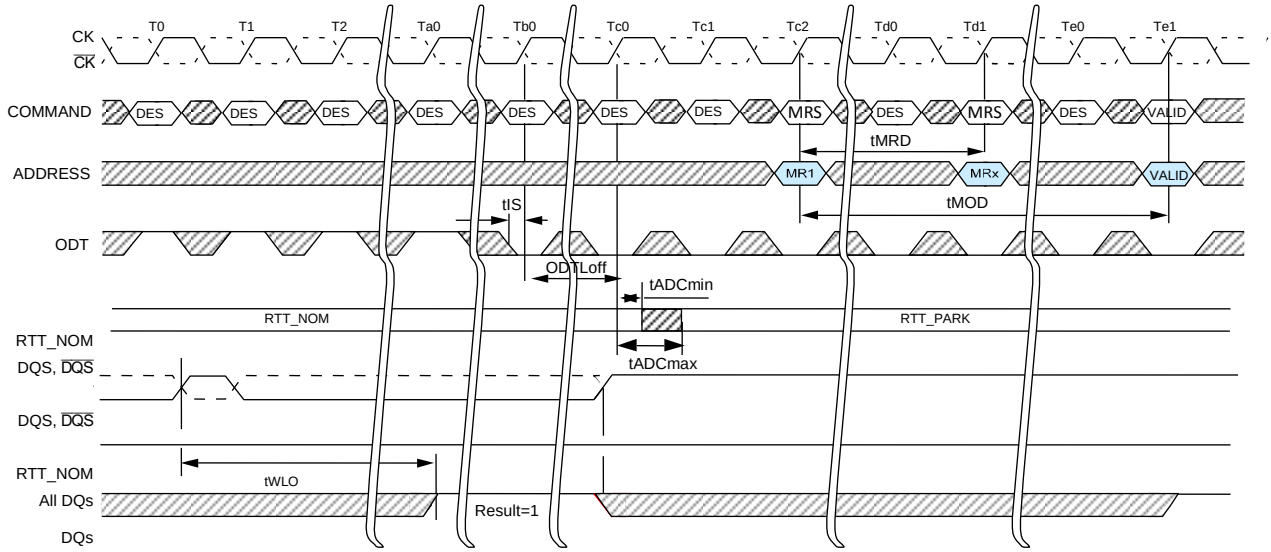
NOTE 8 tWLDQSEN must be satisfied following equation when using ODT.
tWLDQSEN > tMOD(Min) + ODTLon + tADC : at DLL = Enable
tWLDQSEN > tMOD(Min) + tAONAS : at DLL = Disable

Write-Leveling Mode Exit

Write leveling mode should be exited as follows:

1. After the last rising strobe edge (see T0), stop driving the strobe signals (see Tc0). Note that from this point now on, DQ pins are in undefined driving mode and will remain undefined, until tMOD after the respective MRS command (Te1).
2. Drive ODT pin LOW (tIS must be satisfied) and continue registering LOW (see Tb0).
3. After the RTT is switched off, disable write-leveling mode via the MRS command (see Tc2).
4. After tMOD is satisfied (Te1), any valid command can be registered. MR commands can be issued after tMRD (Td1).

Timing details of Write leveling exit



Temperature-Controlled Refresh Modes (TCR)

This mode is enabled and disabled by setting bit A3 in MR4. Two modes are supported that are selected by bit A2 setting in MR4.

Temperature range

Grade	Normal Temperature Mode	Extended Temperature Mode
Commercial grade (0°C ~ 95°C)	0<Tc ≤ 85°C	0<Tc ≤ 95°C
Industrial grade(-40°C ~ 95°C)	-40<Tc ≤ 85°C	-40°C <Tc ≤ 95°C
Quasi-industrial grade(-40°C ~ 95°C)	-40<Tc ≤ 85°C	-40°C <Tc ≤ 95°C

Normal temperature mode

Once this mode is enabled by setting bit A3=1 and A2=0 in MR4, Refresh commands should be issued to DDR4 SDRAM with the average periodic refresh interval (7.8us for 2Gb, 4Gb, 8Gb, and 16Gb device) which is tREFI of normal temperature range. In this mode, the system guarantees that the DRAM temperature does not exceed 85°C.

Below 45°C, DDR4 SDRAM may adjust internal average periodic refresh interval by skipping external refresh commands with proper gear ratio. Not more than three fourths of external refresh commands are skipped at any temperature in this mode.

The internal average periodic refresh interval adjustment is automatically done inside the DRAM and user does not need to provide any additional control.

Extended temperature mode

Once this mode is enabled by setting bit A3=1 and A2=1 in MR4, Refresh commands should be issued to DDR4 SDRAM with the average periodic refresh interval (3.9us for 2Gb, 4Gb, 8Gb, and 16Gb device) which is tREFI of extended temperature range. In this mode, the system guarantees that the DRAM temperature does not exceed extended temperature range.

In the normal temperature range, DDR4 SDRAM adjusts its internal average periodic refresh interval to tREFI of the normal temperature range by skipping external refresh commands with proper gear ratio. Below 45°C, DDR4 SDRAM may further adjust internal average periodic refresh interval. Not more than seven eighths of external commands are skipped at any temperature in this mode. The internal average periodic refresh interval adjustment is automatically done inside the DRAM and user does not need to provide any additional control.

Normal tREFI Refresh (TCR Disabled)

Temperature	Normal Temperature		Extended Temperature	
	External Refresh Period	Internal Refresh Period	External Refresh Period	Internal Refresh Period
Tc <45°C	7.8µs	7.8µs	3.9µs(1)	3.9µs(1)
45≤Tc ≤85°C				
85<Tc ≤ 95°C	(Not Applicable)			

NOTE 1 If T_C is less than 85°C then the external refresh period can be 7.8µs instead of 3.9us.

Normal tREFI Refresh (TCR Enabled)

Temperature	Normal Temperature		Extended Temperature	
	External Refresh Period	Internal Refresh Period	External Refresh Period	Internal Refresh Period
Tc <45°C	7.8µs	>> 7.8µs	3.9µs(1)	>> 7.8µs
45≤Tc ≤85°C		7.8µs		7.8µs
85<Tc ≤ 95°C	(Not Applicable)			3.9µs

NOTE 1 If the external refresh period is 7.8µs then DRAM will refresh internally at half the listed refresh rate and will violate refresh specifications.

Fine Granularity Refresh Mode (FGRM)

Mode Register and Command Truth Table

The REFRESH cycle time (tRFC) and the Average Refresh Interval (tREFI) of DDR4 SDRAM can be programmed by the MRS command. The appropriate setting in the mode register will set a single set of REFRESH cycle time and average refresh interval for the DDR4 SDRAM device (fixed mode), or allow the dynamic selection of one of two sets of REFRESH cycle time and average refresh interval for the DDR4 SDRAM device (on-the-fly mode, OTF). OTF mode must be enabled by MRS before any OTF REFRESH command can be issued.

MR3 definition for Fine Granularity Refresh Mode

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal mode (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Enable on the fly 1x/2x
1	1	0	Enable on the fly 1x/4x
1	1	1	Reserved

There are two types of OTF modes (1x/2x and 1x/4x modes) that are selectable by programming the appropriate values into the mode register. When either of the two OTF modes is selected ('A8=1'), DDR4 SDRAM evaluates the BG0 bit when a REFRESH command is issued, and depending on the status of BG0, it dynamically switches its internal refresh configuration between 1x/2x or 1x/4x modes, then executes the corresponding REFRESH operation.

REFRESH Command Truth Table (OTF modes)

REFRESH	CS	$\overline{ACT}$	$\overline{RAS}$ /A16	$\overline{CAS}$ /A15	$\overline{WE}$ /A14	BG1	BG0	BA0-1	A10/ AP	A[9:0], A[12:11], A17	MR3 A[8:6]
Fixed rate	L	H	L	L	H	V	**V**	V	V	V	**0vv**
OTF – 1x	L	H	L	L	H	V	**L**	V	V	V	**1vv**
OTF – 2x	L	H	L	L	H	V	**H**	V	V	V	**101**
OTF – 4x											**110**

tREFI and tRFC Parameters

The default refresh rate mode is fixed 1x mode where REFRESH commands should be issued with the normal rate, i.e. tREFI1 = tREFI(base) (for TCASE ≤ 85°C), and the duration of each REFRESH command is the normal refresh cycle time (tRFC1). In 2x mode (either fixed 2x or OTF 2x mode), REFRESH commands should be issued to the DRAM at the double frequency (tREFI2 = tREFI(base)/2) of the normal refresh rate. In 4x mode, REFRESH command rate should be quadrupled (tREFI4 = tREFI(base)/4). Per each mode and command type, tRFC parameter has different values as defined in the following table.

The REFRESH command that should be issued at the normal refresh rate and has the normal refresh cycle duration may be referred to as a REF1x command. The refresh command that should be issued at the double frequency (tREFI2 = tREFI(base)/2) may be referred to as a REF2x command. Finally, the REFRESH command that should be issued at the quadruple rate (tREFI4 = tREFI(base)/4) may be referred to as a REF4x command.

In the fixed 1x refresh rate mode, only REF1x commands are permitted. In the fixed 2x refresh rate mode, only REF2x commands are permitted. In the fixed 4x refresh rate mode, only REF4x commands are permitted. When the on-the-fly 1x/2x refresh rate mode is enabled, both REF1x and REF2x commands are permitted. When the OTF 1x/4x refresh rate mode is enabled, both REF1x and REF4x commands are permitted.

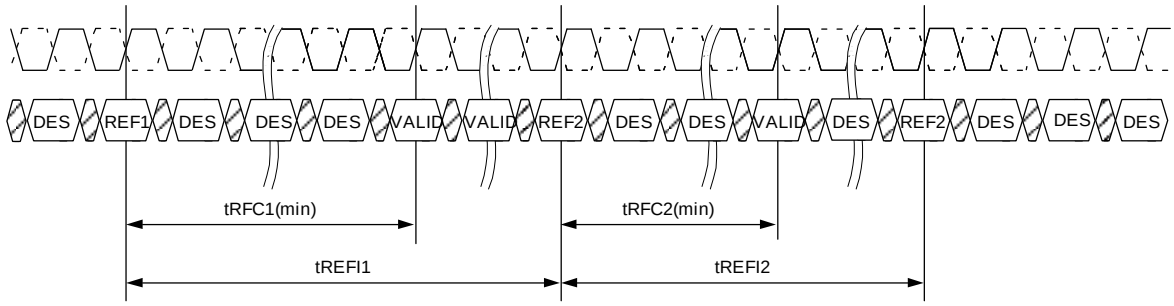
tREFI and tRFC Parameters

Refresh Mode	Parameter		4Gb	Unit
	tREFI (base)		**7.8**	µs
1X mode	**tREFI1**	TCASE ≤ 85°C	**tREFI(base)**	µs
		TCASE ≤ 95°C	**tREFI(base)/2**	µs
	tRFC1 (min)		**260**	ns
2X mode	**tREFI2**	TCASE ≤ 85°C	**tREFI(base)/2**	µs
		85°C < TCASE ≤ 95°C	**tREFI(base)/4**	µs
	tRFC2 (min)		**160**	ns
4X mode	**tREFI4**	TCASE ≤ 85°C	**tREFI(base)/4**	µs
		85°C < TCASE ≤ 95°C	**tREFI(base)/8**	µs
	tRFC4 (min)		**110**	ns

Changing Refresh Rate

If the refresh rate is changed by either MRS or OTF, new tREFI and tRFC parameters will be applied from the moment of the rate change. When the REF1x command is issued to the DRAM, then tREF1 and tRFC1 are applied from the time that the command was issued. And then, when REF2x command is issued, then tREF2 and tRFC2 should be satisfied. As shown in below.

On-the-fly REFRESH Command Timing



The following conditions must be satisfied before the refresh rate can be changed. Otherwise, data retention of DDR4 SDRAM cannot be guaranteed.

- In the fixed 2x refresh rate mode or the OTF 1x/2x refresh mode, an even number of REF2x commands must be issued to the DDR4 SDRAM since the last change of the refresh rate mode with an MRS command before the refresh rate can be changed by another MRS command.
- In the OTF1x/2x refresh rate mode, an even number of REF2x commands must be issued between any two REF1x commands.
- In the fixed 4x refresh rate mode or the OTF 1x/4x refresh mode, a multiple-of-four number of REF4x commands must be issued to the DDR4 SDRAM since the last change of the refresh rate with an MRS command before the refresh rate can be changed by another MRS command.
- In the OTF1x/4x refresh rate mode, a multiple-of-four number of REF4x commands must be issued between any two REF1x commands.

There are no special restrictions for the fixed 1x refresh rate mode. Switching between fixed and OTF modes keeping the same rate is not regarded as a refresh rate change.

Usage with Temperature Controlled Refresh Mode

If the temperature controlled refresh mode is enabled, then only the normal mode (fixed 1x mode, MR3 A[8:6] = 000) is allowed. If any other refresh mode than the normal mode is selected, then the temperature controlled refresh mode must be disabled.

Self Refresh Entry and Exit

DDR4 SDRAM can enter self refresh mode anytime in 1x, 2x, and 4x mode without any restriction on the number of REFRESH commands that have been issued during the mode before the self refresh entry. However, upon self refresh exit, extra REFRESH command(s) may be required, depending on the condition of the self refresh entry.

The conditions and requirements for the extra REFRESH command(s) are defined as follows:

- There are no special restrictions on the fixed 1x refresh rate mode.
- In the fixed 2x refresh rate mode or the enable-OTF 1x/2x refresh rate mode, it is recommended that there should be an even number of REF2x commands before entry into self refresh because the last SELF REFRESH EXIT or REF1x command or MRS command that set the refresh mode. If this condition is met, no additional refresh commands are required upon self refresh exit. In the case that this condition is not met, either one extra REF1x command or two extra REF2x commands are required to be issued to the DDR4 SDRAM upon self refresh exit. These extra REFRESH commands are not counted toward the computation of the average refresh interval (tREFI).
- In the fixed 4x refresh rate mode or the enable-OTF 1x/4x refresh rate mode, it is recommended that there should be a multiple-of-four number of REF4x commands before entry into self refresh since the last self refresh exit or REF1x command or MRS command that set the refresh mode. If this condition is met, no additional refresh commands are required upon self refresh exit. In the case that this condition is not met, either one extra REF1x command or four extra REF4x commands are required to be issued to the DDR4 SDRAM upon self refresh exit. These extra REFRESH commands are not counted toward the computation of the average refresh interval (tREFI).

Multipurpose Register (MPR)

he multipurpose register (MPR) function, MPR Access Mode, is used to write/read specialized data to/from the DRAM. The MPR consists of four logical Pages, MPR Page 0 through MPR Page 3, with each Page having four 8-bit registers, MPR0 through MPR3.

MPR mode enable and Page selection is done with MRS commands. Data Bus Inversion (DBI) is not allowed during MPR Read operation. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). After MPR is enabled, any subsequent RD or RDA commands will be redirected to a specific mode register.

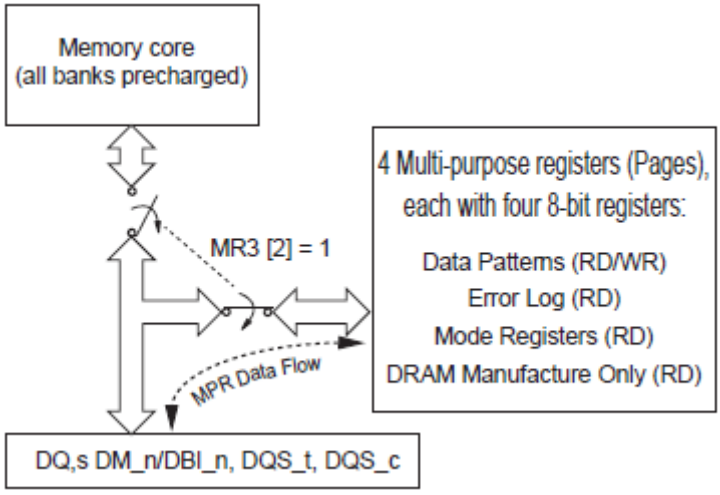
Once the MPR Access Mode is enabled (MR3 A [2] = 1), only the following commands are allowed: MRS, RD, RDA WR, WRA, DES, REF and Reset; RDA/WRA have the same functionality as RD/WR which means the auto precharge part of RDA/WRA is ignored. The mode register location is specified with the READ command using address bits. The MR is split into upper and lower halves to align with a burst length limitation of 8. Power Down mode and Self-Refresh command are not allowed during MPR enable Mode.

No other command can be issued within tRFC after a REF command has been issued. 1x Refresh is only allowed when MPR mode is Enable. While in MPR Access Mode, MPR read or write sequences must be completed prior to a refresh command.

MPR Enable

Allow	Not Allow
1. MPR Read with BL8 or BC4 (A [2:0] = 000 or 100) 2. MRS, RD, RDA WR, WRA, DESELECT, REFRESH and Reset	1. BL OTF 2. Data Bus Inversion (DBI) 3. Power Down mode and Self-Refresh

MPR Block Diagram



MR3 definition

MPR Read Format	MPR Operation	MPR Page Selection	MPR Location
MR3[12:11]	MR3[2]	MR3[1:0]	MPR BA[1:0]

MR3		MPR Read Format
A12	A11	
0	0	Serial
0	1	Parallel
1	0	Staggered
1	1	RFU

MR3	MPR Operation
A2	
0	Normal Operation
1	Data flow from/to MPR

MR3		MPR Page Selection
A1	A0	
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

MPR		MPR Location
BA1	BA0	
0	0	MPR0
0	1	MPR1
1	0	MPR2
1	1	MPR3

MPR pages

After power-up, the content of MPR page 0 has the default values, defined in the MPR Data Format table. MPR page 0 can be rewritten via an MPR WRITE command. The DRAM maintains the default values unless it is re-written by the DRAM controller. If DRAM's controller does overwrite the default values (Page 0 only), the device will maintain the new values unless re-initialized or power loss. Refer to "MRP data format "table in previous section for MPR Page setting.

MPR	Page 0	Page 1	Page 2	Page 3
Definition	**WRITE** and **READ** system patterns used for data bus calibration	**Readout** of the error frame when the C/A parity is enabled	**Readout** of the contents of the MRn registers	RFU
Can be used for	• DRAM controller receiver training. • DRAM controller DQS to DQ phase training.	• Clock to address phase training. • RAS (reliability, accessibility and serviceability) Support: Logging of C/A parity and CRC error information	• Mode Register Confirmation.	N/A.
Readout format	serial, parallel, or staggered	serial	serial	serial

Default value for MPR0 @ Page0 = 01010101
Default value for MPR1 @ Page0 = 00110011
Default value for MPR2 @ Page0 = 00001111
Default value for MPR3 @ Page0 = 00000000

DRAM Address to MPR UI 8-bit Registers Translation

MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
DRAM Address	A7	A6	A5	A4	A3	A2	A1	A0
MPR UI	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7

Bit Number of MPR Definition

128 bits	=	**MPR Page** (Page0 to Page3) (MR3 A[1:0])	×	**MPR Location** (MPR0 to MPR3) (MPR BA[1:0])	×	**Address Bit** MPR burst bit (BL8)

MPR Readout Serial Format

Serial format implies that the same pattern is returned on all DQ lanes.

MPR Readout Parallel Format

Parallel format implies that the MPR data is returned in the first data UI and then repeated in the remaining UIs of the burst as shown in the MPR Readout Parallel Format table. Data pattern location 0 is the only location used for the parallel format. RD/RDA from data pattern locations 1, 2, and 3 are not allowed with parallel data return mode.

Example: The pattern programmed in the data pattern location 0 is 0111 1111. The x4 configuration only outputs the first four bits (0111 in this example). For the x16 configuration, the same pattern is repeated on both the upper and lower bytes.

Serial

X4 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1

X8 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1

X16 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1
DQ8	0	1	1	1	1	1	1	1
DQ9	0	1	1	1	1	1	1	1
DQ10	0	1	1	1	1	1	1	1
DQ11	0	1	1	1	1	1	1	1
DQ12	0	1	1	1	1	1	1	1
DQ13	0	1	1	1	1	1	1	1
DQ14	0	1	1	1	1	1	1	1
DQ15	0	1	1	1	1	1	1	1

Parallel

X4 Device

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1

X8 Device

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1

X16 Device

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1
DQ8	0	0	0	0	0	0	0	0
DQ9	1	1	1	1	1	1	1	1
DQ10	1	1	1	1	1	1	1	1
DQ11	1	1	1	1	1	1	1	1
DQ12	1	1	1	1	1	1	1	1
DQ13	1	1	1	1	1	1	1	1
DQ14	1	1	1	1	1	1	1	1
DQ15	1	1	1	1	1	1	1	1

MPR Readout Staggered Format

The third mode of data return is the staggering of the MPR data across the lanes. In this mode, a read command is issued to a specific MPR and then the data is returned on the DQ from different MPR registers. Read from MPR page1, MPR page2, and MPR page3 are not allowed with staggered data return mode.

For a x4 device, a read command to MPR0will result in data from MPR0 being driven on DQ0, data from MPR1 drived on DQ1, data from MPR2 drived on DQ2, data from MPR3 drived on DQ3.

Issuing a read command to MPR1 will result in data from MPR1 being driven on DQ0, data from MPR2 on DQ1 and so forth. Reads from MPR2 and MPR3 are also shown below. as shown below.

MPR Readout Staggered Format, x4

Read MPR0 command (BA[1:0]='00')		Read MPR1 command (BA[1:0]='01')		Read MPR2 command (BA[1:0]='10')		Read MPR3 command (BA[1:0]='11')	
Stagger	UI0-7	Stagger	UI0-7	Stagger	UI0-7	Stagger	UI0-7
DQ0	MPR0	DQ0	MPR1	DQ0	MPR2	DQ0	MPR3
DQ1	MPR1	DQ1	MPR2	DQ1	MPR3	DQ1	MPR0
DQ2	MPR2	DQ2	MPR3	DQ2	MPR0	DQ2	MPR1
DQ3	MPR3	DQ3	MPR0	DQ3	MPR1	DQ3	MPR2

It is expected that the DRAM can respond to back to back RD/RDA commands to the MPR for all DDR4 frequencies so that a stream as follows can be created on the data bus with no bubbles or clocks between read data. In this case system memory controller issues a consecutive sequence command of RD(MPR0), RD(MPR1), RD(MPR2), RD(MPR3), RD(MPR0), RD(MPR1), RD(MPR2), and RD(MPR3).

MPR Readout Staggered Format, x4 – Consecutive READs

Stagger	UI0-7	UI 8-15	UI 16-23	UI 24-31	UI 32-39	UI 40-47	UI 48-55	UI 56-63
DQ0	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3
DQ1	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0
DQ2	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1
DQ3	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2

For the x8 configuration, the same pattern is repeated on the lower nibble as on the upper nibble. READs to other MPR data pattern locations follow the same format as the x4 case.

MPR Readout Staggered Format, x8 and x16

X8		X16			
Stagger	UI0-7	Stagger	UI0-7	Stagger	UI0-7
DQ0	MPR0	DQ0	MPR0	DQ8	MPR0
DQ1	MPR1	DQ1	MPR1	DQ9	MPR1
DQ2	MPR2	DQ2	MPR2	DQ10	MPR2
DQ3	MPR3	DQ3	MPR3	DQ11	MPR3
DQ4	MPR0	DQ4	MPR0	DQ12	MPR0
DQ5	MPR1	DQ5	MPR1	DQ13	MPR1
DQ6	MPR2	DQ6	MPR2	DQ14	MPR2
DQ7	MPR3	DQ7	MPR3	DQ15	MPR3

MPR Reads

MPR reads are supported using BL8 and BC4(Fixed) modes. BC4 on the fly is not supported for MPR reads.

The DRAM is required to drive associated strobes with the read data similar to normal operation (such as using MRS preamble settings). Timing in MPR Mode should follow below rules:

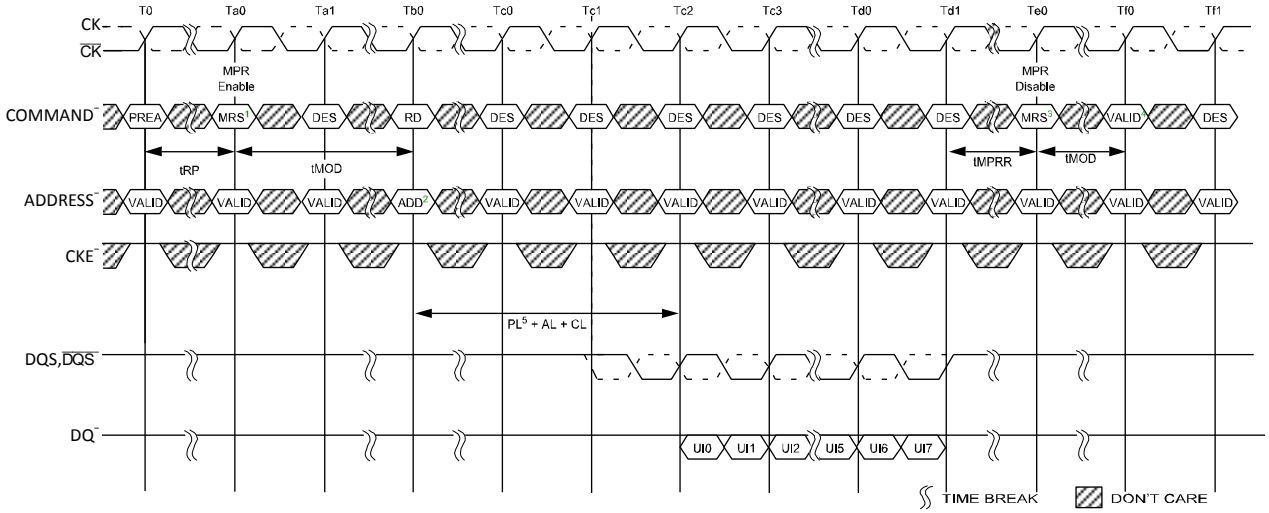
- Reads (back-to-back) from Page 0 may use tCCD_S timing between read commands.
- Reads (back-to-back) from Pages 1, 2, or 3 may not use tCCD_S timing between read commands; tCCD_L must be used for timing between read commands.

The following steps are required to use the MPR to read out the contents of a mode register (MPR Page, MPR location).

1. The DLL must be locked prior to MPR Reads.
2. Precharge all; wait until tRP is satisfied.
3. MRS command to MR3 A [2] = 1 (Enable MPR data flow), MR3 A [12:11] = MPR Read Format, MR3[1:0] = MPR Page.
   a. MR3 A [12:11] MPR Read Format:
      00 = Serial read format
      01 = Parallel read format
      10 = staggered read format
      11 = RFU
   b. MR3 A [1:0] MPR Page:
      00 = MPR Page 0
      01 = MPR Page 1
      10 = MPR Page 2
      11 = MPR Page 3
4. tMRD and tMOD must be satisfied.
5. Redirect all subsequent READ commands to specific MPR location.
6. Issue RD or RDA command:
   a. BA1 and BA0 indicate MPR location:
      00 = MPR0
      01 = MPR1
      10 = MPR2
      11 = MPR3
   b. A12/BC = 0 or 1; BL8 or BC4 Fixed only, BC4 OTF not supported.
      If BL=8 and MR0 A [1:0] = 01, A12/BC must be set to 1 during MPR Read commands.
   c. A [2] = burst type dependent:
      BL8: A [2] = 0 with burst order fixed at 0, 1, 2, 3, 4, 5, 6, 7
      BL8: A [2] = 1 Not support
      BC4: A [2] = 0 with burst order fixed at 0, 1, 2, 3, T, T, T, T
      BC4: A [2] = 1 with burst order fixed at 4, 5, 6, 7, T, T, T, T
   d. A [1:0] = 00, data burst order is fixed starting at nibble, always 00 here.
   e. Remaining address inputs, including A10, and BG1 and BG0 are don't care.
7. After RL = AL + CL, DRAM bursts data from MPR location; Readout format determined by MR3 A [12,11,1,0].
8. Steps 5 through 7 may be repeated until read data capture at memory controller is optimized. Read MPR location can be a different location as specified by the Read command
9. After the last MPR location Read burst, tMPRR must be satisfied prior to exiting.
10. Issue MRS command to exit MPR mode; MR A [2] = 0.
11. Wait tMOD. DRAM is ready for normal operation from the core such as ACT.

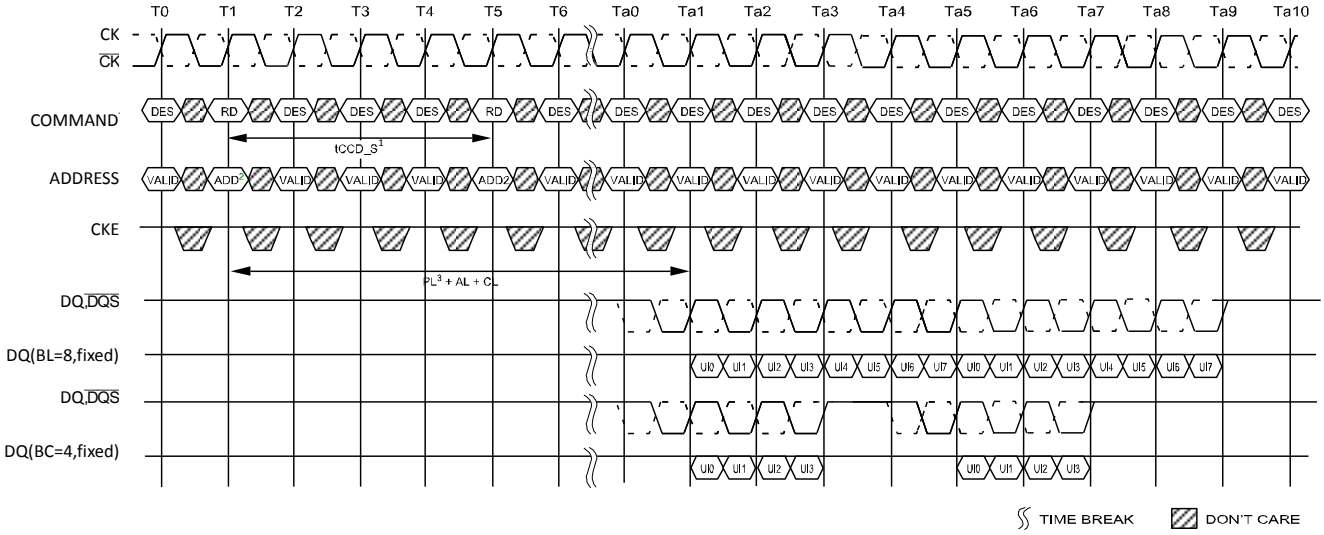
MPR READ Timing

(BL = 8, PL=0, AL = 0, CL = 11, CAL = 3, Preamble = 1tCK)



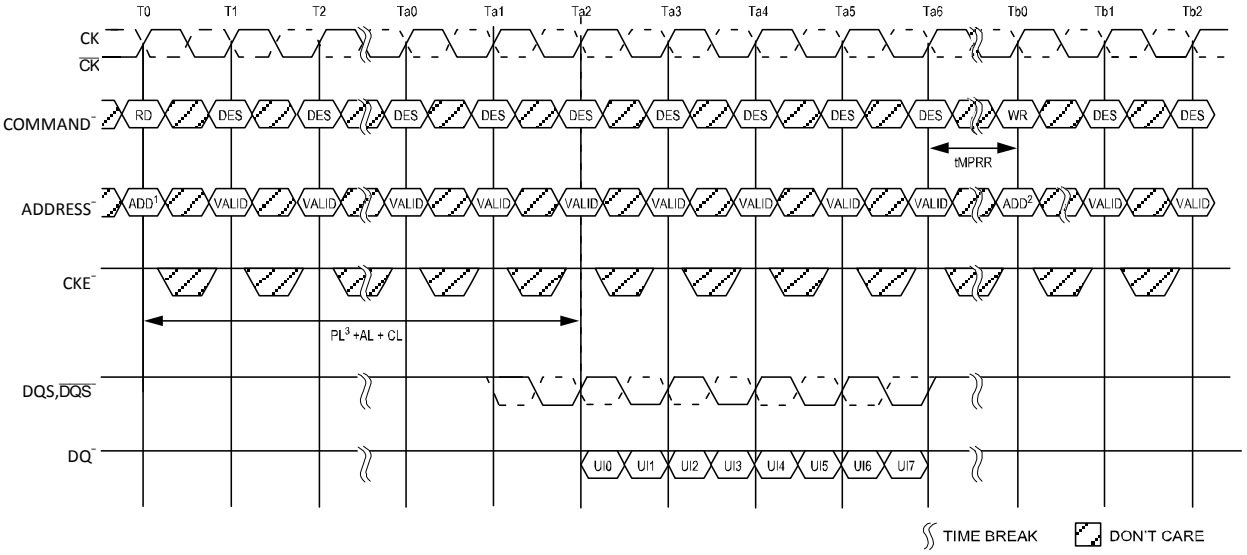
NOTE 1 Multipurpose registers Read/Write Enable (MR3 A2 = 1). Redirect all subsequent reads and writes to MPR locations.
NOTE 2 Address setting:
A[1:0] = "00" (data burst order is fixed starting at nibble, always 00b here)
A[2]= 0 (For BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7)
BA1 and BA0 indicate the MPR location
A10 and other address pins are "Don't Care" including BG1 and BG0.
A12 is don't care when MR0 A[1:0] = 00 or 10, and must be "1" when MR0 A[1:0] = 01
NOTE 3 Multipurpose registers Read/Write Disable (MR3 A2 = 0).
NOTE 4 Continue with regular DRAM command.
NOTE 5 Parity latency (PL) is added to data output delay when C/A parity latency mode is enabled.

MPR Back-to-Back READ Timing



NOTE 1 tCCD_S = 4, Read Preamble = 1tCK
NOTE 2 Address setting:
A[1:0] = 00 (data burst order is fixed starting at nibble, always 00b here)
A[2] = 0 (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7; for BC = 4, burst order is fixed at 0, 1, 2, 3, T, T, T, T)
BA1 and BA0 indicate the MPR location
A10 and other address pins are "Don't Care" including BG1 and BG0.
A12 is "Don't Care" when MR0 A[1:0] = 00 or 10, and must be "1" when MR0 A[1:0] = 01
NOTE 3 Parity latency (PL) is added to data output delay when C/A parity latency mode is enabled.

MPR READ-to-WRITE Timing



NOTE 1 Address setting:
A[1:0] = 00 (data burst order is fixed starting at nibble, always 00 here)
A[2]= 0 (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7)
BA1 and BA0 indicate the MPR location
A10 and other address pins are "Don't Care" including BG1 and BG0.
A12 is "Don't Care" when MR0 A[1:0] = 00, and must be 1b when MR0 A[1:0] = 01

NOTE 2 Address setting:
BA1 and BA0 indicate the MPR location
A [7:0] = data for MPR
A10 and other address pins are don't care.

NOTE 3 Parity latency (PL) is added to data output delay when C/A parity latency mode is enabled.

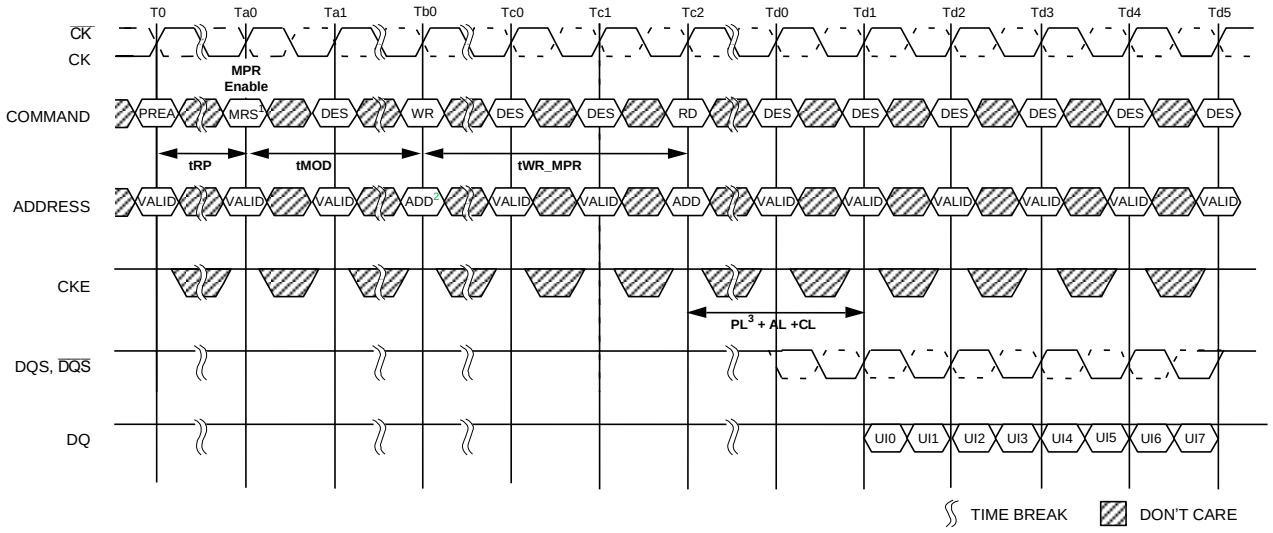
MPR Writes

MPR Access Mode allows 8-bit writes to the MPR location using the address bus A7:A0(refer to table: DRAM Address to MPR UI 8-bit Registers Translation)

The following steps are required to use the MPR to write to mode register MPR Page 0.

1. The DLL must be locked prior to MPR Writes. DLL is Enabled, MR1 A0 = 1
2. Precharge all; wait until tRP is satisfied.
3. MR3 A2 = 1 (Enable MPR data flow) and MR3 A[1:0] = 00 (MPR Page 0); 01, 10, 11 = Not allowed.
4. Redirect all subsequent Write commands to specific MPR location.
5. tMRD and tMOD must be satisfied.
6. Issue WR or WRA command:
   a. BA1 and BA0 indicate MPR location:
      00 = MPR0
      01 = MPR1
      10 = MPR2
      11 = MPR3
   b. A [7:0] = data for MPR Page 0, mapped A [7:0] to UI [0:7].
   c. Remaining address inputs, including A10, BG0 and BG1 are don't care.
7. tWR_MPR must be satisfied to complete MPR Write.
8. Steps 5 through 7 may be repeated these calibration writes and reads until data capture at memory controller is optimized.
9. After the last MPR location Write, tMPRR must be satisfied prior to exiting.
10. Issue MRS command to exit MPR mode; MR3 A2= 0.
11. Wait until tMRD and tMOD are satisfied; Continue with regular DRAM commands like Activate.

MPR Write Timing and Write to Read Timing

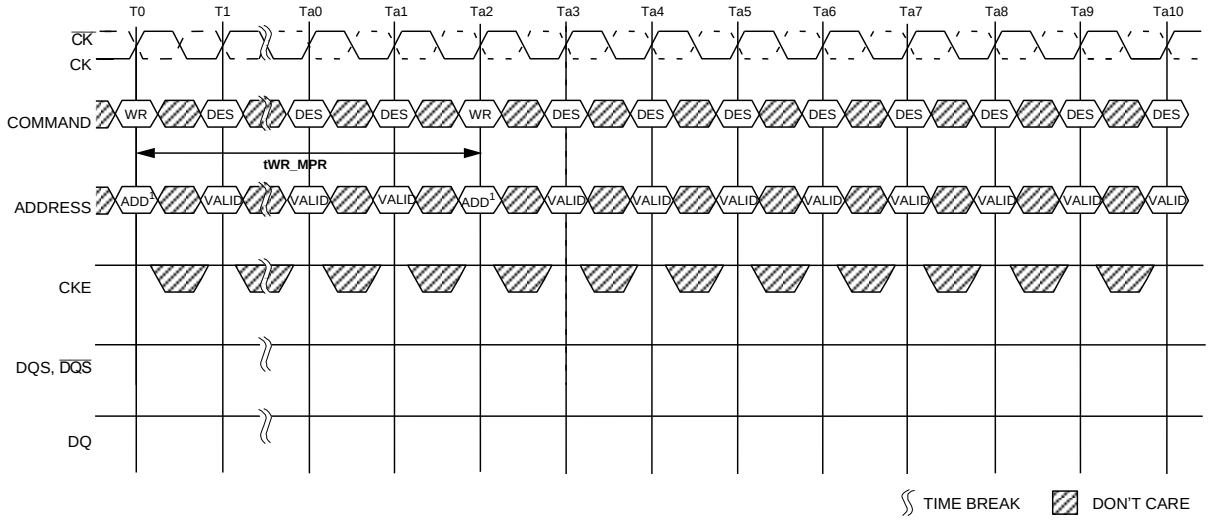


NOTE 1 Multipurpose registers Read/Write Enable (MR3 A2 = 1).

NOTE 2 Address setting:
BA1 and BA0 indicate the MPR location
A [7:0] = data for MPR
A10 and other address pins are "Don't Care"

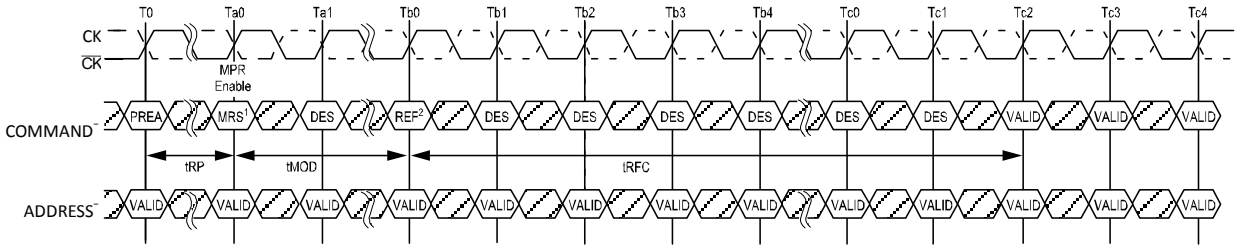
NOTE 3 Parity latency (PL) is added to data output delay when C/A parity latency mode is enabled.

MPR Back-to-Back WRITE Timing



NOTE 1 Address setting:
BA1 and BA0 indicate the MPR location
A [7:0] = data for MPR
A10 and other address pins are "Don't Care"

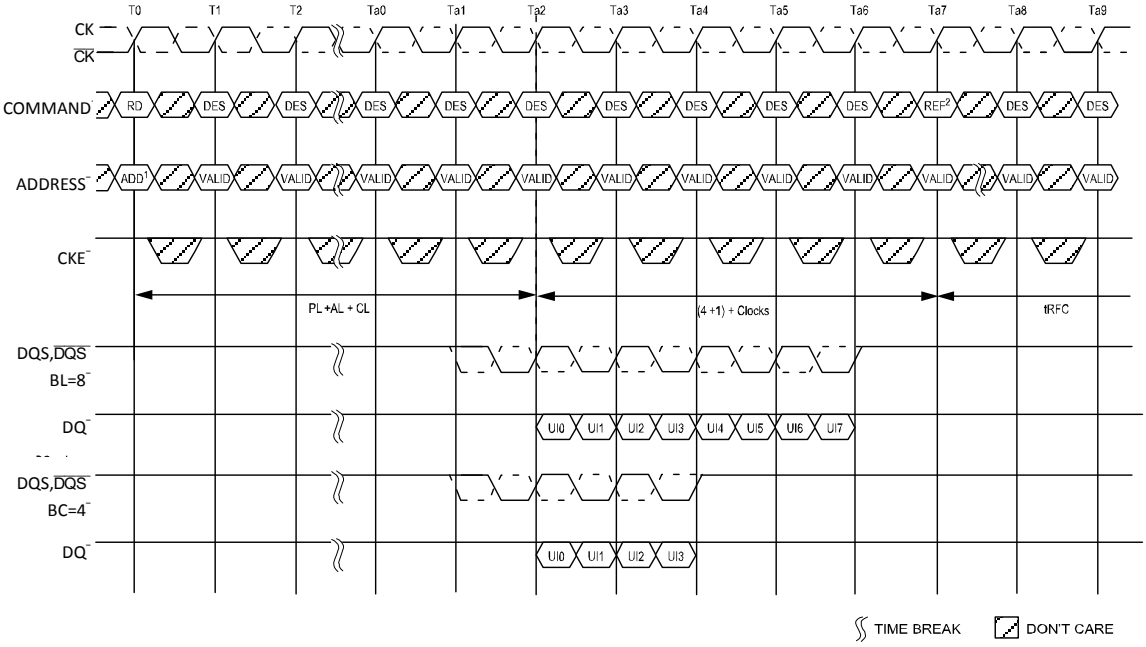
REFRESH Command Timing



NOTE 1 Multipurpose registers Read/Write Enable (MR3 A2 = 1). Redirect all subsequent read and writes to MPR locations.

NOTE 2 1x refresh is only allowed when MPR mode is enabled.

READ-to-REFRESH Command Timing



NOTE 1 Address setting:

A[1:0] = 00 (data burst order is fixed starting at nibble, always 00 here)

A[2]= 0 (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7)

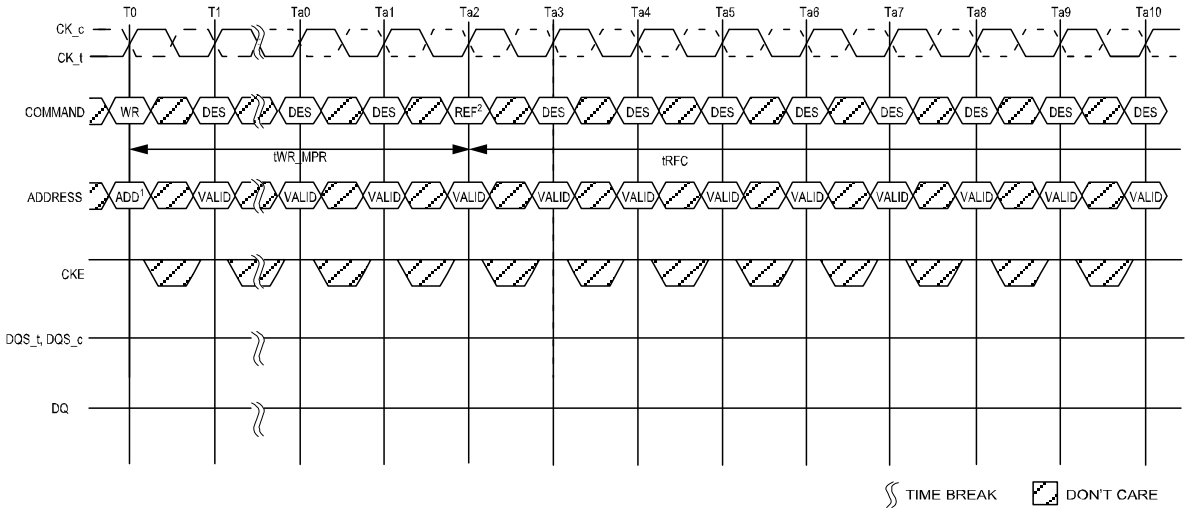
BA1 and BA0 indicate the MPR location

A10 and other address pins are "Don't Care" including BG1 and BG0.

A12 is "Don't Care" when MR0 A[1:0] = 00 or 10, and must be 1b when MR0 A[1:0] = 01

NOTE 2 1x refresh is only allowed when MPR mode is enabled.

WRITE-to-REFRESH Timing



NOTE 1 Address setting: BA1 and BA0 indicate the MPR location A [7:0] = data for MPR
A10 and other address pins are "Don't Care"

NOTE 2 1x refresh is only allowed when MPR mode is enabled.

Data Mask(DM), Data Bus Inversion (DBI) and TDQS

DDR4 SDRAM supports Data Mask (DM) function and Data Bus Inversion (DBI) function in x8 and x16 DRAM configuration. x4 DDR4 SDRAM does not support DM and DBI function. x8 DDR4 SDRAM supports TDQS function. x4 and x16 DDR4 SDRAM does not support TDQS function.DM, DBI & TDQS functions are supported with dedicated one pin labeled as $\overline{DM}/\overline{DBI}/\overline{TDQS}$. The pin is bi-directional pin for DRAM. The $\overline{DM}/\overline{DBI}$ pin is Active Low as DDR4 supports VDDQ reference termination. TDQS function does not drive actual level on the pin.DM, DBI & TDQS functions are programmable through DRAM Mode Register (MR). The MR bit location is bit A11 in MR1 and bit A12:A10 in MR5 .

Write operation: Either DM or DBI function can be enabled but both functions cannot be enabled simultaneously. When both DM and

DBI functions are disabled, DRAM turns off its input receiver and does not expect any valid logic level. Read operation: Only DBI function applies. When DBI function is disabled, DRAM turns off its output driver and does not drive any valid logic level.

TDQS function: When TDQS function is enabled, DM & DBI functions are not supported. When TDQS function is disabled, DM and DBI functions are supported as described below.When enabled, the same termination resistance function is applied to the $\overline{TDQS}$/TDQS pins that is applied to $\overline{DQS}$/DQS pins.

DM, DBI & TDQS functions are programmable through DRAM Mode Register (MR) shown as below

DM, DBI & TDQS MRS

TDQS MR1 A[11]	Read DBI MR5 A[12]	Write DBI MR5 A[11]	Data Mask MR5 A[10]
0=Disable	0=Disable	0=Disable	0=Disable
1=Enable	1=Enable	1=Enable	1=Enable

TDQS function: When TDQS function is enabled, DM & DBI functions are not supported. When TDQS function is disabled, DM and DBI functions are supported as table below.

DBI vs. DM vs. TDQS Function Matrix

TDQS (x8 only) MR1 A[11]	Data Mask MR5 A[10]	Read DBI MR5 A[12]	Write DBI MR5 A[11]
Disabled	Enabled	Enabled or Disabled	Disabled
Disabled	Disabled	Enabled or Disabled	Enabled
Disabled	Disabled	Enabled or Disabled	Disabled
Enabled	Disabled	Disabled	Disabled

DM function during Write operation: DRAM masks the write data received on the DQ inputs if $\overline{DM}$ was sampled Low on a given byte lane. If $\overline{DM}$ was sampled High on a given byte lane, DRAM does not mask the write data and writes into the DRAM core. DBI function during Write operation: DRAM inverts write data received on the DQ inputs if $\overline{DBI}$ was sampled Low on a given byte lane. If $\overline{DBI}$ was sampled High on a given byte lane, DRAM leaves the data received on the DQ inputs non-inverted.DBI function during Read operation: DRAM inverts read data on its DQ outputs and drives $\overline{DBI}$ pin Low when the number of '0' databits within a given byte lane is greater than 4; otherwise DRAM does not invert the read data and drives $\overline{DBI}$ pin High.

x8 DRAM Write DQ Frame Format

Function	Data transfer							
	0	1	2	3	4	5	6	7
DQ[7:0]	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
$\overline{DM}$ or $\overline{DBI}$	DM0 or DBI0	DM1 or DBI1	DM2 or DBI2	DM3 or DBI3	DM4 or DBI4	DM5 or DBI5	DM6 or DBI6	DM7 or DBI7

x8 DRAM Read DQ Frame Format

Function	Data transfer							
	0	1	2	3	4	5	6	7
DQ[7:0]	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
$\overline{DBI}$	$\overline{DBI0}$	$\overline{DBI1}$	$\overline{DBI2}$	$\overline{DBI3}$	$\overline{DBI4}$	$\overline{DBI5}$	$\overline{DBI6}$	$\overline{DBI7}$

x16 DRAM Write DQ Frame Format

Function	Data transfer							
	0	1	2	3	4	5	6	7
DQ[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
$\overline{LDM}$ or $\overline{LDBI}$	$\overline{LDM0}$ or $\overline{LDBI0}$	$\overline{LDM1}$ or $\overline{LDBI1}$	$\overline{LDM2}$ or $\overline{LDBI2}$	$\overline{LDM3}$ or $\overline{LDBI3}$	$\overline{LDM4}$ or $\overline{LDBI4}$	$\overline{LDM5}$ or $\overline{LDBI5}$	$\overline{LDM6}$ or $\overline{LDBI6}$	$\overline{LDM7}$ or $\overline{LDBI7}$
DQ[15:8]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
$\overline{UDM}$ or $\overline{UDBI}$	$\overline{UDM0}$ or $\overline{UDBI0}$	$\overline{UDM1}$ or $\overline{UDBI1}$	$\overline{UDM2}$ or $\overline{UDBI2}$	$\overline{UDM3}$ or $\overline{UDBI3}$	$\overline{UDM4}$ or $\overline{UDBI4}$	$\overline{UDM5}$ or $\overline{UDBI5}$	$\overline{UDM6}$ or $\overline{UDBI6}$	$\overline{UDM7}$ or $\overline{UDBI7}$

x16 DRAM Read DQ Frame Format

Function	Data transfer							
	0	1	2	3	4	5	6	7
DQ[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
$\overline{LDBI}$	$\overline{LDBI0}$	$\overline{LDBI1}$	$\overline{LDBI2}$	$\overline{LDBI3}$	$\overline{LDBI4}$	$\overline{LDBI5}$	$\overline{LDBI6}$	$\overline{LDBI7}$
DQ[15:8]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
$\overline{UDBI}$	$\overline{UDBI0}$	$\overline{UDBI1}$	$\overline{UDBI2}$	$\overline{UDBI3}$	$\overline{UDBI4}$	$\overline{UDBI5}$	$\overline{UDBI6}$	$\overline{UDBI7}$

ZQ Calibration Commands

ZQ Calibration Description

The ZQCL command is used to perform the initial calibration during the power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. The ZQCL command triggers the calibration engine inside the DRAM and, once calibration is achieved, the calibrated values are transferred from the calibration engine to DRAM IO, which is reflected as an updated output driver and on-die termination values.

The first ZQCL command issued after reset is allowed a timing period of tZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after RESET are allowed a timing period of tZQoper.

The ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter tZQCS. One ZQCS command can effectively correct a minimum of 0.5 % (ZQ correction) of RON and RTT impedance error within 128 nCK for all speed bins assuming the maximum sensitivities specified in the Output Driver and ODT Voltage and Temperature Sensitivity tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the device is subjected to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{TSens} \times \text{Tdriftrate}) + (\text{VSens} \times \text{Vdriftrate})}$$

where TSens = max (dRTTdT, dRONdTM) and VSens = max (dRTTdV, dRONdVM) define the temperature and voltage sensitivities.

For example, if TSens = 1.5% / °C, VSens = 0.15% / mV, Tdriftrate = 1°C / sec and Vdriftrate = 15 mV /sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128\text{ms}$$

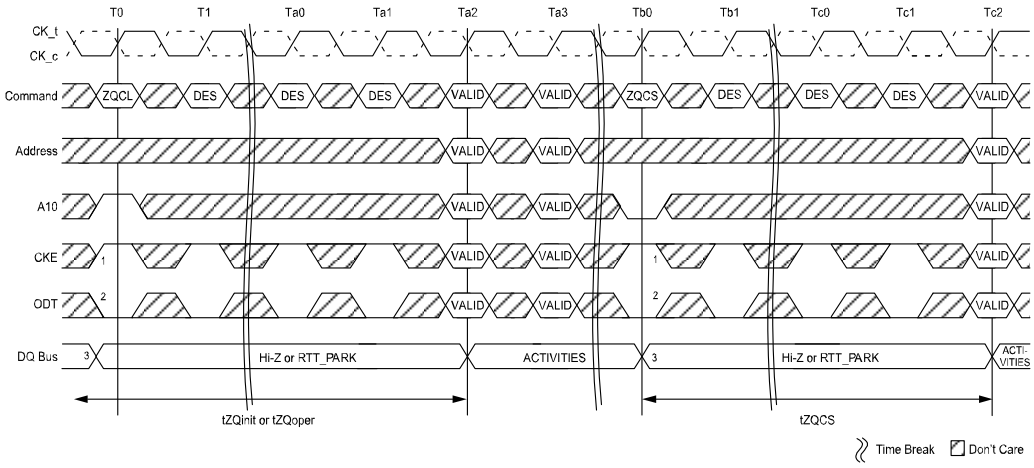
No other activities should be performed on the DRAM channel by the controller for the duration of tZQinit, tZQoper, or tZQCS. The quiet time on the DRAM channel allows accurate calibration of output driver and on-die termination values. Once DRAM calibration is achieved, the device should disable the ZQ current consumption path to reduce power.

All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self refresh. Upon self refresh exit, the device will not perform an IO calibration without an explicit ZQ calibration command. The earliest possible time for a ZQ calibration command (short or long) after self refresh exit is XS, XS_Abort/ XS_FAST depending on operation mode.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of tZQoper, tZQinit, or tZQCS between the devices.

ZQ Calibration Timing



NOTE 1 CKE must be continuously registered HIGH during the calibration procedure.

NOTE 2 During ZQ Calibration, ODT signal must be held LOW and DRAM continues to provide RTT_PARK.

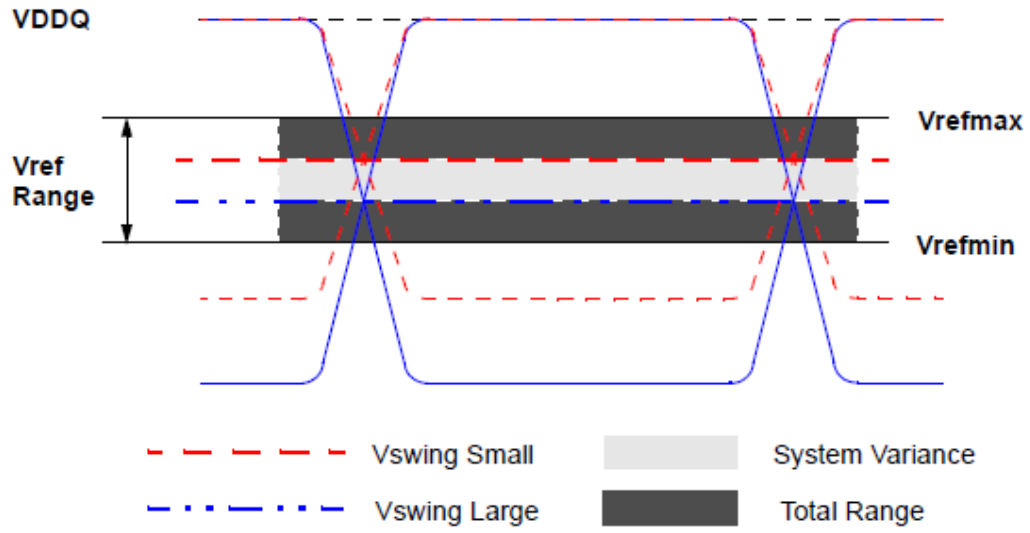
NOTE 3 All devices connected to the DQ bus should be High Z or RTT_PARK during the calibration procedure.

DQ Vref Training

The DRAM internal DQ Vref specification parameters are operating voltage range, stepsize, Vref step time, Vref full step time and Vref valid level.

The voltage operating range specifies the minimum required Vref setting range for DDR4 DRAM devices. The minimum range is defined by Vrefmax and Vrefmin as depicted in the following figure.

VREFDQ Operating Range (Vrefmin, Vrefmax)

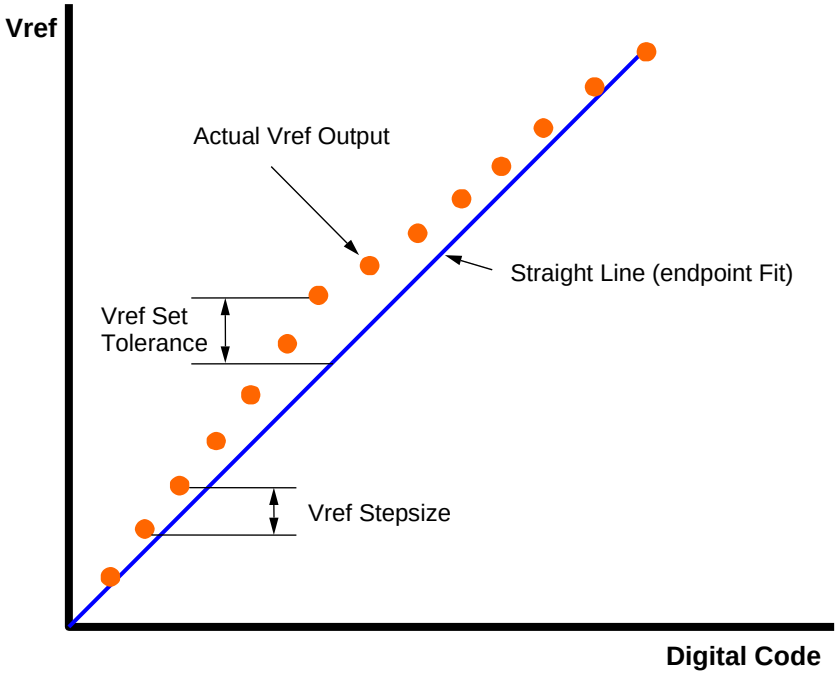


The Vref stepsize is defined as the stepsize between adjacent steps. Vref stepsize ranges from 0.5% VDDQ to 0.8% VDDQ. However, for a given design, DRAM has one value for Vref step size that falls within the range.

The Vref set tolerance is the variation in the Vref voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for Vref set tolerance uncertainty. The range of Vref set tolerance uncertainty is a function of number of steps n.

The Vref set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max Vref values for a specified range. An illustration depicting an example of the stepsize and Vref set tolerance is below.

Example of Vref set tolerance(max case only shown) and stepsize



The V_{REF} increment/decrement step times are defined by V_{REF_time}. V_{REF_time} is defined from t0 to t1, where t1 is referenced to when the V_{REF} voltage is at the final DC level within the V_{REF} valid tolerance ($V_{REF\_val\_tol}$).

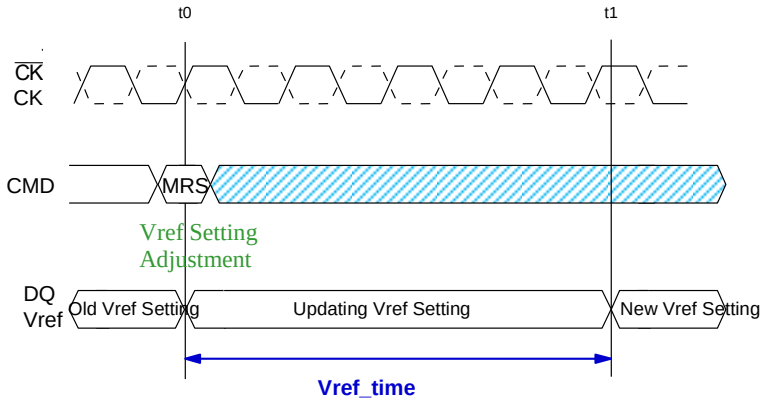
The V_{REF} valid level is defined by V_{REF_val} tolerance to qualify the step time t1. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any V_{REF} increment/decrement adjustment.

This parameter is only applicable for DRAM component level validation/charachterization.

V_{REF_time} is the time including up to $V_{REF,min}$ to $V_{REF,max}$ or $V_{REF,max}$ to $V_{REF,min}$ change in V_{REF} voltage.

Note:
t0 - is referenced to the MRS command clock
t1 - is referenced to $V_{REF\_val\_tol}$

Vref_time timing diagram



VrefDQ Calibration Mode is entered via MRS command setting MR6 A [7] to 1 (0 disables VrefDQ Calibration Mode),

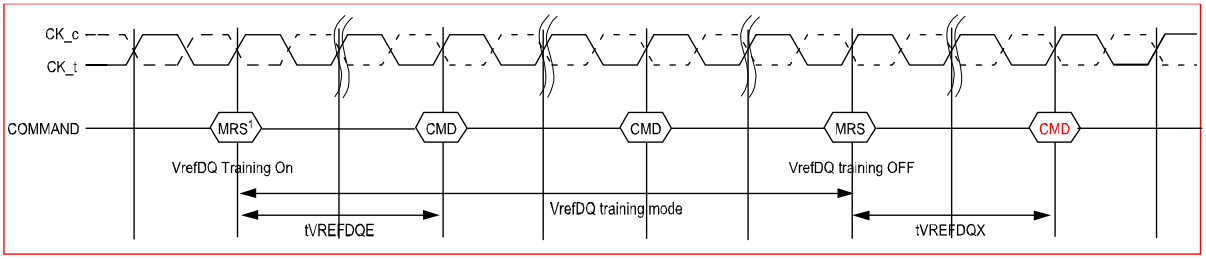
and setting MR6 A [6] to either 0 or 1 to select the desired range, and MR6 A [5:0] with a "don't care" setting (there is no default initial setting; whether VrefDQ training value (MR6 A [5:0]) at training mode entry with MR6 A [7] =1 is captured by the DRAM or not is vendor specific). The next subsequent MR command is used to set the desired VrefDQ values at MR6 A [5:0]. Once VrefDQ Calibration Mode has been entered, VrefDQ Calibration Mode legal commands may be issued once tVREFDQE has been satisfied. VrefDQ Calibration Mode legal commands are ACT, WR, WRA, RD, RDA, PRE, DES, MRS to set VrefDQ values, and MRS to exit VrefDQ Calibration Mode. Once VrefDQ Calibration Mode has been entered, "dummy" write commands may be issued prior to adjusting VrefDQ value the first time VrefDQ calibration is performed after initialization. The "dummy" write commands may have bubbles between write commands provided other DRAM timings are satisfied. A possible example command sequence would be: WR1, DES, DES, DES, WR2, DES, DES, DES, WR3, DES, DES, DES, WR4, DES, DES……. DES, DES, WR50, DES, DES, DES. Setting VrefDQ values requires MR6 [7] set to 1, MR6 [6] unchanged from initial range selection, and MR6 A [5:0] set to desired VrefDQ value; if MR6 [7] is set to 0, MR6

[6;0] are not written. Vref_time must be satisfied after each MR6 command to set VrefDQ value before the internal VrefDQ value is valid.

If PDA mode is used in conjunction with VrefDQ calibration, the PDA mode requirement that only MRS commands are allowed while PDA mode is enabled is not waived. That is, the only VrefDQ Calibration Mode legal commands noted above that may be used are the MRS commands, i.e. MRS to set VrefDQ values, and MRS to exit VrefDQ Calibration Mode.

The last A [6:0] setting written to MR6 prior to exiting VrefDQ Calibration Mode is the range and value used for the internal VrefDQ setting. VrefDQ Calibration Mode may be exited when the DRAM is in idle state. After the MRS command to exit VrefDQ Calibration Mode has been issued, DES must be issued till tVREFDQX has been satisfied where any legal command may then be issued.

VrefDQ training mode entry and exit timing diagram



NOTE 1 The MR command used to enter VrefDQ Calibration Mode treats MR6 A [5:0] as don' t care while the next subsequent MR command sets VrefDQ values in MR6 A[5:0]

NOTE 2 Depending on the step size of the latest programmed VREF value, Vref_time-must be satisfied before disabling VrefDQ training mode.

AC parameters of DDR4 VrefDQ training

Speed		DDR4-1600,1866, 2133,2400,2666		Units	NOTE
Parameter	Symbol	Min	Max		
VrefDQ training					
Enter VrefDQ training mode to the first valid command delay	**tVREFDQE**	150	–	ns	
Exit VrefDQ training mode to the first valid command delay	**tVREFDQX**	150	–	ns	

Example scripts for VREFDQ Calibration Mode

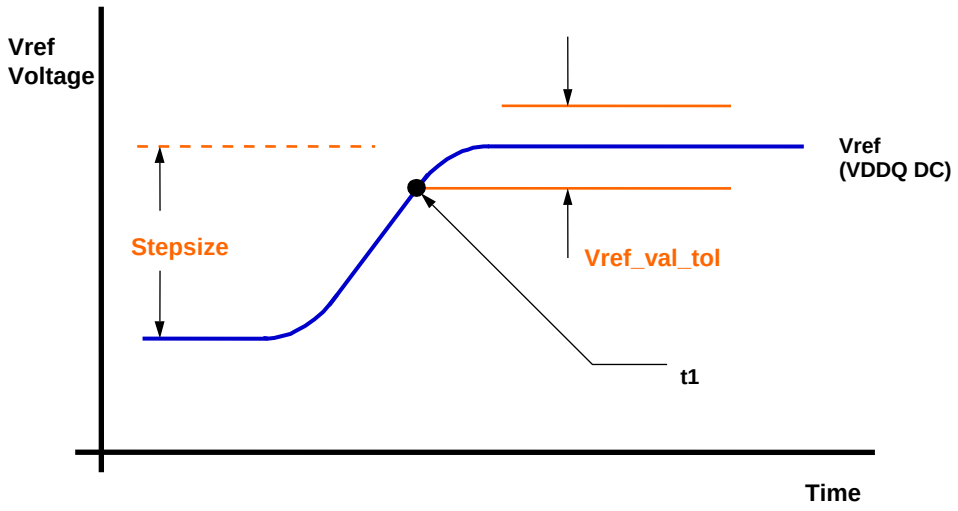
When MR6 A [7] = 0 then MR6 A [6:0] = XXXXXXX
Entering VREFDQ Calibration if entering range 1:

- MR6 A [7:6] =10 & A [5:0] =XXXXXX
- All subsequent VREFDQ Calibration MR setting commands are MR6 A [7:6] =10 & MR6 A [5:0] =VVVVVV {VVVVVV are desired settings for VrefDQ}
- Issue ACT/WR/RD looking for pass/fail to determine Vcent(midpoint) as needed
- Just prior to exiting VREFDQ Calibration mode:
- Last two VREFDQ Calibration MR commands are
- MR6 A [7:6] =10, MR6 A [5:0] =VVVVVV' where VVVVVV' = desired value for VREFDQ
- MR6 A [7] =0, MR6 A [6:0] =XXXXXXX to exit VREFDQ Calibration mode

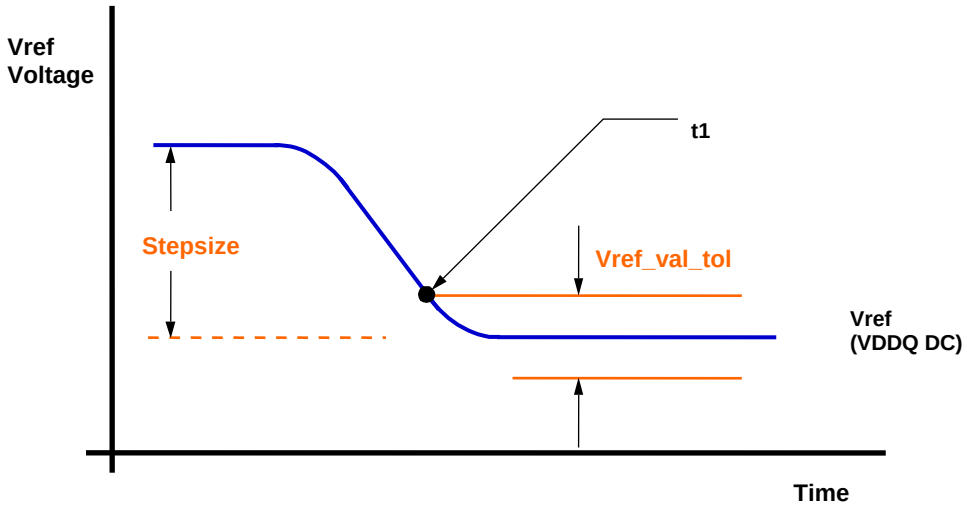
Entering VREFDQ Calibration if entering range 2:

- MR6 A [7:6] =11 & A [5:0] =XXXXXX
- All subsequent VREFDQ Calibration MR setting commands are MR6 A [7:6] =11 & MR6 A [5:0] =VVVVVV {VVVVVV are desired settings for VrefDQ}
- Issue ACT/WR/RD looking for pass/fail to determine Vcent(midpoint) as needed
- Just prior to exiting VREFDQ Calibration mode:
- Last two VREFDQ Calibration MR commands are
- MR6 A [7:6] =11, MR6 A [5:0] =VVVVVV' where VVVVVV' = desired value for VREFDQ
- MR6 A [7] =0, MR6 A [6:0] =XXXXXXX to exit VREFDQ Calibration mode

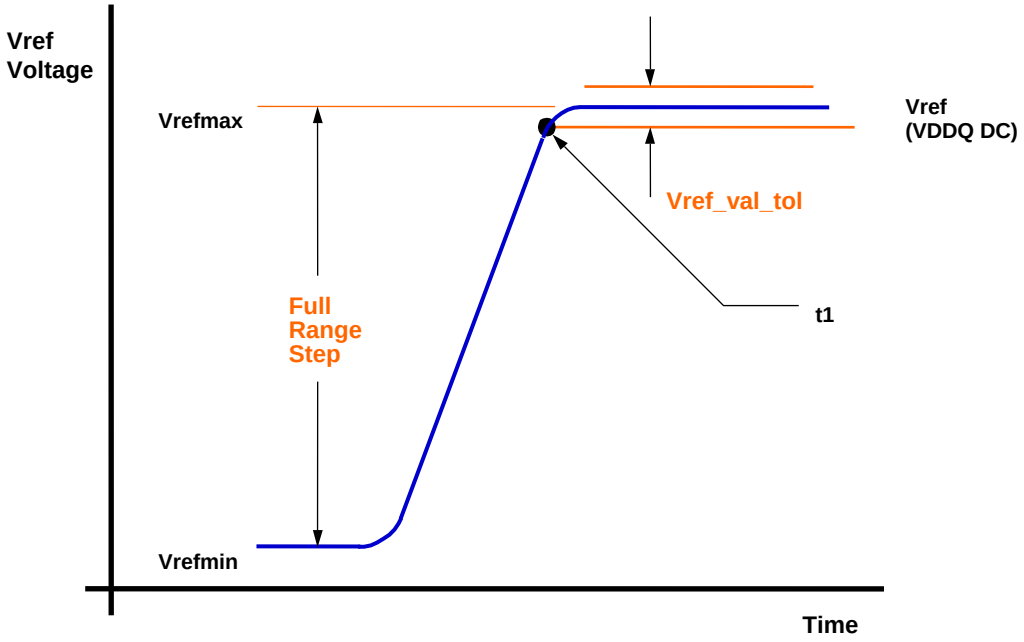
VREF Step Single Step Size Increment Case



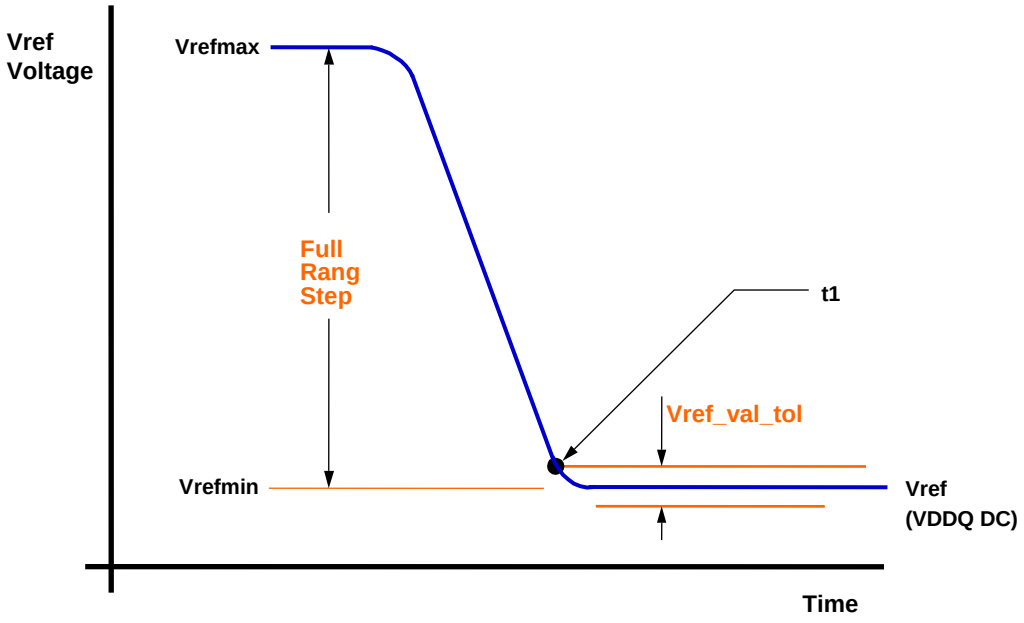
VREF Step Single Step Size Decrement Case



VREF Full Step From VREF,min to VREF,max Case



VREF Full Step From VREF,max to VREF,minCase



The DDR4 SDRAM internally generates its own V_{REFDQ}. DRAM internal V_{REFDQ} specification parameters: voltage range, step-size, V_{REF} step time, V_{REF} full step time, and V_{REF} valid level. The voltage operating range specifies the minimum required V_{REF} setting range for DDR4 DRAM devices. The minimum range is defined by $V_{REFDQ,min}$ and $V_{REFDQ,max}$. A calibration sequence should be performed by the DRAM controller to adjust V_{REFDQ} and optimize the timing and voltage margin of the DRAM data input receivers.

DQ Internal Vref Specifications

Symbol	Parameter	Min	Typ	Max	Unit	NOTE
VrefDQ R1	Range 1 VrefDQ operating points	60%	–	92%	VDDQ	1, 10
VrefDQ R2	Range 2 VrefDQ operating points	45%	–	77%	VDDQ	1, 10
Vref step	Vref Stepsize	0.50%	0.65%	0.80%	VDDQ	2
Vref_set_tol	Vref Set Tolerance	-1.625%	0.00%	1.625%	VDDQ	3, 4, 6
		-0.15%	0.00%	0.15%	VDDQ	3, 5, 7
Vref_time	Vref Step Time	–	–	150	ns	8,11
Vref_val_tol	Vref Valid tolerance	-0.15%	0.00%	0.15%	VDDQ	9

NOTE 1. VREF(DC) voltage is referenced to VDDQ(DC). VDDQ(DC) is 1.2V.

NOTE 2. VREF step size increment/decrement range. VREF at DC level.

NOTE 3. VREF_new = VREF_old ± n × VREF_step; n = number of steps. If increment, use "+;" if decrement, use "-."

NOTE 4. The minimum value of VREF setting tolerance = VREF_new - 1.625% × VDDQ. The maximum value of VREF setting tolerance = VREF_new + 1.625% × VDDQ for n>4

NOTE 5. The minimum value of VREF setting tolerance = VREF_new - 0.15% × VDDQ. The maximum value of VREF setting tolerance = VREF_new + 0.15% × VDDQ for n≤4

NOTE 6. Measured by recording the MIN and MAX values of the VREF output over the range, drawing a straight line between those points, and comparing all other VREF output settings to that line.

NOTE 7. Measured by recording the MIN and MAX values of the VREF output across four consecutive steps (n = 4), drawing a straight line between those points, and comparing all VREF output settings to that line.

NOTE 8. Time from MRS command to increment or decrement one step size up to the full range of VREF.

NOTE 9. Only applicable for DRAM component-level test/characterization purposes. Not applicable for normal mode of operation. VREF valid qualifies the step times, which will be characterized at the component level.

NOTE 10. DRAM range 1 or range 2 is set by the MR6, A6.

NOTE 11. If the Vref monitor is enabled, Vref_time must be derated by: +10ns if DQ bus load is 0pF and an additional +15ns/pF of DQ bus loading.

NOTE 12. Internal VREFDQ specification parameters: voltage range, step size, Vref full step time, Vref step time, and Vref valid level are not pass or fail limits. These parameters are used to help provide estimated values for the internal VrefDQ.

Per-DRAM Addressability (PDA Mode)

DDR4 allows programmability of a single, specific DRAM on a rank. This feature can be used to program different ODT or Vref values on DRAM devices on a given rank. the DRAM may incorrectly read DQ level at the first DQS edge and the last falling DQS edge. It is recommended that DRAM samples DQ0 on either the first falling or second rising DQS edges. This supports a common implementation between BC4 and BL8 modes on the DRAM. The DRAM controller is required to drive DQ0 to a 'Stable Low or High' during the length of the data transfer for BC4 and BL8 cases.

1. Before entering Per-DRAM addressability mode, write leveling is required.
2. Before entering per-DRAM addressability mode, the following MR settings are possible:
   - RTT_PARK MR5 A [8:6] = Enabled
   - RTT_NOM MR1 A [10:8] = Enabled
3. Enable per-DRAM addressability mode using MR3 A [4] = 1. (The default programmed value of MR3 A [4] = 0.)
4. In the per-DRAM addressability mode, all MRS commands are qualified with DQ0 forx4, x8, x16. The device captures DQ0 by using DQS and $\overline{DQS}$ for x4 and x8, DQSL and $\overline{DQSL}$ for x16 signals as shown MRS w/ per DRAM addressability (PDA) issuing before MRS. If the value on DQ0 for x4, x8, x16 is 0, then DRAM executes the MRS command. If the value on DQ0 is 1, the DRAM ignores the MRS command. The controller can choose to drive all the DQ bits.
5. Program the desired DRAM and mode registers using the MRS command and DQ0 for x4, x8, x16.
6. In per-DRAM addressability mode, only MRS commands are allowed.
7. The MODE REGISTER SET command cycle time at AL + CWL + BL/2 – 0.5 tCK+ tMRD_PDA + (PL) is required to complete the WRITE operation to the mode register and is the minimum time required between two MRS commands. shown in MRS w/ per DRAM addressability (PDA) issuing before MRS.
8. Remove the device from per-DRAM addressability mode by setting MR3[4] = 0. (This command requires DQ0 = 0 for x4, x8, x16.)

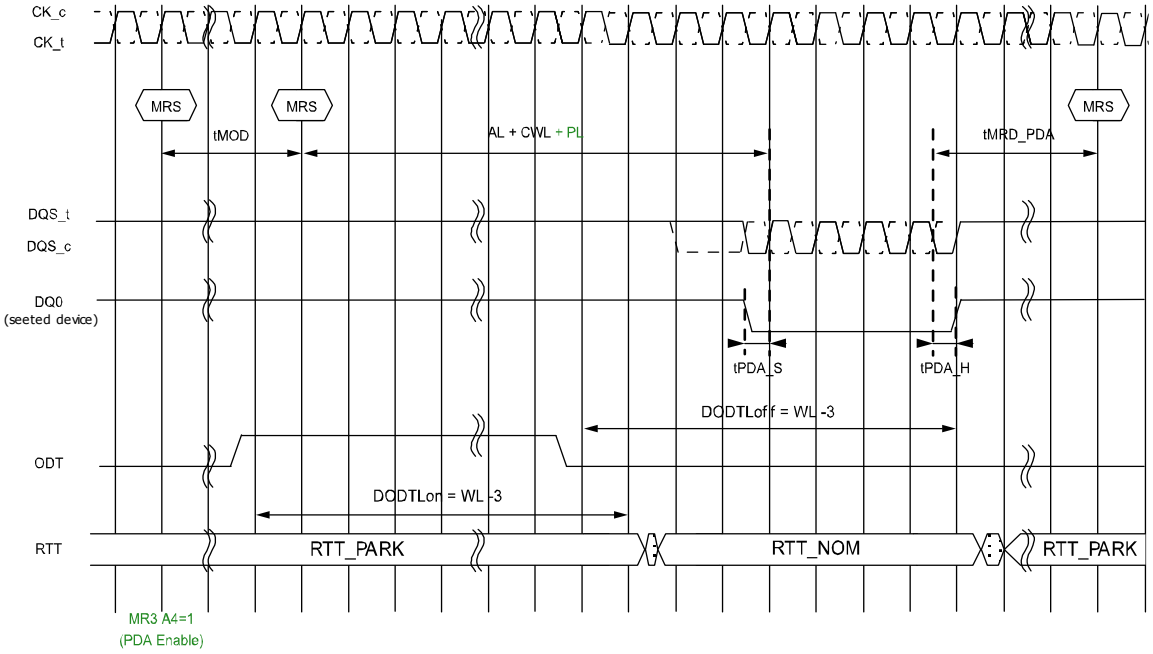
NOTE: Removing a DRAM from per-DRAM addressability mode will require programming the entire MR3 when the MRS command is issued. This may impact some per-DRAM addressability values programmed within a rank as the EXIT command is sent to the rank. In order to avoid such a case, the PDA Enable/Disable Control bit is located in a mode register that does not have any Per-DRAM addressability mode controls.

In per-DRAM addressability mode, the device captures DQ0 for x4, x8, x16 using DQS and $\overline{DQS}$ for x4, x8, DQSL and $\overline{DQSL}$ for x16like normal WRITE operation; however, dynamic ODT is not supported. Extra care is required for the ODT setting. If RTT_NOM MR1 [10:8] = Enable, DDR4 SDRAM data termination needs to be controlled by the ODT pin and applies the same timing parameters as defined in direct ODT function that is shown below. VrefDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 low level for entering PDA mode.

Applied ODT Timing Parameter to PDA Mode

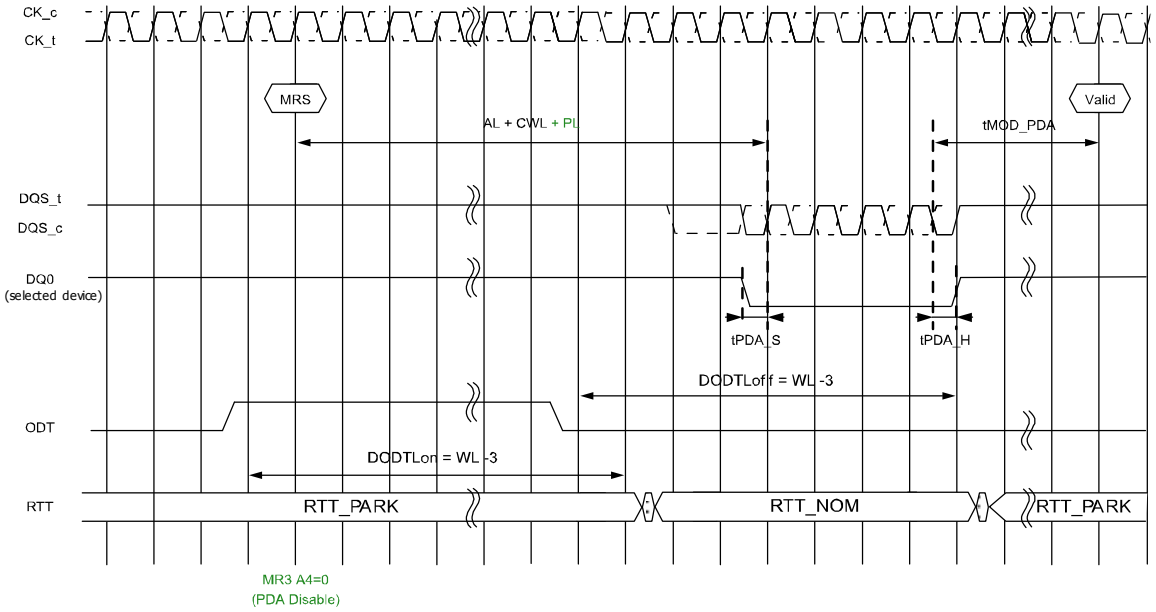
Symbol	Parameter
DODTLon	Direct ODT turn on latency
DODTLoff	Direct ODT turn off latency
tADC	RTT change timing skew
tAONAS	Asynchronous RTT_NOM turn-on delay
tAOFAS	Asynchronous RTT_NOM turn-off delay

MRS w/ per DRAM addressability (PDA) issuing before MRS



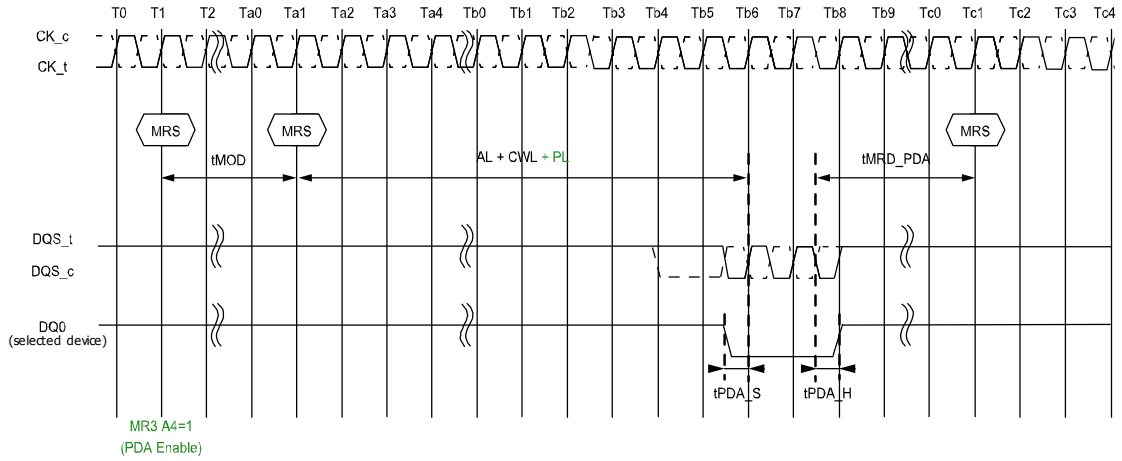
NOTE RTT_PARK = Enable, RTT_NOM = Enable, Write Preamble Set = 2tCK and DLL = ON, CA parity is used

MRS w/ per DRAM addressability (PDA) Exit



NOTE RTT_PARK = Enable; RTT_NOM = Enable, Write Preamble Set = 2tCK and DLL = ON, CA parity is used

PDA using Burst Chop 4



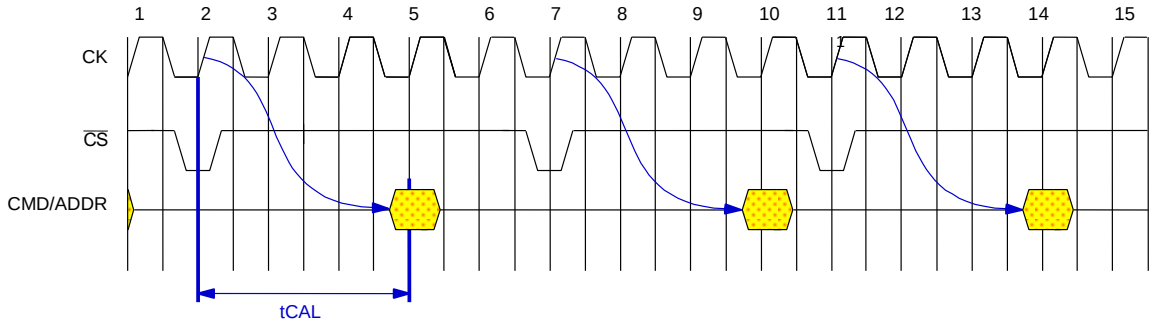
NOTE CA parity is used

CAL Mode ($\overline{CS}$ to Command Address Latency)

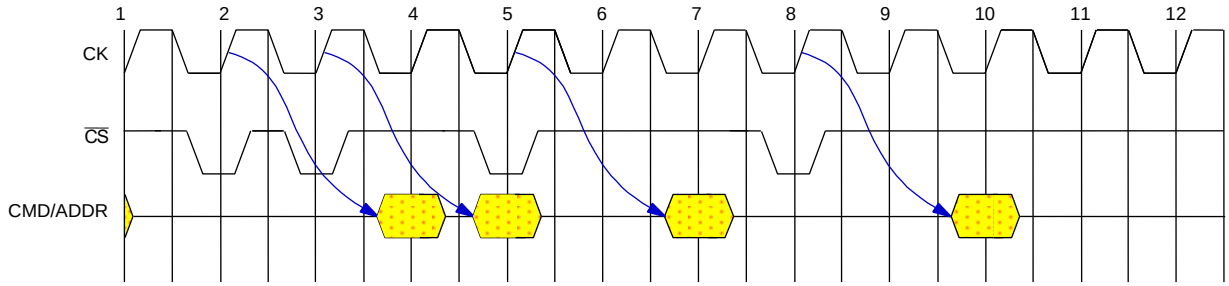
CAL Mode Description

DDR4 supports the Command Address Latency (CAL) function as a power savings feature. CAL is the delay in clock cycles between CS and CMD/ADDR defined by MR4 A [8:6]. CAL gives the DRAM time to enable the CMD/ADDR receivers before a command is issued. Once the command and the address are latched, the receivers can be disabled. For consecutive commands, the DRAM will keep the receivers enabled for the duration of the command sequence.

Definition of CAL Timing



CAL Operational Timing for Consecutive command issues



The following tables show the timing requirements for tCAL and MRS settings at different data rates.

$\overline{CS}$ to Command Address Latency

Parameter	Symbol	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	Units	Note
$\overline{CS}$ to Command Address Latency	tCAL(min)	max(3 nCK, 3.748 ns)				nCK	1
NOTE 1 Geardown mode is not supported for speed bins below DDR4-2666.							

Parameter	Symbol	DDR4-2666	Units	Note
$\overline{CS}$ to Command Address Latency	tCAL(min)	max(3 nCK, 3.748 ns)	nCK	1
NOTE 1 In geardown mode, odd nCK values for tCAL are not supported, and nCK values must be rounded up to the next higher even integer. For example, when operating at DDR4-2666, a minimum of 6 nCK is required for tCAL.				

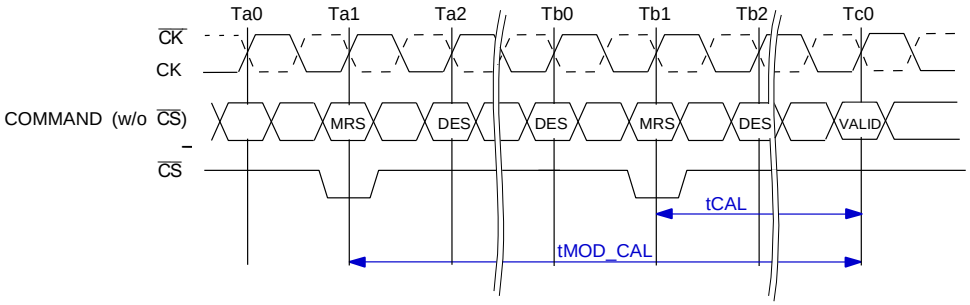
MRS settings for CAL

A[8:6] @ MR4	CAL (tCK cycles)
000	**Default (disable)**
001	**3**
010	**4**
011	**5**
100	**6**
101	**8**
110	**Reserved**
111	**Reserved**

MRS Timings with Command/Address Latency enabled

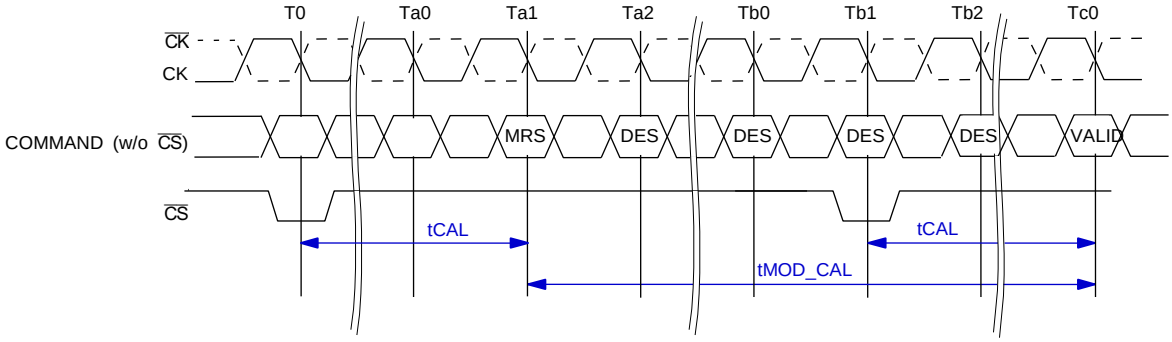
When the Command Address Latency mode is enabled; users must allow more time for MRS commands to take effect. When CAL mode is enabled, or being enabled by an MRS command, the earliest the next valid command can be issued is tMOD_CAL, where tMOD_CAL=tMOD+tCAL. The two following figures are examples.

CAL Enable Timing - tMOD_CAL



NOTE 1 MRS command at Ta1 enables CAL mode
NOTE 2 tMOD_CAL=tMOD+tCAL.

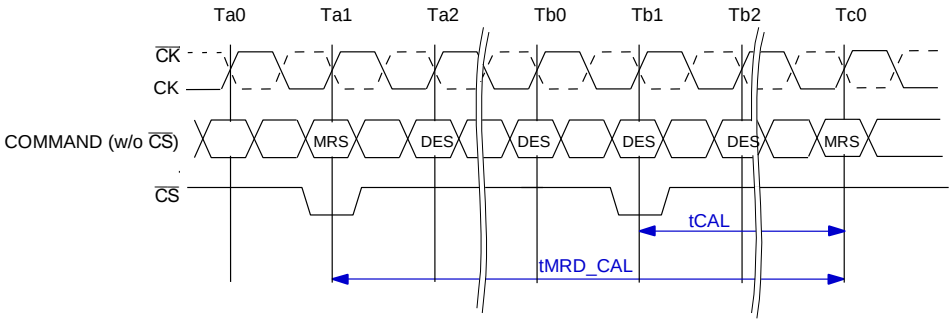
tMOD_CAL, MRS to Valid Command Timing with CAL Enabled



NOTE 1 MRS at Ta1 may or may not modify CAL, tMOD_CAL is computed based on new tCAL setting if modified.
NOTE 2 tMOD_CAL=tMOD+tCAL.

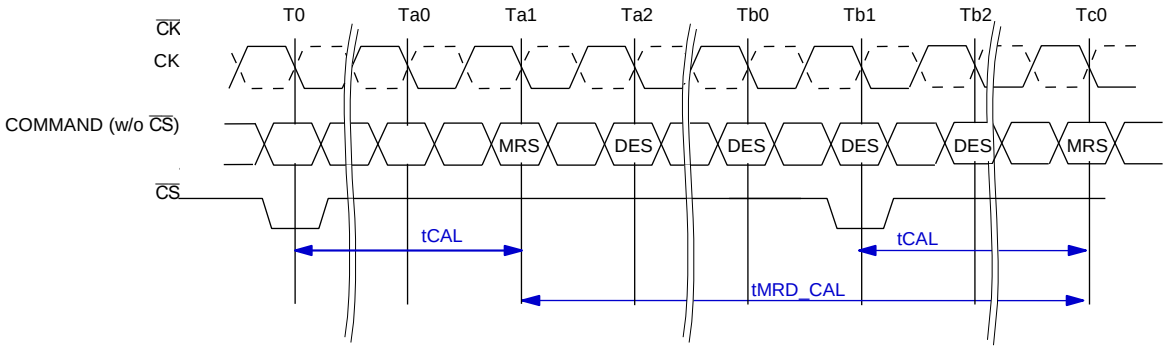
When Command/Address latency is enabled or being entered, users must wait tMRD_CAL until the next MRS command can be issued. tMRD_CAL=tMOD+tCAL. The two following figures are examples.

CAL Enabling MRS to Next MRS Command, tMRD_CAL



NOTE 1 MRS command at Ta1 enables CAL mode.
NOTE 2 tMRD_CAL=tMOD+tCAL

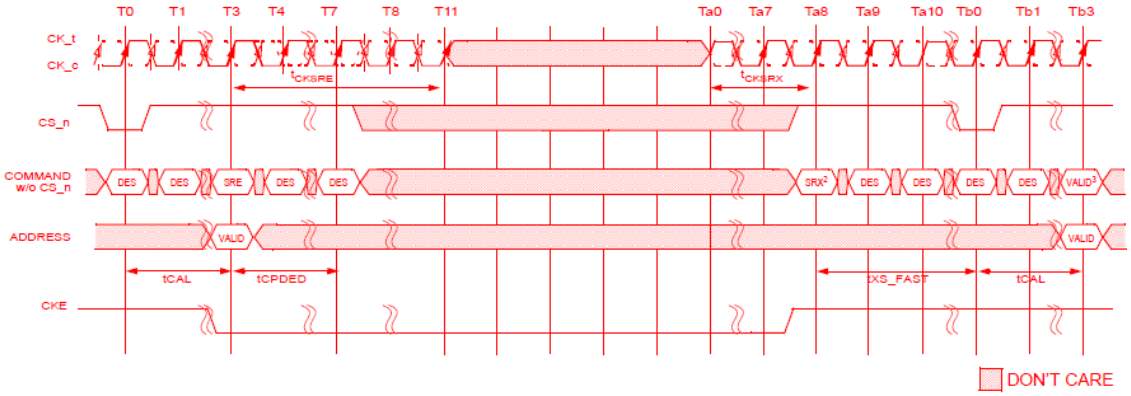
tMRD_CAL, Mode Register Cycle Time with CAL Enabled



NOTE 1 MRS at Ta1 may or may not modify CAL, tMRD_CAL is computed based on new tCAL setting.
NOTE 2 tMRD_CAL=tMOD+tCAL

Command Address Latency Examples: Consecutive READ BL8 with two different CALs and 1tCK Preamble in Different Bank Group shown in figures below.

Self Refresh Entry, Exit Timing with CAL

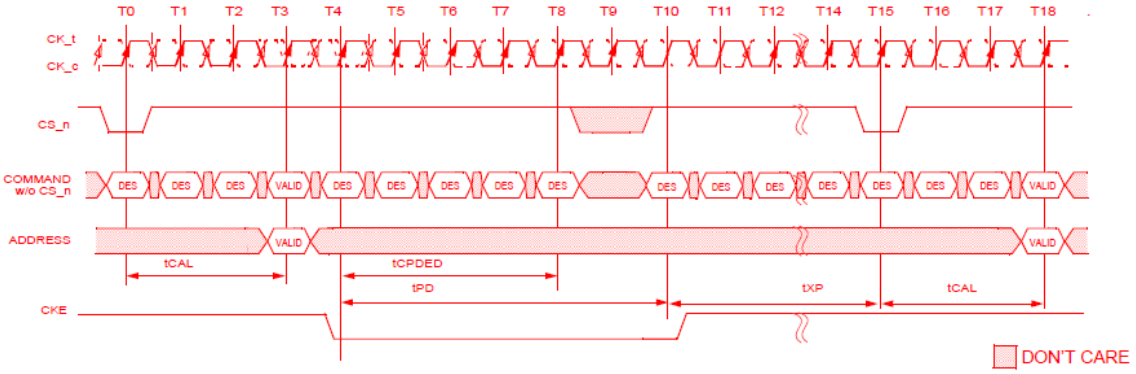


NOTE 1 tCAL = 3nCK, tCPDED = 4nCK, tCKSRE = 8nCK, tCKSRX = 8nCK, tXS_FAST = tRFC4(min) + 10ns

NOTE 2 $\overline{CS}$ = H, $\overline{ACT}$ = Don't Care, $\overline{RAS}$/A16 = Don't Care, $\overline{CAS}$/A15 = Don't Care, $\overline{WE}$/A14 = Don't Care

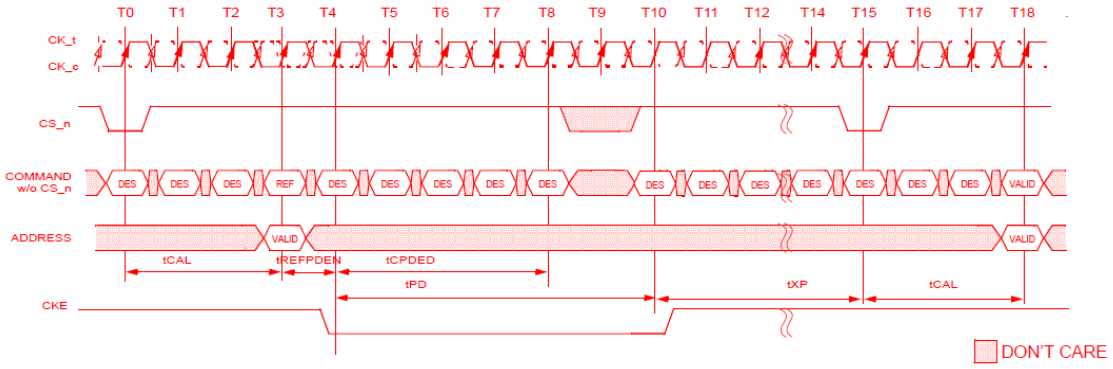
NOTE 3 Only MRS (limited to those described in the Self-Refresh Operation section). ZQCS or ZQCL command allowed.

Power Down Entry, Exit Timing with CAL



NOTE 1 tCAL = 3nCK, tCPDED = 4nCK, tPD = 6nCK, tXP = 5nCK

Refresh Command to Power Down Entry



NOTE 1 tCAL = 3nCK, tREFPDEN = 1nCK, tCPDED = 4nCK, tPD = 6nCK, tXP = 5nCK.

CRC

CRC Polynomial and logic equation

DDR4 supports CRC for write operation, and doesn't support CRC for read operation.

The CRC polynomial used by DDR4 is the ATM-8 HEC, X^8+X^2+X^1+1

A combinatorial logic block implementation of this 8-bit CRC for 72-bits of data contains 272 two-input XOR gates contained in eight 6 XOR gate deep trees.

The CRC polynomial and combinatorial logic used by DDR4 is the same as used on GDDR5.

CRC Error Detection Details

Error Type	Detection Capability
Random Single Bit Error	100%
Random Double Bit Error	100%
Random Odd Count Error	100%
Random one Multi-bit UI vertical column error detection excluding DBI bits	100%

CRC Polynomial and logic equation

```
module CRC8_D72;
// polynomial: (0 1 2 8)
// data width: 72
// convention: the first serial data bit is D [71]
// initial condition all 0 implied
function [7:0]
nextCRC8_D72;
input [71:0] Data;
reg [71:0] D;
reg [7:0] NewCRC;
begin
D = Data;
NewCRC[0] =  D[69] ^ D[68] ^ D[67] ^ D[66] ^ D[64] ^ D[63] ^ D[60] ^
             D[56] ^ D[54] ^ D[53] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^
             D[45] ^ D[43] ^ D[40] ^ D[39] ^ D[35] ^ D[34] ^ D[31] ^
             D[30] ^ D[28] ^ D[23] ^ D[21] ^ D[19] ^ D[18] ^ D[16] ^
             D[14] ^ D[12] ^ D[8] ^ D[7] ^ D[6] ^ D[0] ;
NewCRC[1] =  D[70] ^ D[66] ^ D[65] ^ D[63] ^ D[61] ^ D[60] ^ D[57] ^
             D[56] ^ D[55] ^ D[52] ^ D[51] ^ D[48] ^ D[46] ^ D[45] ^
             D[44] ^ D[43] ^ D[41] ^ D[39] ^ D[36] ^ D[34] ^ D[32] ^
             D[30] ^ D[29] ^ D[28] ^ D[24] ^ D[23] ^ D[22] ^ D[21] ^
             D[20] ^ D[18] ^ D[17] ^ D[16] ^ D[15] ^ D[14] ^ D[13] ^
             D[12] ^ D[9] ^ D[6] ^ D[1] ^ D[0];
NewCRC[2] =  D[71] ^ D[69] ^ D[68] ^ D[63] ^ D[62] ^ D[61] ^ D[60] ^
             D[58] ^ D[57] ^ D[54] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
             D[44] ^ D[43] ^ D[42] ^ D[39] ^ D[37] ^ D[34] ^ D[33] ^
             D[29] ^ D[28] ^ D[25] ^ D[24] ^ D[22] ^ D[17] ^ D[15] ^
             D[13] ^ D[12] ^ D[10] ^ D[8] ^ D[6] ^ D[2] ^ D[1] ^ D[0];
NewCRC[3] =  D[70] ^ D[69] ^ D[64] ^ D[63] ^ D[62] ^ D[61] ^ D[59] ^
             D[58] ^ D[55] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^ D[45] ^
             D[44] ^ D[43] ^ D[40] ^ D[38] ^ D[35] ^ D[34] ^ D[30] ^
             D[29] ^ D[26] ^ D[25] ^ D[23] ^ D[18] ^ D[16] ^ D[14] ^
             D[13] ^ D[11] ^ D[9] ^ D[7] ^ D[3] ^ D[2] ^ D[1];
NewCRC[4] =  D[71] ^ D[70] ^ D[65] ^ D[64] ^ D[63] ^ D[62] ^ D[60] ^
             D[59] ^ D[56] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^ D[46] ^
             D[45] ^ D[44] ^ D[41] ^ D[39] ^ D[36] ^ D[35] ^ D[31] ^
             D[30] ^ D[27] ^ D[26] ^ D[24] ^ D[19] ^ D[17] ^ D[15] ^
             D[14] ^ D[12] ^ D[10] ^ D[8] ^ D[4] ^ D[3] ^ D[2];
```

NewCRC[5] = D[71] ^ D[66] ^ D[65] ^ D[64] ^ D[63] ^ D[61] ^ D[60] ^
D[57] ^ D[53] ^ D[51] ^ D[50] ^ D[49] ^ D[47] ^ D[46] ^
D[45] ^ D[42] ^ D[40] ^ D[37] ^ D[36] ^ D[32] ^ D[31] ^
D[28] ^ D[27] ^ D[25] ^ D[20] ^ D[18] ^ D[16] ^ D[15] ^
D[13] ^ D[11] ^ D[9] ^ D[5] ^ D[4] ^ D[3];

NewCRC[6]= D[67] ^ D[66] ^ D[65] ^ D[64] ^ D[62] ^ D[61] ^ D[58] ^
D[54] ^ D[52] ^ D[51] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
D[43] ^ D[41] ^ D[38] ^ D[37] ^ D[33] ^ D[32] ^ D[29] ^
D[28] ^ D[26] ^ D[21] ^ D[19] ^ D[17] ^ D[16] ^ D[14] ^
D[12] ^ D[10] ^ D[6] ^ D[5] ^ D[4];

NewCRC[7]= D[68] ^ D[67] ^ D[66] ^ D[65] ^ D[63] ^ D[62] ^ D[59] ^
D[55] ^ D[53] ^ D[52] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^
D[44] ^ D[42] ^ D[39] ^ D[38] ^ D[34] ^ D[33] ^ D[30] ^
D[29] ^ D[27] ^ D[22] ^ D[20] ^ D[18] ^ D[17] ^ D[15] ^
D[13] ^ D[11] ^ D[7] ^ D[6] ^ D[5];

nextCRC8_D72 = NewCRC

The Controller generates the CRC checksum and forms the write data frames as below tables. The DRAM checks for an error in a received code word D[71:0] by comparing the received checksum against the computed checksum and reports errors using the signal if there is a mis-match. DRAM can write data to the DRAM core without waiting for CRC check for full writes. If bad data is written to the DRAM core, then controller will retry the transaction and overwrite the bad data. Controller is responsible for data coherency.

CRC Data Mapping (X4 Configuration, BL8)

A x4 device has a CRC tree with 32 input bits. The input for the upper 40 bits D[71:32] are '1's.

X4	Transfer Burst Bit (BL8)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	D4	D5	D6	D7	CRC0	CRC4
DQ1	D8	D9	D10	D11	D12	D13	D14	D15	CRC1	CRC5
DQ2	D16	D17	D18	D19	D20	D21	D22	D23	CRC2	CRC6
DQ3	D24	D25	D26	D27	D28	D29	D30	D31	CRC3	CRC7

CRC Data Mapping (X8 Configuration, BL8)

For a x8 DRAM the controller must send 1's in the transfer 9 if CRC is enabled and must send 1's in transfer 8 and transfer 9 of the lane if DBI function is enabled. A x8 device has a CRC tree with 72 input bits. The 8 bits D[71:64] are used if either Write DBI or DM is enabled. Note that Write DBI and DM function cannot be enabled simultaneously. If both Write DBI and DM is disabled, then the inputs of the 8 bits D [71:64] are '1's.

X8	Transfer Burst Bit (BL8)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	D4	D5	D6	D7	CRC0	1
DQ1	D8	D9	D10	D11	D12	D13	D14	D15	CRC1	1
DQ2	D16	D17	D18	D19	D20	D21	D22	D23	CRC2	1
DQ3	D24	D25	D26	D27	D28	D29	D30	D31	CRC3	1
DQ4	D32	D33	D34	D35	D36	D37	D38	D39	CRC4	1
DQ5	D40	D41	D42	D43	D44	D45	D46	D47	CRC5	1
DQ6	D48	D49	D50	D51	D52	D53	D54	D55	CRC6	1
DQ7	D56	D57	D58	D59	D60	D61	D62	D63	CRC7	1
$\overline{DM}$ / $\overline{DBI}$	D64	D65	D66	D67	D68	D69	D70	D71	1	1

CRC Data Mapping (X16 Configuration, BL8)

For a x16 DRAM the controller must send 1's in the transfer 9 if CRC is enabled and must send 1's in transfer 8 and transfer 9 of the DBIL_n and DBIU_n lanes if DBI function is enabled. A x16 device has two identical CRC trees with 72 input bits each. The upper 8 bits are used if either Write DBI or DM is enabled. Note that Write DBI and DM function cannot be enabled simultaneously. If both Write DBI and DM is disabled, then the inputs of the upper 8 bits D [143:136] and D [71:64] are '1's.

A x16 device is treated as two x8 devices; a x16 device will have two identical CRC trees implemented. CRC [7:0] covers data bits D [71:0]. CRC [15:8] covers data bits D [143:72].

X16	Transfer Burst Bit (BL8)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	D4	D5	D6	D7	CRC0	1
DQ1	D8	D9	D10	D11	D12	D13	D14	D15	CRC1	1
DQ2	D16	D17	D18	D19	D20	D21	D22	D23	CRC2	1
DQ3	D24	D25	D26	D27	D28	D29	D30	D31	CRC3	1
DQ4	D32	D33	D34	D35	D36	D37	D38	D39	CRC4	1
DQ5	D40	D41	D42	D43	D44	D45	D46	D47	CRC5	1
DQ6	D48	D49	D50	D51	D52	D53	D54	D55	CRC6	1
DQ7	D56	D57	D58	D59	D60	D61	D62	D63	CRC7	1
$\overline{\text{LDM}}$ / $\overline{\text{LDBI}}$	D64	D65	D66	D67	D68	D69	D70	D71	1	1
DQ8	D72	D73	D74	D75	D76	D77	D78	D79	CRC8	1
DQ9	D80	D81	D82	D83	D84	D85	D86	D87	CRC9	1
DQ10	D88	D89	D90	D91	D92	D93	D94	D95	CRC10	1
DQ11	D96	D97	D98	D99	D100	D101	D102	D103	CRC11	1
DQ12	D104	D105	D106	D107	D108	D109	D110	D111	CRC12	1
DQ13	D112	D113	D114	D115	D116	D117	D118	D119	CRC13	1
DQ14	D120	D121	D122	D123	D124	D125	D126	D127	CRC14	1
DQ15	D128	D129	D130	D131	D132	D133	D134	D135	CRC15	1
$\overline{\text{UDM}}$ / $\overline{\text{UDBI}}$	D136	D137	D138	D139	D140	D141	D142	D143	1	1

CRC Error Handling

CRC Error mechanism shares the same $\overline{\text{ALERT}}$ signal for reporting errors on writes to DRAM. The controller has no way to distinguish between CRC errors and Command/Address/Parity errors other than to read the DRAM mode registers. This is a very time consuming process in a multi-rank configuration.

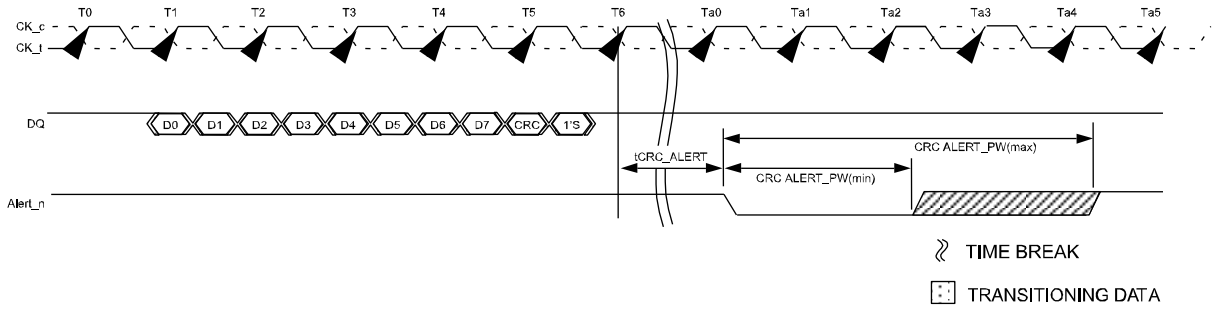
To speed up recovery for CRC errors, CRC errors are only sent back as a pulse. The minimum pulse-width is 6 clocks. The latency to $\overline{\text{Alert}}$ signal is defined as tCRC_ALERT in the figure below.

DRAM will set CRC Error Clear bit in A3 of MR5 to '1' and CRC Error Status bit in MPR3 of page1 to '1' upon detecting a CRC error. The CRC Error Clear bit remains set at '1' until the host clears it explicitly using an MRS command.

The controller upon seeing an error as a pulse width will retry the write transactions. The controller understands the worst case delay for $\overline{\text{Alert}}$ (during unit) and can back up the transactions accordingly or the controller can be made more intelligent and try to correlate the write CRC error to a specific rank or a transaction. The controller is also responsible for opening any pages and ensuring that retrying of writes is done in a coherent fashion.

The pulse width may be seen longer than six clocks at the controller if there are multiple CRC errors as the $\overline{\text{Alert}}$ is a daisy chain bus.

CRC Error Reporting



NOTE 1 CRC ALERT_PW is specified from the point where the DRAM starts to drive the signal low to the point where the DRAM driver releases and the controller starts to pull the signal up.

NOTE 2 Timing diagram applies to x4, x8, and x16 devices.

CRC Error Timing Parmeters

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit
CRC error to $\overline{\text{ALERT}}$ latency	tCRC_ALERT	_	13	_	13	_	13	_	13	ns
CRC $\overline{\text{ALERT}}$ pulse width	CRC ALERT_PW	6	10	6	10	6	10	6	10	nCK

CRC Frame Format with BC4

DDR4 SDRAM supports CRC function for Write operation for Burst Chop 4 (BC4). The CRC function is programmable using DRAM mode register and can be enabled for writes.

When CRC is enabled the data frame length is fixed at 10UI for both BL8 and BC4 operations. DDR4 SDRAM also supports burst length on the fly with CRC enabled. This is enabled using mode register.

CRC Data Bit Mapping for x4 Devices (BC4)

For a x4 device, the CRC tree inputs are 16 data bits; and the inputs for the remaining bits are 1.

CRC Data Mapping (x4 Configuration, BC4, A2 = 0)

X4	Transfer Burst Bit (BC4, A2=0)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	1	1	1	1	CRC0	CRC4
DQ1	D8	D9	D10	D11	1	1	1	1	CRC1	CRC5
DQ2	D16	D17	D18	D19	1	1	1	1	CRC2	CRC6
DQ3	D24	D25	D26	D27	1	1	1	1	CRC3	CRC7

CRC Data Mapping (x4 Configuration, BC4, A2 = 1)

X4	Transfer Burst Bit (BC4, A2=1)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D4	D5	D6	D7	1	1	1	1	CRC0	CRC4
DQ1	D12	D13	D14	D15	1	1	1	1	CRC1	CRC5
DQ2	D20	D21	D22	D23	1	1	1	1	CRC2	CRC6
DQ3	D28	D29	D30	D31	1	1	1	1	CRC3	CRC7

When A2 = 1, data bits D [7:4] are used as inputs for D [3:0], D [15:12] are used as inputs to D [11:8] and so forth for the CRC tree.

CRC with BC4 Data Bit Mapping for x8 Devices

For a x8 device, the CRC tree inputs are 36 data bits in transfer's four through seven as 1's.

CRC Data Mapping (x8 Configuration, BC4, A2 = 0)

X8	Transfer Burst Bit (BC4, A2=1)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	1	1	1	1	CRC0	1
DQ1	D8	D9	D10	D11	1	1	1	1	CRC1	1
DQ2	D16	D17	D18	D19	1	1	1	1	CRC2	1
DQ3	D24	D25	D26	D27	1	1	1	1	CRC3	1
DQ4	D32	D33	D34	D35	1	1	1	1	CRC4	1
DQ5	D40	D41	D42	D43	1	1	1	1	CRC5	1
DQ6	D48	D49	D50	D51	1	1	1	1	CRC6	1
DQ7	D56	D57	D58	D59	1	1	1	1	CRC7	1
$\overline{DM}$ / $\overline{DBI}$	D64	D65	D66	D67	1	1	1	1	1	1

When A2 = 0, the input bits D [67:64] are used if $\overline{DM}$ or $\overline{DBI}$ functions are enabled; if $\overline{DM}$ and $\overline{DBI}$ are disabled then D [67:64] are 1's.

CRC Data Mapping (x8 Configuration, BC4, A2 = 1)

X8	Transfer Burst Bit (BC4, A2=1)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D4	D5	D6	D7	1	1	1	1	CRC0	1
DQ1	D12	D13	D14	D15	1	1	1	1	CRC1	1
DQ2	D20	D21	D22	D23	1	1	1	1	CRC2	1
DQ3	D28	D29	D30	D31	1	1	1	1	CRC3	1
DQ4	D36	D37	D38	D39	1	1	1	1	CRC4	1
DQ5	D44	D45	D46	D47	1	1	1	1	CRC5	1
DQ6	D52	D53	D54	D55	1	1	1	1	CRC6	1
DQ7	D60	D61	D62	D63	1	1	1	1	CRC7	1
$\overline{DM}$ / $\overline{DBI}$	D68	D69	D70	D71	1	1	1	1	1	1

When A2 = 1, data bits D [7:4] are used as inputs for D [3:0], D [15:12] are used as inputs to D [11:8] and so forth for the CRC tree.

The input bits D [71:68] are used if $\overline{DM}$ or $\overline{DBI}$ functions are enabled; if $\overline{DM}$ and $\overline{DBI}$ are disabled then D [71:68] are 1's.

CRC with BC4 Data Bit Mapping for x16 Devices

There are two identical CRC trees for x16 devices, each have CRC tree inputs of 36 bits.

CRC Data Mapping (x16 Configuration, BC4, A2 = 0)

X16	Transfer Burst Bit (BC4, A2=0)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	1	1	1	1	CRC0	1
DQ1	D8	D9	D10	D11	1	1	1	1	CRC1	1
DQ2	D16	D17	D18	D19	1	1	1	1	CRC2	1
DQ3	D24	D25	D26	D27	1	1	1	1	CRC3	1
DQ4	D32	D33	D34	D35	1	1	1	1	CRC4	1
DQ5	D40	D41	D42	D43	1	1	1	1	CRC5	1
DQ6	D48	D49	D50	D51	1	1	1	1	CRC6	1
DQ7	D56	D57	D58	D59	1	1	1	1	CRC7	1
$\overline{\text{LDM}}$ / $\overline{\text{LDBI}}$	D64	D65	D66	D67	1	1	1	1	1	1
DQ8	D72	D73	D74	D75	1	1	1	1	CRC8	1
DQ9	D80	D81	D82	D83	1	1	1	1	CRC9	1
DQ10	D88	D89	D90	D91	1	1	1	1	CRC10	1
DQ11	D96	D97	D98	D99	1	1	1	1	CRC11	1
DQ12	D104	D105	D106	D107	1	1	1	1	CRC12	1
DQ13	D112	D113	D114	D115	1	1	1	1	CRC13	1
DQ14	D120	D121	D122	D123	1	1	1	1	CRC14	1
DQ15	D128	D129	D130	D131	1	1	1	1	CRC15	1
$\overline{\text{UDM}}$ / $\overline{\text{UDBI}}$	D136	D137	D138	D139	1	1	1	1	1	1

The lower CRC tree inputs has 36 bits. The input bits D [67:64] are used if DBI or DM functions are enabled. If DBI and DM are disabled, then D [67:64] are “1”.

The upper CRC tree inputs has 36 bits. The input bits D [139:136] are used if DBI or DM functions are enabled. If DBI and DM are disabled then D[139:136] are “1”.

CRC Data Mapping (x16 Configuration, BC4, A2 = 1)

X16	Transfer Burst Bit (BC4, A2=1)									
	0	1	2	3	4	5	6	7	8	9
DQ0	D4	D5	D6	D7	1	1	1	1	CRC0	1
DQ1	D12	D13	D14	D15	1	1	1	1	CRC1	1
DQ2	D20	D21	D22	D23	1	1	1	1	CRC2	1
DQ3	D28	D29	D30	D31	1	1	1	1	CRC3	1
DQ4	D36	D37	D38	D39	1	1	1	1	CRC4	1
DQ5	D44	D45	D46	D47	1	1	1	1	CRC5	1
DQ6	D52	D53	D54	D55	1	1	1	1	CRC6	1
DQ7	D60	D61	D62	D63	1	1	1	1	CRC7	1
$\overline{\text{LDM}}$ / $\overline{\text{LDBI}}$	D68	D69	D70	D71	1	1	1	1	1	1
DQ8	D76	D77	D78	D79	1	1	1	1	CRC8	1
DQ9	D84	D85	D86	D87	1	1	1	1	CRC9	1
DQ10	D92	D93	D94	D95	1	1	1	1	CRC10	1
DQ11	D100	D101	D102	D103	1	1	1	1	CRC11	1
DQ12	D108	D109	D110	D111	1	1	1	1	CRC12	1
DQ13	D116	D117	D118	D119	1	1	1	1	CRC13	1
DQ14	D124	D125	D126	D127	1	1	1	1	CRC14	1
DQ15	D132	D133	D134	D135	1	1	1	1	CRC15	1
$\overline{\text{UDM}}$ / $\overline{\text{UDBI}}$	D140	D141	D142	D143	1	1	1	1	1	1

When A2 = 1, data bits D [7:4] are used as inputs for D [3:0], D [15:12] are used as inputs to D [11:8] and so forth for the CRC tree.

Input bits D [71:68] are used if $\overline{\text{DM}}$ or $\overline{\text{DBI}}$ functions are enabled and if $\overline{\text{DM}}$ and $\overline{\text{DBI}}$ are disabled then D [71:68] are 1; input bits D [143:140] are used if $\overline{\text{DM}}$ or $\overline{\text{DBI}}$ functions are enabled and if $\overline{\text{DM}}$ and $\overline{\text{DBI}}$ are disabled, then D [143:140] are 1's.

CRC equations for x8 device in BC4 mode with A2=0 are as follows:

CRC[0] = D[69]=1 ^ D[68]=1 ^ D[67] ^ D[66] ^ D[64] ^ D[63]=1 ^ D[60]=1 ^ D[56] ^ D[54]=1 ^ D[53]=1 ^ D[52]=1 ^ D[50] ^ D[49] ^ D[48] ^ D[45]=1 ^ D[43] ^ D[40] ^ D[39]=1 ^ D[35] ^ D[34] ^ D[31]=1^ D[30]=1 ^ D[28]=1 ^ D[23]=1 ^ D[21]=1 ^ D[19] ^ D[18] ^ D[16] ^ D[14]=1 ^ D[12]=1 ^ D[8] ^ D[7]=1 ^ D[6] =1 ^ D[0] ;

CRC[1] = D[70]=1 ^ D[66] ^ D[65] ^ D[63]=1 ^ D[61]=1 ^ D[60]=1 ^ D[57] ^D[56] ^ D[55]=1 ^ D[52]=1 ^ D[51] ^ D[48] ^ D[46]=1 ^ D[45]=1 ^ D[44]=1 ^ D[43] ^ D[41] ^ D[39]=1 ^ D[36]=1 ^ D[34] ^ D[32] ^ D[30]=1 ^ D[29]=1 ^ D[28]=1 ^ D[24] ^ D[23]=1 ^ D[22]=1 ^ D[21]=1 ^ D[20]=1 ^ D[18] ^ D[17] ^ D[16] ^ D[15]=1 ^ D[14]=1 ^ D[13]=1 ^ D[12]=1 ^ D[9] ^ D[6]=1 ^ D[1] ^ D[0];

CRC[2] = D[71]=1 ^ D[69]=1 ^ D[68]=1 ^ D[63]=1 ^ D[62]=1 ^ D[61]=1 ^ D[60]=1 ^ D[58] ^ D[57] ^ D[54]=1 ^ D[50] ^ D[48] ^ D[47]=1 ^ D[46]=1 ^ D[44]=1 ^ D[43] ^ D[42] ^ D[39]=1 ^ D[37]=1 ^ D[34] ^ D[33] ^ D[29]=1 ^ D[28]=1 ^ D[25] ^ D[24] ^ D[22]=1 ^ D[17] ^ D[15]=1 ^ D[13]=1 ^ D[12]=1 ^ D[10] ^ D[8] ^ D[6]=1 ^ D[2] ^ D[1] ^ D[0];

CRC[3] = D[70]=1 ^ D[69]=1 ^ D[64] ^ D[63]=1 ^ D[62]=1 ^ D[61]=1 ^ D[59] ^ D[58] ^ D[55]=1 ^ D[51] ^ D[49] ^ D[48] ^ D[47]=1 ^ D[45]=1 ^ D[44]=1 ^ D[43] ^ D[40] ^ D[38]=1 ^ D[35] ^ D[34] ^ D[30]=1 ^ D[29]=1 ^ D[26] ^ D[25] ^ D[23]=1 ^ D[18] ^ D[16] ^ D[14]=1 ^ D[13]=1 ^ D[11] ^ D[9] ^ D[7]=1 ^ D[3] ^ D[2] ^ D[1];

CRC[4] = D[71]=1 ^ D[70]=1 ^ D[65] ^ D[64] ^ D[63]=1 ^ D[62]=1 ^ D[60]=1 ^ D[59] ^ D[56] ^ D[52]=1 ^ D[50] ^ D[49] ^ D[48] ^ D[46]=1 ^ D[45]=1 ^ D[44]=1 ^ D[41] ^ D[39]=1 ^ D[36]=1 ^ D[35] ^ D[31]=1 ^ D[30]=1 ^ D[27] ^ D[26] ^ D[24] ^ D[19] ^ D[17] ^ D[15]=1 ^ D[14]=1 ^ D[12]=1 ^ D[10] ^ D[8] ^ D[4]=1 ^ D[3] ^ D[2];

CRC[5] = D[71]=1 ^ D[66] ^ D[65] ^ D[64] ^ D[63]=1 ^ D[61]=1 ^ D[60]=1 ^ D[57] ^ D[53]=1 ^ D[51] ^ D[50] ^ D[49] ^ D[47]=1 ^ D[46]=1 ^ D[45]=1 ^ D[42] ^ D[40] ^ D[37]=1 ^ D[36]=1 ^ D[32] ^ D[31]=1 ^ D[28]=1 ^ D[27] ^ D[25] ^ D[20]=1 ^ D[18] ^ D[16] ^ D[15]=1 ^ D[13]=1 ^ D[11] ^ D[9] ^ D[5]=1 ^ D[4]=1 ^ D[3];

CRC[6] = D[67] ^ D[66] ^ D[65] ^ D[64] ^ D[62]=1 ^ D[61]=1 ^ D[58] ^ D[54]=1 ^ D[52]=1 ^ D[51] ^ D[50] ^ D[48] ^ D[47]=1 ^ D[46]=1 ^ D[43] ^ D[41] ^ D[38]=1 ^ D[37]=1 ^ D[33] ^ D[32] ^ D[29]=1 ^ D[28]=1 ^ D[26] ^ D[21]=1 ^ D[19] ^ D[17] ^ D[16] ^ D[14]=1 ^ D[12]=1 ^ D[10] ^ D[6]=1 ^ D[5]=1 ^ D[4]=1;

CRC[7] = D[68]=1 ^ D[67] ^ D[66] ^ D[65] ^ D[63]=1 ^ D[62]=1 ^ D[59] ^ D[55]=1 ^ D[53]=1 ^ D[52]=1 ^ D[51] ^ D[49] ^ D[48] ^ D[47]=1 ^ D[44]=1 ^ D[42] ^ D[39]=1 ^ D[38]=1 ^ D[34] ^ D[33] ^ D[30]=1 ^ D[29]=1 ^ D[27] ^ D[22]=1 ^ D[20]=1 ^ D[18] ^ D[17] ^ D[15] =1^ D[13]=1 ^ D[11] ^ D[7]=1 ^ D[6]=1 ^ D[5]=1;

CRC equations for x8 device in BC4 mode with A2=1 are as follows:

CRC[0] = 1 ^ 1 ^ D[71] ^ D[70] ^ D[68] ^ 1 ^ 1 ^ D[60] ^ 1 ^ 1 ^ 1 ^ D[54] ^ D[53] ^ D[52] ^ 1 ^ D[47] ^ D[44] ^ 1 ^ D[39] ^ D[38] ^ 1^ 1 ^ 1 ^ 1 ^ 1 ^ D[23] ^ D[22] ^ D[20] ^ 1 ^ 1 ^ D[12] ^ 1 ^ 1 ^ D[4] ;

CRC[1] = 1 ^ D[70] ^ D[69] ^ 1 ^ 1 ^ 1 ^ D[61] ^ D[60] ^ 1 ^ 1 ^ D[55] ^ D[52] ^ 1 ^ 1 ^ 1 ^ D[47] ^ D[45] ^ 1 ^ 1 ^ D[38] ^ D[36] ^ 1 ^ 1 ^ 1 ^ D[28] ^ 1 ^ 1 ^ 1 ^ 1 ^ 1 ^ D[22] ^ D[21] ^ D[20] ^1 ^ 1 ^1 ^ 1 ^ D[13] ^ 1 ^ D[5] ^ D[4];

CRC[2] = 1 ^ 1 ^ 1 ^1 ^1 ^ 1 ^ 1 ^ D[62] ^ D[61] ^ 1 ^ D[54] ^ D[52] ^ 1 ^ 1 ^ 1 ^ D[47] ^ D[46] ^ 1 ^ 1 ^ D[38] ^ D[37] ^ 1 ^ 1 ^ D[29] ^ D[28] ^ 1 ^ D[21] ^ 1 ^ 1 ^ 1 ^ D[14] ^ D12] ^1 ^ D[6] ^ D[5] ^ D[4];

CRC[3] = 1 ^ 1 ^ D[68] ^ 1 ^ 1 ^ 1 ^ D[63] ^ D[62] ^ 1 ^ D[55] ^ D[53] ^ D[52] ^ 1 ^ 1 ^ 1 ^ D[47] ^ D[44] ^ 1 ^ D[39] ^ D[38] ^ 1 ^ 1 ^ D[30] ^ D[29] ^ 1 ^ D[22] ^ D[20] ^ 1 ^ 1 ^ D[15] ^ D[13] ^ 1 ^ D[7] ^ D[6] ^ D[5];

CRC[4] = 1 ^1 ^ D[69] ^ D[68] ^ 1 ^ 1 ^ 1 ^ D[63] ^ D[60] ^ 1 ^ D[54] ^ D[53] ^ D[52] ^ 1 ^1 ^ 1 ^ D[45] ^ 1 ^ 1 ^ D[39] ^1 ^ 1 ^ D[31] ^ D[30] ^ D[28] ^ D[23] ^ D[21] ^ 1 ^ 1 ^ 1 ^ D[14] ^ D[12] ^ 1 ^ D[7] ^ D[6];

CRC[5] = 1 ^ D[70] ^ D[69] ^ D[68] ^ 1 ^ 1 ^ 1 ^ D[61] ^ 1 ^ D[55] ^ D[54] ^ D[53] ^ 1 ^ 1 ^ 1 ^ D[46] ^ D[44] ^ 1 ^ 1 ^ D[36] ^ 1 ^ 1 ^ D[31] ^ D[29] ^ 1 ^ D[22] ^ D[20] ^ 1 ^ 1 ^ D[15] ^ D[13] ^ 1 ^ 1 ^ D[7];

CRC[6] = D[71] ^ D[70] ^ D[69] ^ D[68] ^ 1 ^ 1 ^ D[62] ^ 1 ^ 1 ^ D[55] ^ D[54] ^ D[52] ^ 1 ^1 ^ D[47] ^ D[45] ^ 1 ^ 1 ^ D[37] ^ D[36] ^1 ^ 1 ^ D[30] ^ 1 ^ D[23] ^ D[21] ^ D[20] ^ 1 ^ 1 ^ D[14] ^ 1 ^ 1 ^ 1;

CRC[7] = 1 ^ D[71] ^ D[70] ^ D[69] ^ 1 ^ 1 ^ D[63] ^ 1 ^ 1 ^ 1 ^ D[55] ^ D[53] ^ D[52] ^ 1 ^ 1 ^ D[46] ^ 1 ^ 1 ^ D[38] ^ D[37] ^ 1 ^ 1 ^ D[31] ^ 1 ^ 1 ^ D[22] ^ D[21] ^ 1^ 1 ^ D[15] ^ 1 ^ 1 ^ 1;

Simultaneous DM and CRC Functionality

When both DM and Write CRC are enabled in the DRAM mode register, the DRAM calculates CRC before sending the write data into the array. If there is a CRC error, the DRAM blocks the write operation and discards the data. For a x16, when the DRAM detects an error in CRC tree, DDR4 DRAMs may mask all DQs or half the DQs depending upon the specific vendor implementation behavior. Both implementations are valid. For the DDR4 DRAMs that masking half the DQs, DQ0 through DQ7 will be masked if the lower byte. CRC tree had the error and DQ8 through DQ15 will be masked if the upper byte CRC tree had the error.

Simultaneous MPR Write, Per DRAM Addressability and CRC Functionality

The following combination of DDR4 features are prohibited for simultaneous operation:

(1) MPR Write and Write CRC (Note: MPR Write is via Address pins)

(2) Per DRAM Addressability and Write CRC (Note : Only MRS are allowed during PDA and also DQ0 is used for PDA detection)

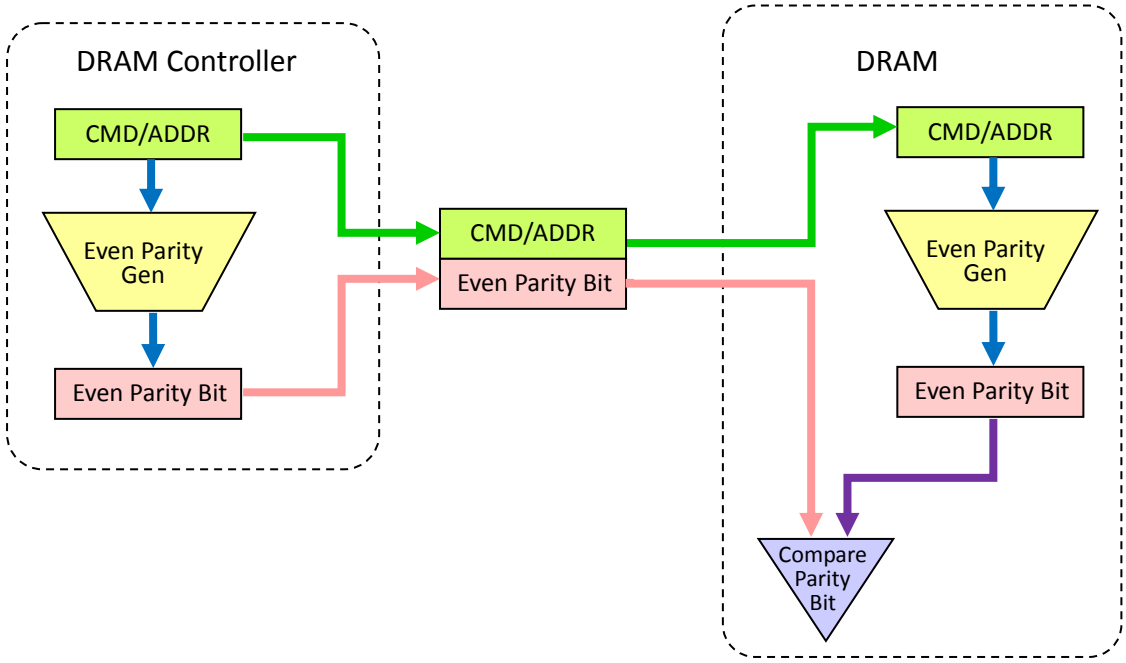
Command/Address Parity (CAP)

[A2:A0] of MR5 are defined to enable or disable C/A Parity in the DRAM. The default state of the C/A Parity bits is disabled. If C/A parity is enabled by programming a non-zero value to C/A Parity Latency in the mode register (the Parity Error bit must be set to zero when enabling C/A any Parity mode), then the DRAM has to ensure that there is no parity error before executing the command. The additional delay for executing the commands versus a parity disabled mode is programmed in the mode register (MR5, A2:A0) when C/A Parity is enabled (PL: Parity Latency) and is applied to commands that are latched via the rising edge of CK when $\overline{CS}$ is low. The command is held for the time of the Parity Latency before it is executed inside the device. This means that issuing timing of internal command is determined with PL. When C/A Parity is enabled, only DES is allowed between valid commands to prevent DRAM from any malfunctioning. CA Parity Mode is supported when DLL-on Mode is enabled, use of CA Parity Mode when DLL-off Mode is enabled is not allowed.

CA Parity signal covers $\overline{ACT}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and the address bus, including bank address and bank group bits, the control signals CKE, ODT, and $\overline{CS}$ are not covered. For example, for a 4 Gbit x4 monolithic device, parity is computed across BG [1:0], BA [1:0], A16/$\overline{RAS}$, A15/$\overline{CAS}$, A14/$\overline{WE}$, A [13:0], and $\overline{ACT}$. The DRAM treats any unused address pins internally as zeros; for example, if a common die has stacked pins but the device is used in a monolithic application, then the address pins used for stacking should internally be treated as 0's.

The convention for parity is even parity; for example, valid parity is defined as an even number of ones across the inputs used for parity computation combined with the parity signal. In other words, the parity bit is chosen so that the total number of "1's" in the transmitted signal, including the parity bit is even.

Command/Address Parity Operation



If a DRAM device detects a CA Parity error in any command qualified by $\overline{CS}$, then it will perform the following steps:

1. Ignore the erroneous command. Commands in MAX NnCK window (tPAR_UNKNOWN) prior to the erroneous command are not guaranteed to be executed. When a READ command in this NnCK window is not executed, the device does not activate DQS outputs.
2. Log the error by storing the erroneous command and address bits in the MPR Page 1 error log.
3. Set the parity error status bit in the mode register to "1". The Parity Error Status bit must be set before the $\overline{ALERT}$ signal is released by the DRAM (i.e. tPAR_ALERT_ON + tPAR_ALERT_PW(min)).
4. Assert the $\overline{ALERT}$ signal to the host ($\overline{ALERT}$ is active LOW) within tPAR_ALERT_ON time.
5. Wait for all in-progress commands to complete. These commands were received tPAR_UNKOWN before the erroneous command.

If a parity error occurs on a command issued between the tXS_Fast and tXS window after self-refresh exit, then the DRAM may delay the de-assertion of $\overline{ALERT}$ signal as a result of any internal on going refresh. (See CA Parity Error Checking - SRX)

6. Wait for tRAS_min before closing all the open pages. The DRAM is not executing any commands during the window defined by (tPAR_ALERT_ON +tPAR_ALERT_PW).
7. After tPAR_ALERT_PW_min has been satisfied, the device may de-assert $\overline{ALERT}$.
8. After the DRAM has returned to a known pre-charged state it may de-assert $\overline{ALERT}$.
9. After (tPAR_ALERT_ON + tPAR_ALERT_PW), the DRAM is ready to accept commands for normal operation. Parity latency will be in effect, however, parity checking will not resume until the memory controller has cleared the Parity Error Status bit by writing a '0' (the DRAM will execute any erroneous commands until the bit is cleared).
10. It is possible that the DRAM might have ignored a refresh command during the (tPAR_ALERT_ON + tPAR_ALERT_PW) window or the refresh command is the first erroneous frame so it is recommended that the controller issues extra refresh cycles as needed.

11. The Parity Error Status bit may be read any time after (tPAR_ALERT_ON + tPAR_ALERT_PW) to determine which DRAM had the error. The DRAM maintains the Error Log for the first erroneous command until the Parity Error Status bit is reset to '0'.

Mode Register for C/A Parity Error is defined as follows. C/A Parity Latency bits are write only, Parity Error Status bit is read/write and error logs are read only bits. The controller can only program the Parity Error Status bit to '0'. If the controller illegally attempts to write a '1' to the Parity Error Status bit, the DRAM does not guarantee that parity will be checked. The DRAM may opt to block the controller from writing a '1' to the Parity Error Status bit.

DDR4 SDRAM supports MR bit for 'Persistent Parity Error Mode'. This mode is enabled by setting MR5 A9=High and when it is enabled, DRAM resumes checking CA Parity after the $\overline{\text{ALERT}}$ is deasserted, even if Parity Error Status bit is set as High. If multiple errors occur before the Error Status bit is cleared the Error log in MPR page 1 should be treated as 'Don't Care'. In 'Persistent Parity Error Mode' the $\overline{\text{ALERT}}$ pulse will be asserted and deasserted by the DRAM as defined with the min. and max. value for tPAR_ALERT_PW. The controller must issue DESELECT commands once it detects the $\overline{\text{ALERT}}$. signal, this response time is defined as tPAR_ALERT_RSP.

The following figure captures the flow of events on the C/A bus and the $\overline{\text{ALERT}}$ signal.

Mode Registers for C/A Parity

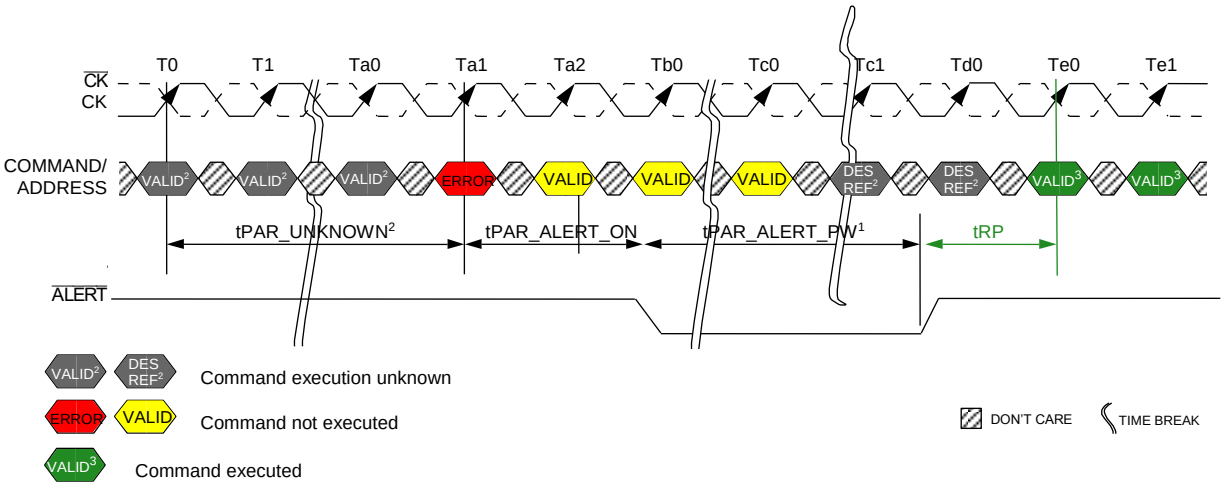
C/A Parity Latency MR5[2:0][1]	Speed bins	C/A Parity Error Status MR5 A[4]	Parity Persistent Mode MR5 A[9]	Errant C/A Frame
000= Disabled	NA	0=clear	0 = Disabled	$\overline{\text{ACT}}$, PAR, BG1, BG0, BA0, BA1, A16/$\overline{\text{RAS}}$, A15/$\overline{\text{CAS}}$, A14/$\overline{\text{WE}}$, A[17,13:0]
001= 4 Clocks	1600,1866,2133			
010= 5 Clocks	2400	1=Error	1 = Enabled	
011= 6 Clocks	RFU			
100= 8 Clocks	RFU			

NOTE 1 Parity latency is applied to all commands.

NOTE 2 Parity latency can be changed only from a CA parity disabled state; for example, a direct change from PL = 3 to PL = 4 is not allowed. The correct sequence is PL = 3 to disabled to PL = 4.

NOTE 3 Parity Latency is applied to write and read latency. Write Latency = AL+CWL+PL. Read Latency = AL+CL+PL.

Normal CA Parity Error Checking Operation

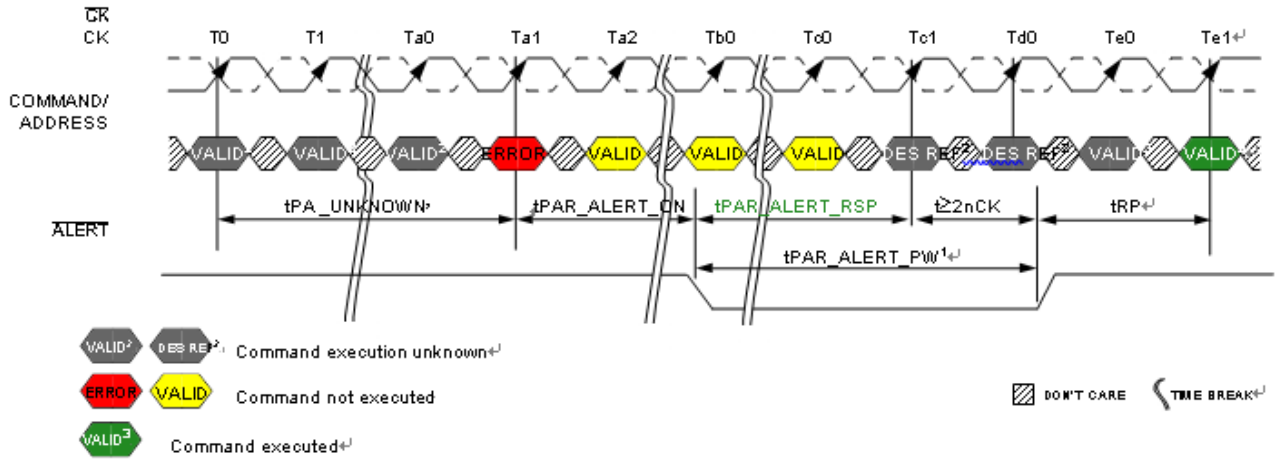


NOTE 1 DRAM is emptying queues. Precharge all and parity checking off until Parity Error Status bit cleared.

NOTE 2 Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.

NOTE 3 Normal operation with parity latency (CA Parity Persistent Error Mode disabled). Parity checking off until Parity Error Status bit cleared.

Persistent CA Parity Error Checking Operation

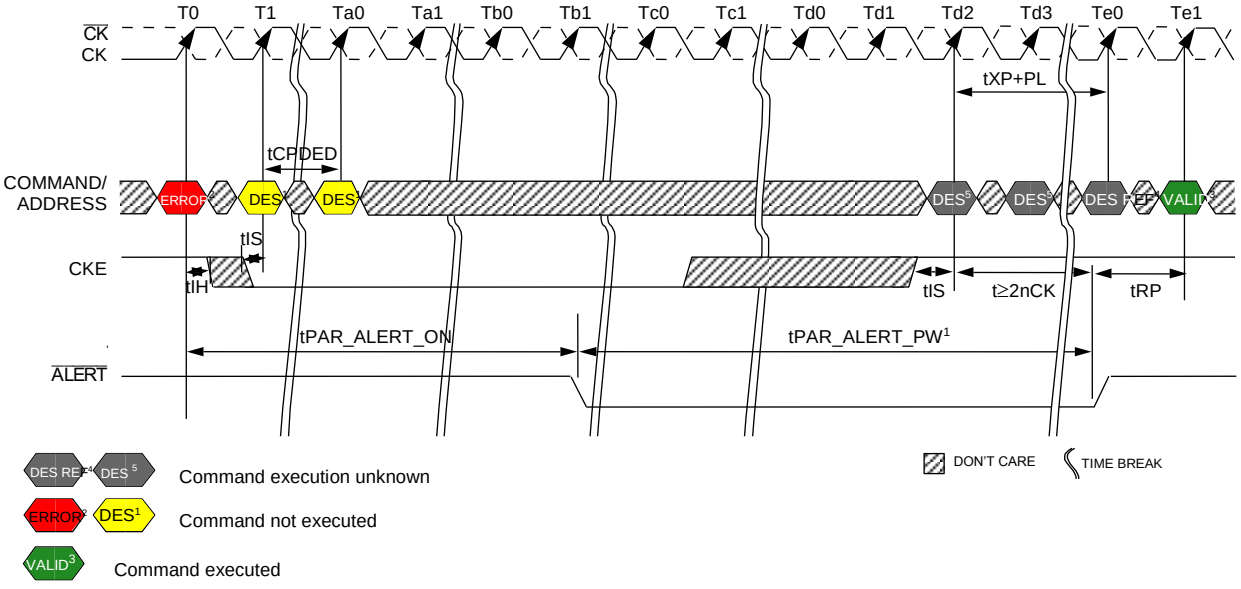


NOTE 1 DRAM is emptying queues. Precharge all and parity check re-enable finished by tPAR_ALERT_PW.

NOTE 2 Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.

NOTE 3 Normal operation with parity latency and parity checking (CA Parity Persistent Error Mode enabled).

CA Parity Error Checking - PDE/PDX



NOTE 1 Deselect command only allowed.

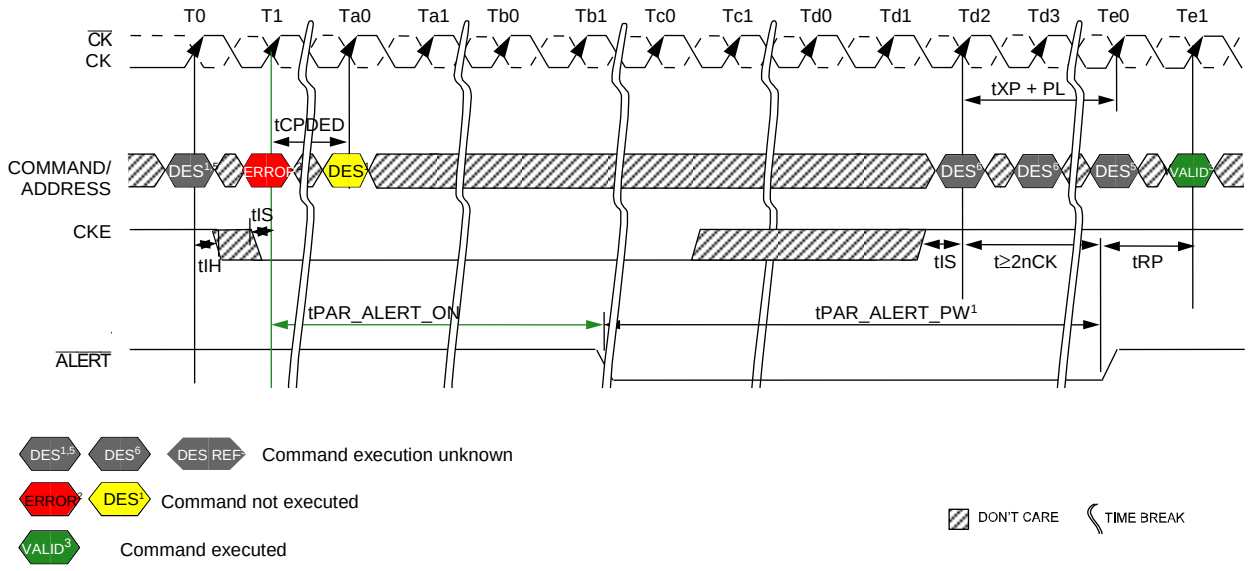
NOTE 2 Error could be Precharge or Activate.

NOTE 3 Normal operation with parity latency (CA Parity Persistent Error Mode disabled). Parity checking is off until Parity Error Status bit cleared.

NOTE 4 Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.

NOTE 5 Deselect command only allowed; CKE may go high prior to Td2 as long as DES commands are issued.

CA Parity Error Checking - SRE Attempt



NOTE 1 Deselect command only allowed.

NOTE 2 Self Refresh command error. DRAM masks the intended SRE command and enters Precharge Power Down.

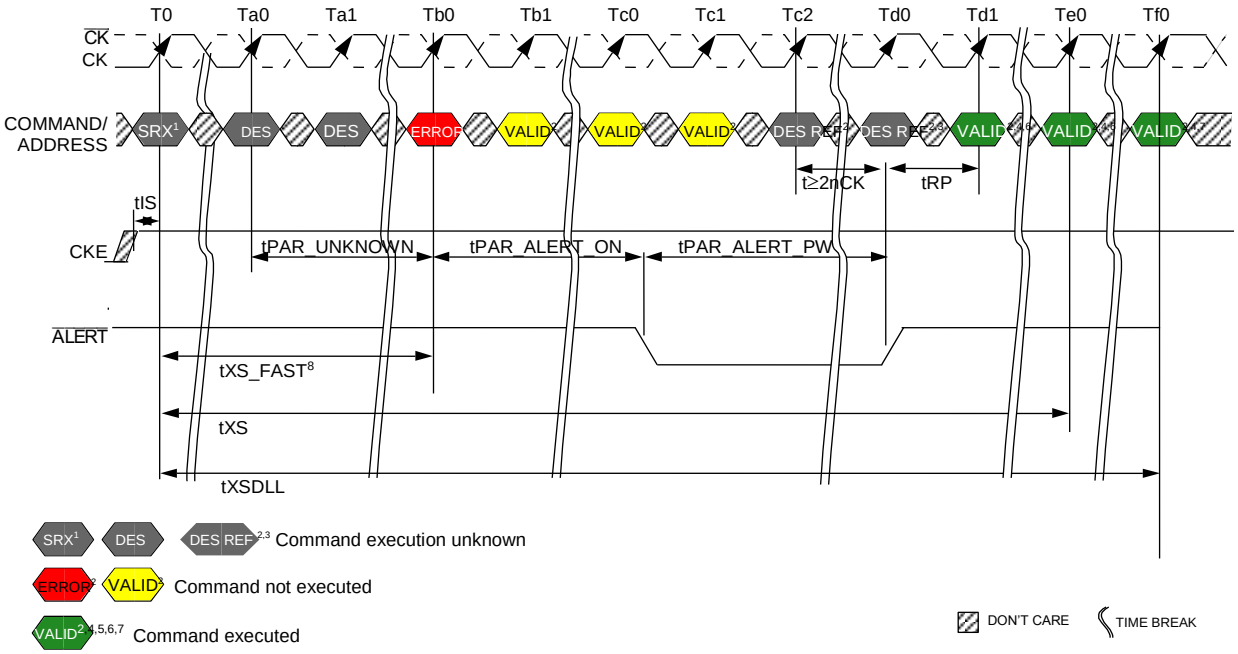
NOTE 3 Normal operation with parity latency (CA Parity Persistent Error Mode disabled). Parity checking is off until Parity Error Status bit cleared.

NOTE 4 Controller cannot disable clock until it has been able to have detected a possible C/A Parity error.

NOTE 5 Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.

NOTE 6 Deselect command only allowed; CKE may go high prior to Tc2 as long as DES commands are issued.

CA Parity Error Checking - SRX



NOTE 1 Self Refresh Abort = Disable: MR4 A[9] = 0.

NOTE 2 Input commands are bounded by tXSDLL, tXS, tXS_ABORT and tXS_FAST timing.

NOTE 3 Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.

NOTE 4 Normal operation with parity latency (CA Parity Persistent Error Mode disabled). Parity checking off until Parity Error Status bit cleared.

NOTE 5 Only MRS (limited to those described in the Self-Refresh Operation section), ZQCS, or ZQCL command allowed

NOTE 6 Valid commands not requiring a locked DLL.

NOTE 7 Valid commands requiring a locked DLL.

NOTE 8 This figure shows the case from which the error occurred after tXS_FAST. An error may also occur after tXS_ABORT and tXS.

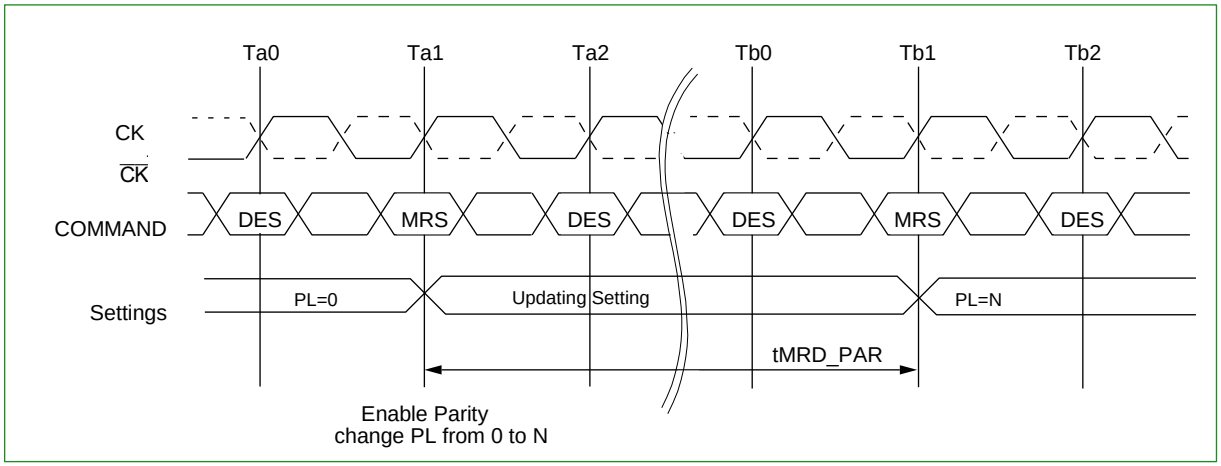
Command/Address parity entry and exit timings

When in CA Parity mode, including entering and exiting CA Parity mode, users must wait tMRD_PAR before issuing another MRS command, and wait tMOD_PAR before any other commands.

tMOD_PAR = tMOD + PL
tMRD_PAR = tMOD + PL

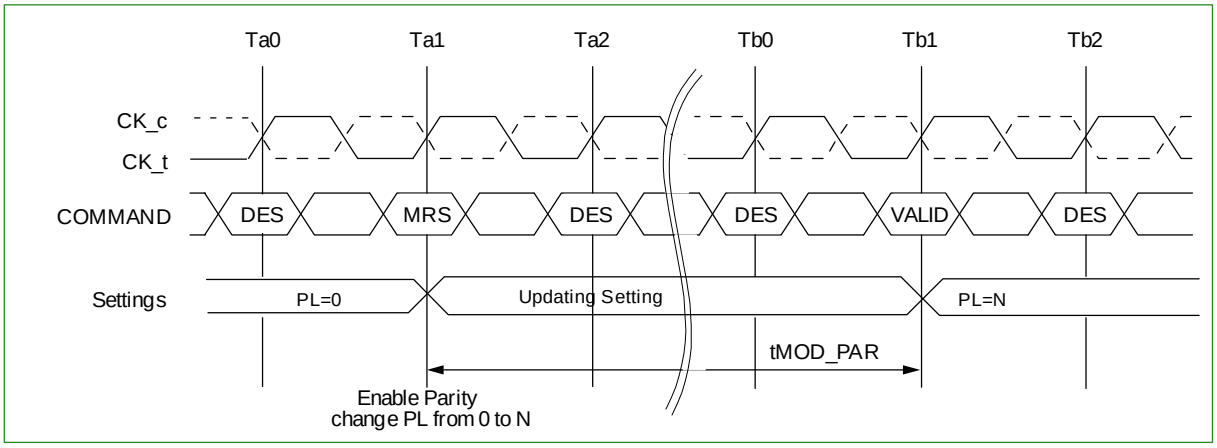
For CA parity entry, PL in the equations above is the parity latency programmed with the MRS command entering CA parity mode.
For CA parity exit, PL in the equations above is the programmed parity latency prior to the MRS command exiting CA parity mode.

Parity Entry Timing Example - tMRD_PAR



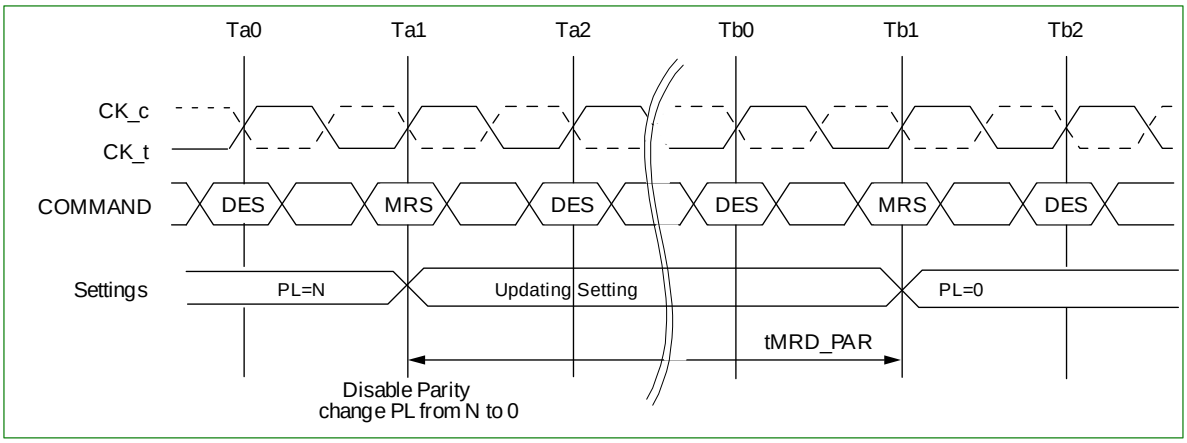
NOTE 1 tMRD_PAR = tMOD + N; where N is the programmed parity latency with the MRS command entering CA parity mode.
NOTE 2 Parity check is not available at Ta1 of MRS command due to PL=0 being valid.
NOTE 3 In case parity error happens at Tb1 of MRS command, tPAR_ALERT_ON is 'N[nCK] + 6[ns]'.

Parity Entry Timing Example - tMOD_PAR



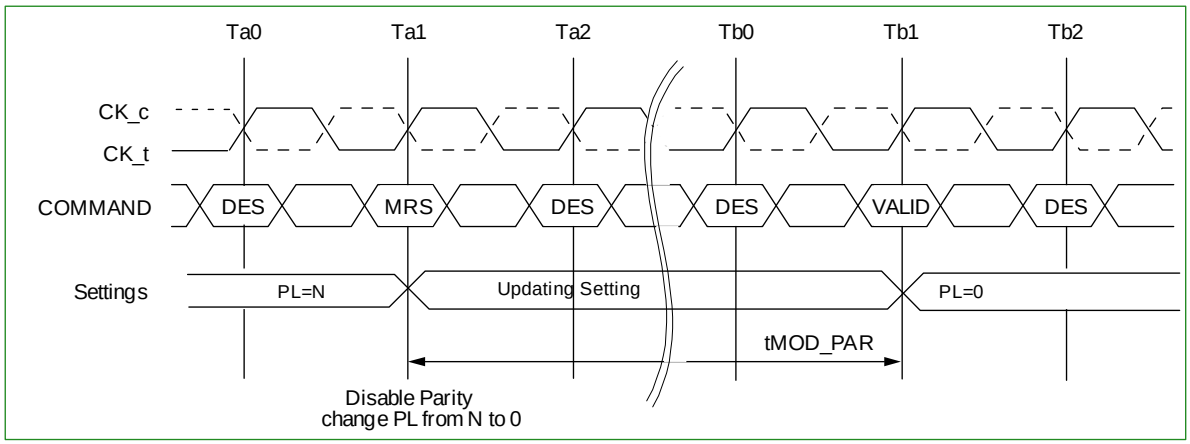
NOTE 1 tMOD_PAR = tMOD + N; where N is the programmed parity latency with the MRS command entering CA parity mode.
NOTE 2 Parity check is not available at Ta1 of MRS command due to PL=0 being valid.
NOTE 3 In case parity error happens at Tb1 of VALID command, tPAR_ALERT_ON is 'N[nCK] + 6[ns]'.

Parity Exit Timing Example - tMRD_PAR



NOTE 1 tMRD_PAR = tMOD + N; where N is the programmed parity latency prior to the MRS command exiting CA parity mode.
NOTE 2 In case parity error happens at Ta1 of MRS command, tPAR_ALERT_ON is 'N[nCK] + 6[ns]'.
NOTE 3 Parity check is not available at Tb1 of MRS command due to disabling parity mode.

Parity Exit Timing Example - tMOD_PAR



NOTE 1 tMOD_PAR = tMOD + N; where N is the programmed parity latency prior to the MRS command exiting CA parity mode.
NOTE 2 In case parity error happens at Ta1 of MRS command, tPAR_ALERT_ON is 'N[nCK] + 6[ns]'.
NOTE 3 Parity check is not available at Tb1 of VALID command due to disabling parity mode.

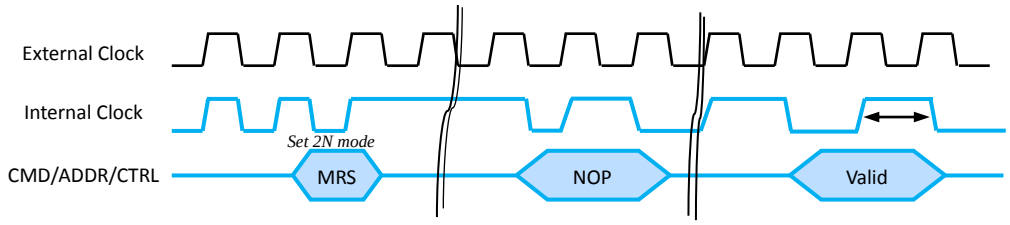
CA Parity Error Log Readout

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BA[1:0] =0:1	00=MPR0	A7	A6	A5	A4	A3	A2	A1	A0
	01=MPR1	$\overline{CAS}$ /A15	$\overline{WE}$/A14	A13	A12	A11	A10	A9	A8
	10=MPR2	PAR	$\overline{ACT}$	BG1	BG0	BA1	BA0	A17	$\overline{RAS}$/A16
	11=MPR3	CRC Error Status	CA Parity Error Status	CA Parity Latency			C2	C1	C0

NOTE 1 MPR used for CA parity error log readout is enabled by setting A[2] in MR3
NOTE 2 For higher density of DRAM, where A [17] is not used, MPR2[1] should be treated as don't care.
NOTE 3 If a device is used in monolithic application, where C [2:0] are not used, then MPR3[2:0] should be treated as don't care.

Control Gear-down Mode

The following description represents the sequence for the gear-down mode which is specified with MR3:A3. This mode is allowed just during initialization and self refresh exit. The DDR4 SDRAM defaults in 1/2 rate (1N) clock mode and utilizes a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines $\overline{CS}$, CKE, and ODT when in 1/4 rate (2N) mode. For operation in 1/2 rate mode, MRS command or sync pulse is not required.



General sequence for operation in geardown during initialization

1. DRAM defaults to a 1/2 rate (1N mode) internal clock at power-up/reset.
2. Assertion of reset.
3. Assertion of CKE enables the DRAM.
4. MRS is accessed with a low frequency NxtCK MRS Gear-down CMD (set MR3:A3 to 1). (NtCK static MRS command is qualified by 1N $\overline{CS}$.)
5. DRAM controller sends a 1N sync pulse with a low frequency N*tCK NOP CMD; tSYNC_GEAR is an even number of clocks; sync pulse on even clock boundary from MRS CMD.
6. Initialization sequence, including the expiration of tDLLK and tZQinit, starts in 2N mode after tCMD_GEAR from 1N Sync Pulse.

General sequence for operation in gear-down after self refresh exit

1. DRAM reset to 1N mode during self refresh
2. MRS is accessed with a low frequency N*tck MRS gear-down CMD (set MR3:A3 to 1)

Ntck static MRS command qualified by 1N $\overline{CS}$ which meets tXS or tXS_Abort

Only Refresh command is allowed to be issued to DRAM before Ntck static MRS command

3. DRAM controller sends 1N sync pulse with a low frequency N*tck NOP CMD. tSYNC_GEAR is an even number of clocks. Sync pulse is on even clock boundary from MRS CMD.
4. Valid command not requiring locked DLL is available in 2N mode after tCMD_GEAR from 1N Sync Pulse.
5. Valid command requiring locked DLL is available in 2N mode after tDLLK from 1N Sync Pulse

If operation is 1/2 rate(1N) mode after self refresh, no N*tCK MRS command or sync pulse is required during self refresh exit. The min exit delay is tXS, or tXS_Abort to the first valid command.

The DRAM may be changed from 1/4 rate (2N) to 1/2 rate (1N) by entering Self Refresh Mode, which will reset to 1N automatically. Changing from 1/4 (2N) to 1/2 rate (1 N) by any other means, including setting MR3[A3] from 1 to 0, can result in loss of data and operation of the DRAM uncertain.

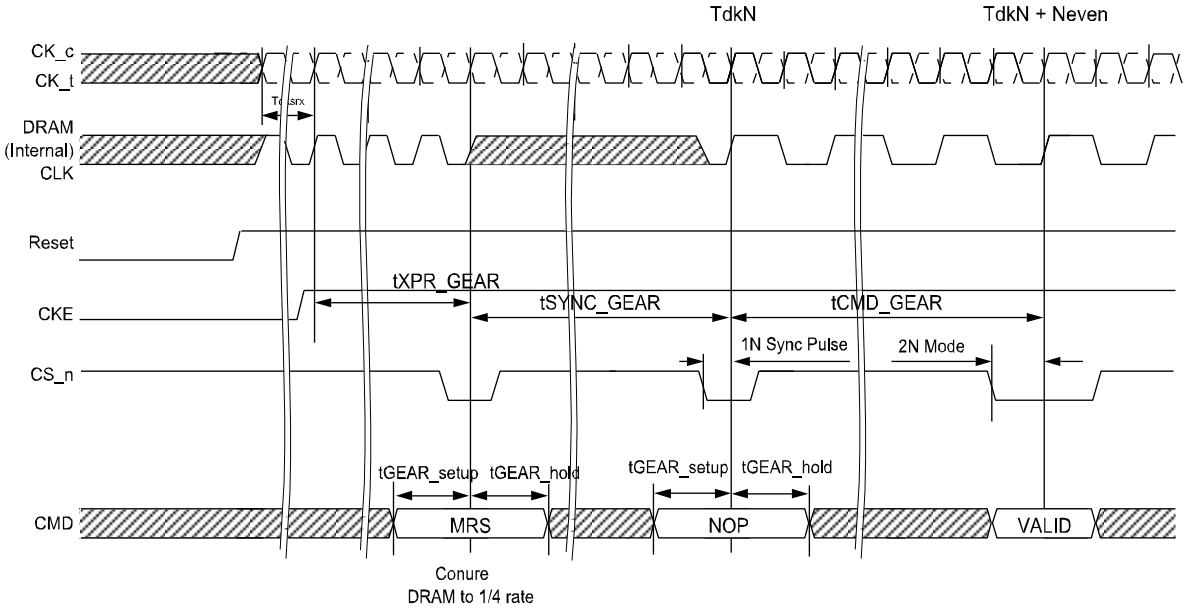
When operating in 1/4 rate Gear-down Mode, the following MR settings apply:

- CAS Latency (MR0 A [6:4,2]): Even number of clocks
- Write Recovery and Read to Precharge (MR0 A [11:9]): Even number of clocks
- Additive Latency (MR1 A [4:3]): 0, CL -2

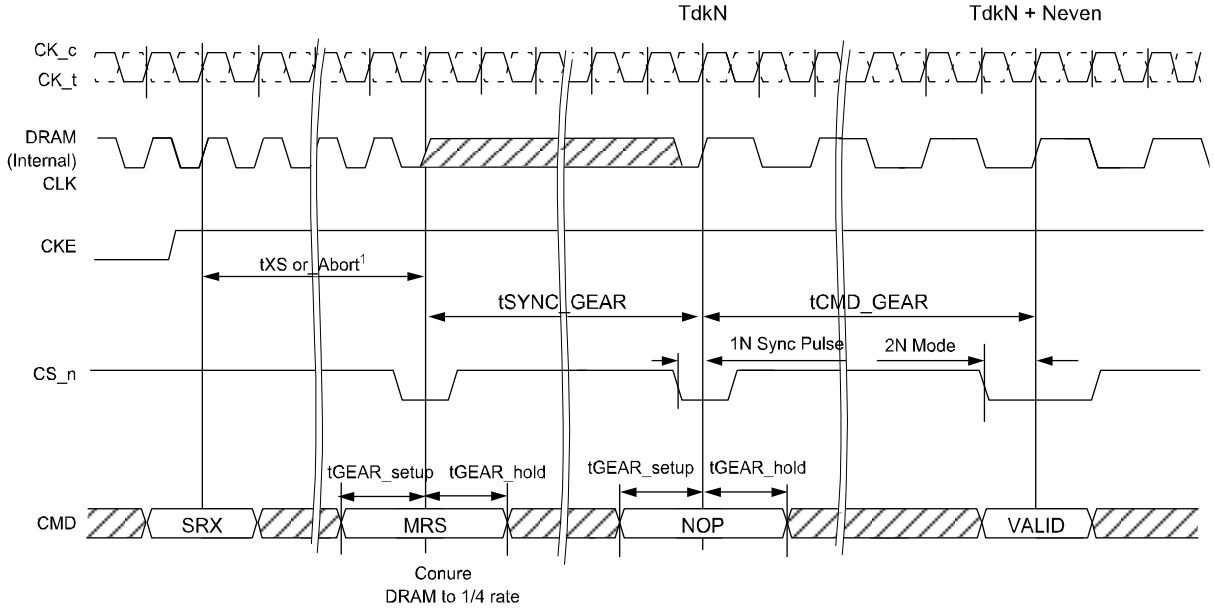
- CAS Write Latency (MR2 A [5:3]): Even number of clocks
- $\overline{CS}$ to Command/Address Latency Mode (MR4 [8:6]): Even number of clocks
- CA Parity Latency Mode (MR5 A [2:0]): Even number of clocks

CAL or CA parity mode must be disabled prior to Gear down MRS command. They can be enabled again after tSYNC_GEAR and tCMD_GEAR periods are satisfied.

Gear down (2N) mode entry sequence during initialization

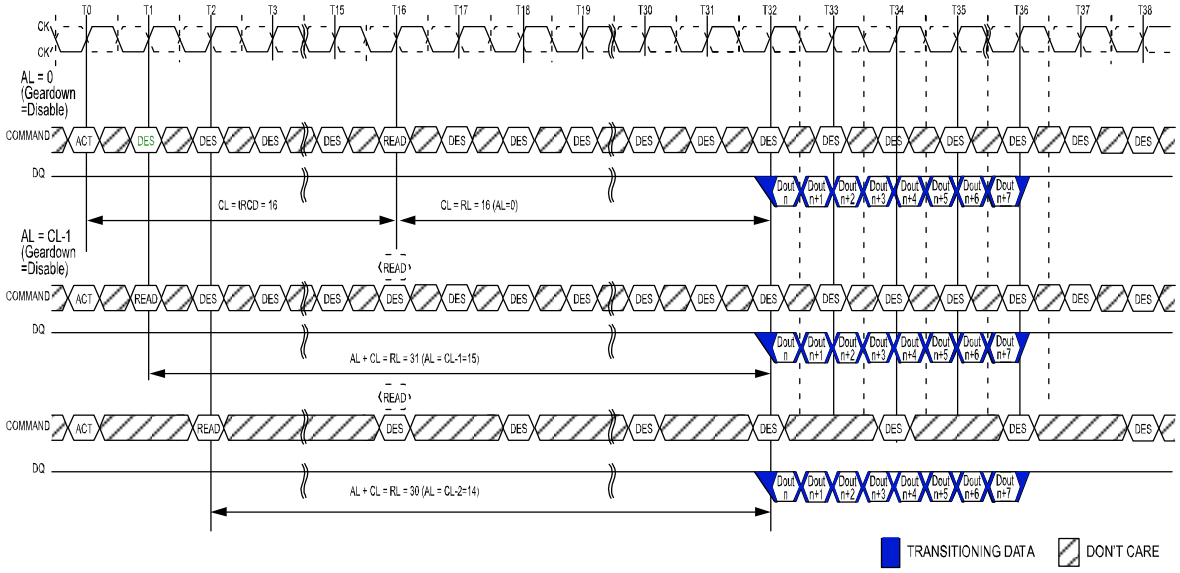


Clock Mode Change After Exiting Self Refresh



NOTE 1 CKE High Assert to Gear Down Enable Time (tXS, tXS_Abort) depend on MR setting. A correspondence of tXS/tXS_Abort and MR Setting is as follows. - MR4[A9] = 0: tXS - MR4[A9] = 1: tXS_Abort
NOTE 2 Command not requiring locked DLL
NOTE 3 Only DES is allowed during tSYNC_GEAR

Comparison Timing Diagram Between Gear-down Disable and Enable



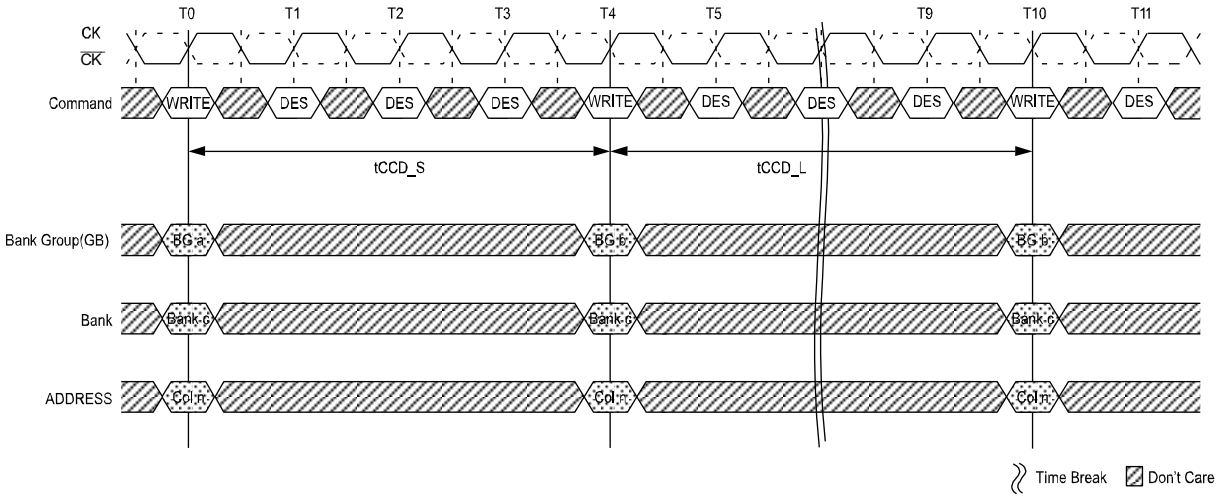
NOTE 1 BL=8, tRCD=CL=16

NOTE 2 DOUT n = data-out from column n. s are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable.

DDR4 Key Core Timing

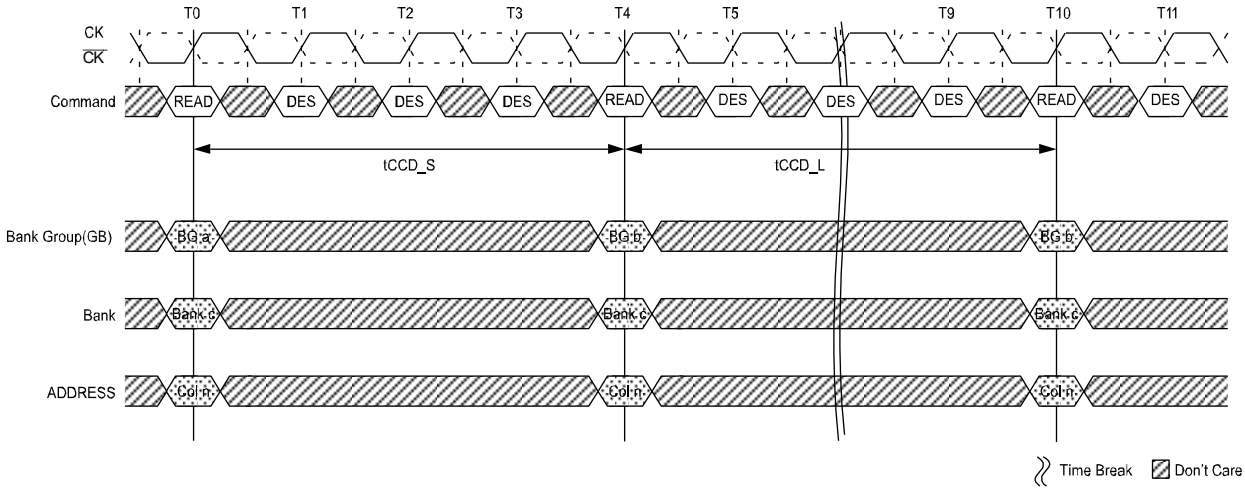
tCCD Timing (WRITE to WRITE Example)



NOTE 1 tCCD_S; $\overline{CAS}$-to-$\overline{CAS}$ delay (short). Applies to consecutive $\overline{CAS}$ to different bank groups (i.e., T0 to T4).

NOTE 2 tCCD_L; $\overline{CAS}$-to-$\overline{CAS}$ delay (long). Applies to consecutive $\overline{CAS}$ to the same bank group (i.e., T4 to T10).

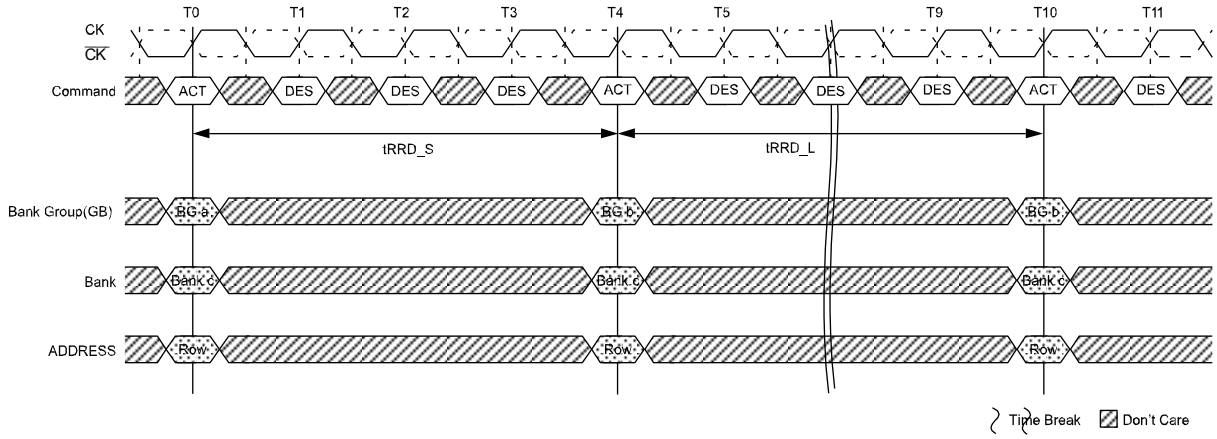
tCCD Timing (READ to READ Example)



NOTE 1 tCCD_S; $\overline{CAS}$-to-$\overline{CAS}$ delay (short). Applies to consecutive $\overline{CAS}$ to different bank groups (i.e., T0 to T4).

NOTE 2 tCCD_L; $\overline{CAS}$-to-$\overline{CAS}$ delay (long). Applies to consecutive $\overline{CAS}$ to the same bank group (i.e., T4 to T10).

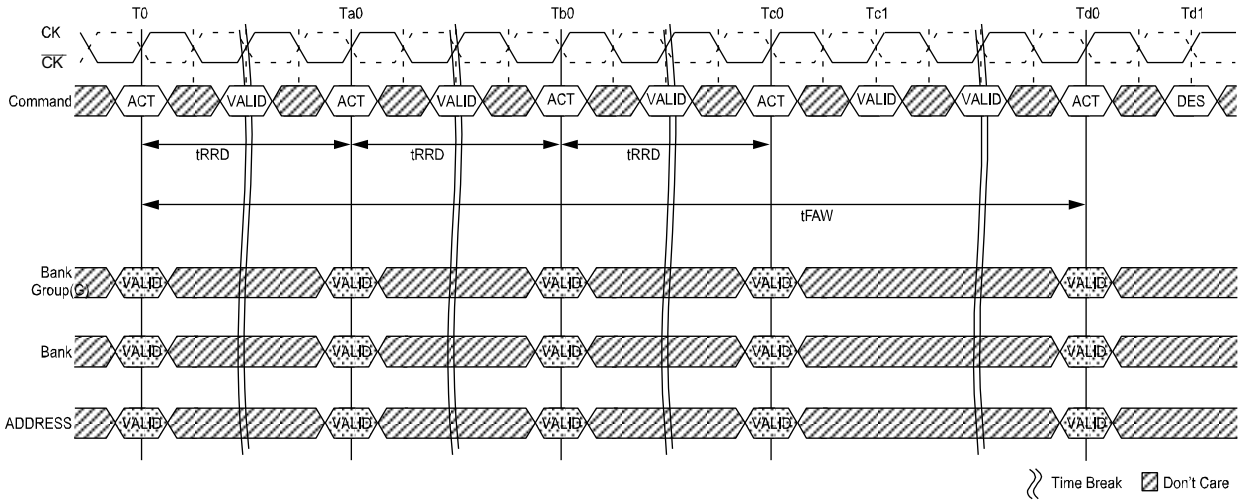
tRRD Timing



NOTE 1 tRRD_S; ACTIVATE-to-ACTIVATE command period (short); applies to consecutive ACTIVATE commands to different bank groups (i.e., T0 and T4).

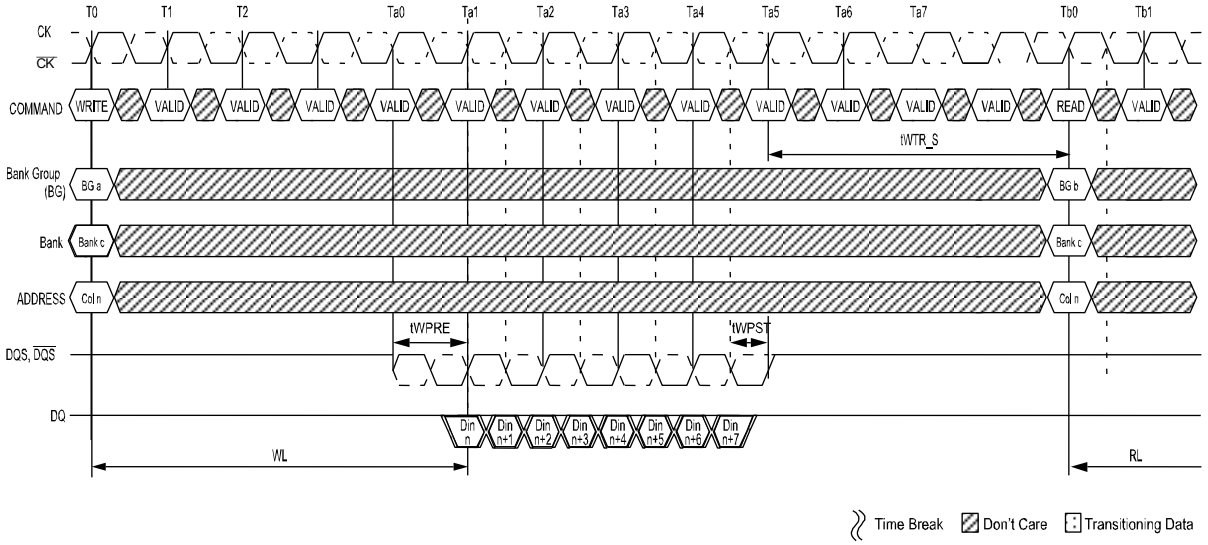
NOTE 2 tRRD_L; ACTIVATE-to-ACTIVATE command period (long); applies to consecutive ACTIVATE commands to the different banks in the same bank group (i.e., T4 and T10).

tFAW Timing



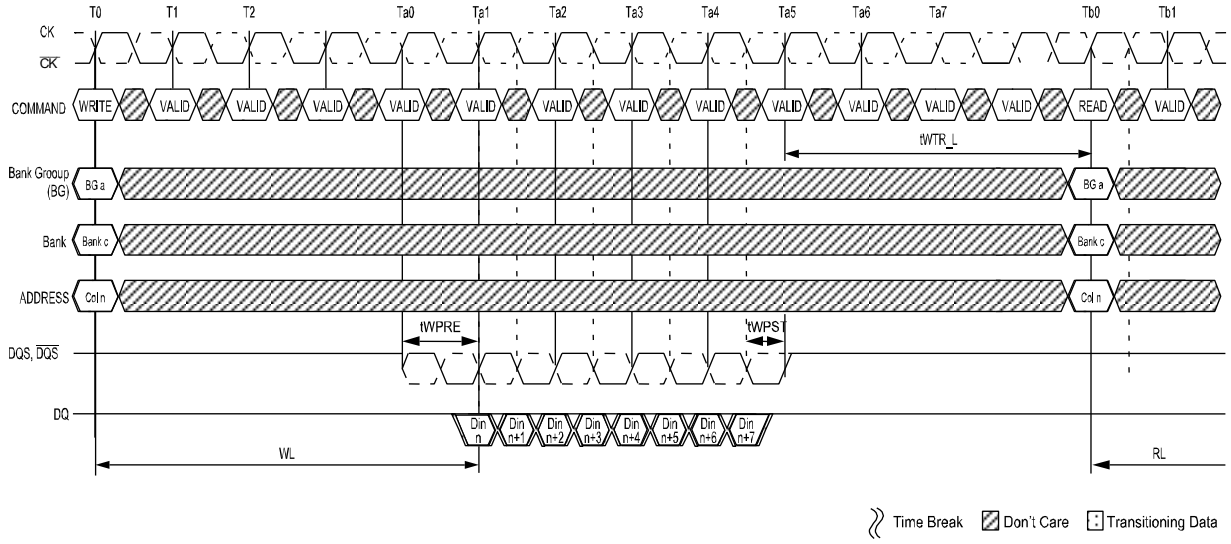
NOTE 1 tFAW : Four activate window

tWTR_S Timing (WRITE-to-READ, Different Bank Group, CRC and DM Disabled)



NOTE 1 tWTR_S: Delay from start of internal write transaction to internal READ command to a different bank group. When AL is non-zero, the external read command at Tb0 can be pulled in by AL.

tWTR_L Timing (WRITE-to-READ, Same Bank Group, CRC and DM Disabled)



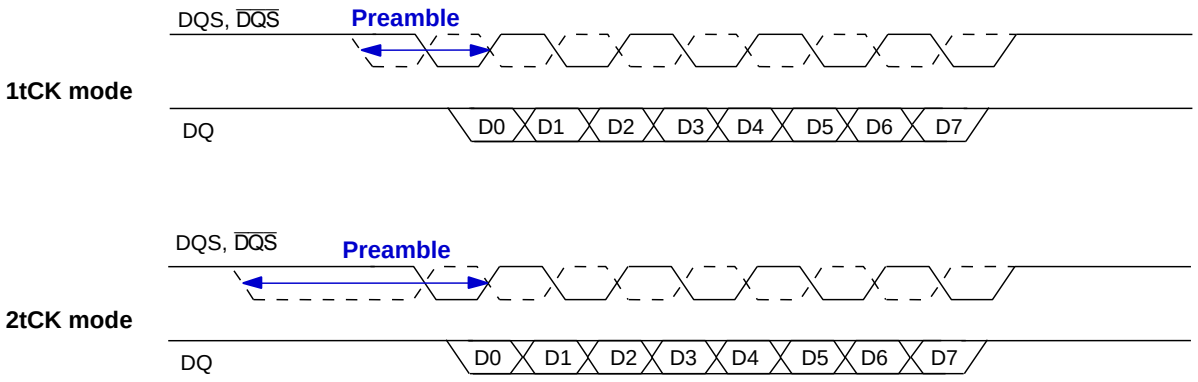
NOTE 1 tWTR_L: delay from start of internal write transaction to internal READ command to the same bank group. When AL is non-zero, the external read command at Tb0 can be pulled in by AL.

Programmable Preamble

The DQS preamble can be programmed to one or the other of 1 tCK and 2 tCK preamble; selectable via MRS (MR4 A [12:11]). The 1 tCK preamble applies to all Speed-Grade and The 2 tCK preamble is valid for DDR4-2400/2666 Speed bin Tables.

Write Preamble

The 1 tCK or 2tCK Write Preamble is selected via MR4 [A12]. MR4 A [12] = 0 selects 1 tCK Write Preamble Mode while MR4 A [12] = 1 selects 2 tCK Write Preamble Mode, examples in the figures below.

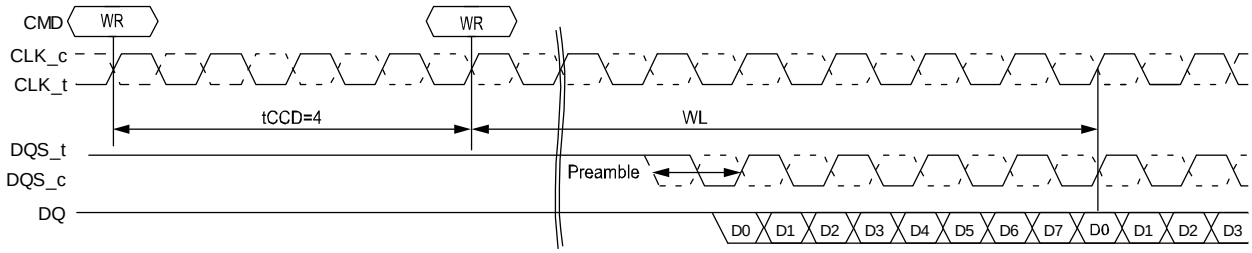


When operating in 2 tCK Write preamble mode in MR2 CWL (CAS Write Latency), CWL of 1st Set needs to be incremented by 2 nCK and CWL of 2nd Set does not need increment of it. tWTR must be increased by one clock cycle from the tWTR required in the applicable speed bin table. WR must be programmed to a value one or two clock cycle(s), depending on available settings, greater than the WR setting required per the applicable speed bin table.

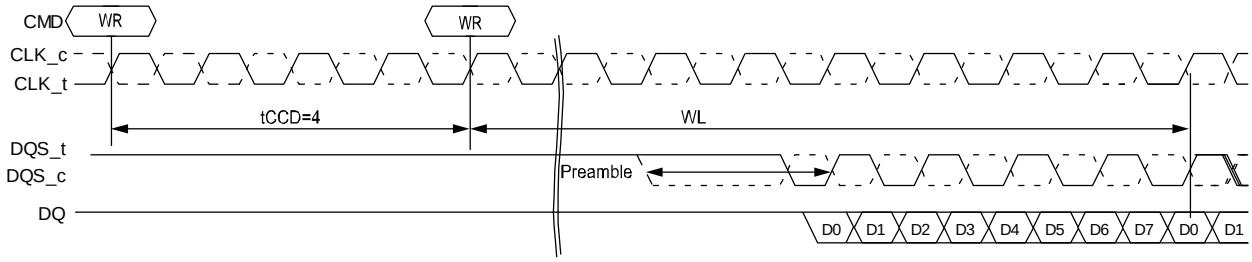
The timing diagrams contained in tCCD=4 (AL=PL=0), tCCD=5 and tCCD=6 (AL=PL=0) illustrate 1 and 2 tCK preamble scenarios for consecutive write commands with tCCD timing of 4, 5 and 6 nCK, respectively. Setting tCCD to 5nCK is not allowed in 2 tCK preamble mode

tCCD=4 (AL=PL=0)

1tCK mode

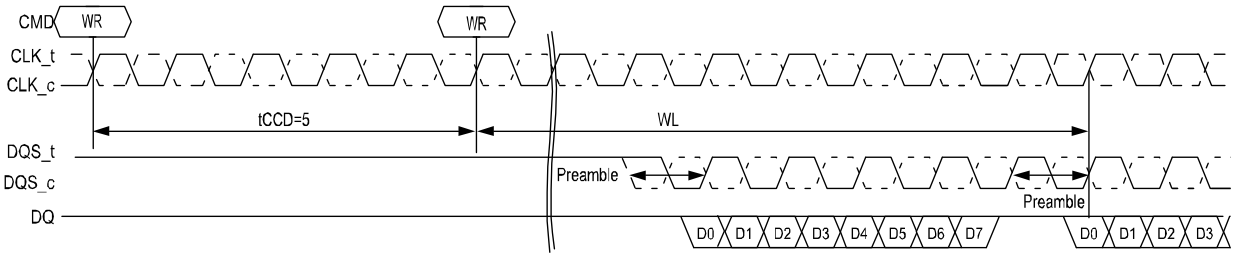


2tCK mode



tCCD=5 (AL=PL=0)

1tCK mode

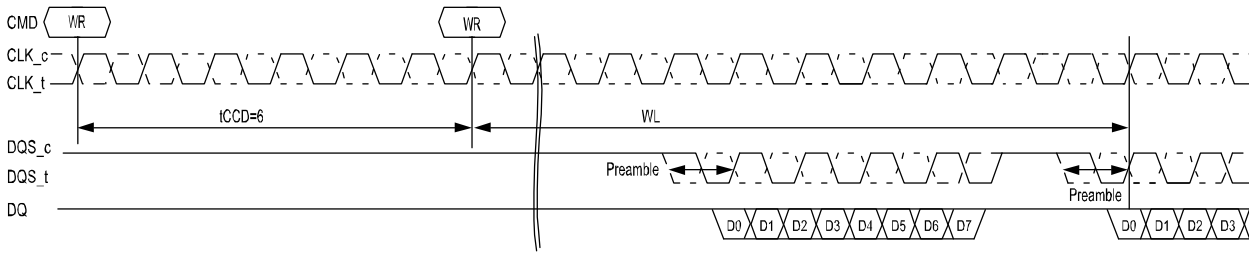


2tCK mode: tCCD=5 is not allowed in 2tCK mode

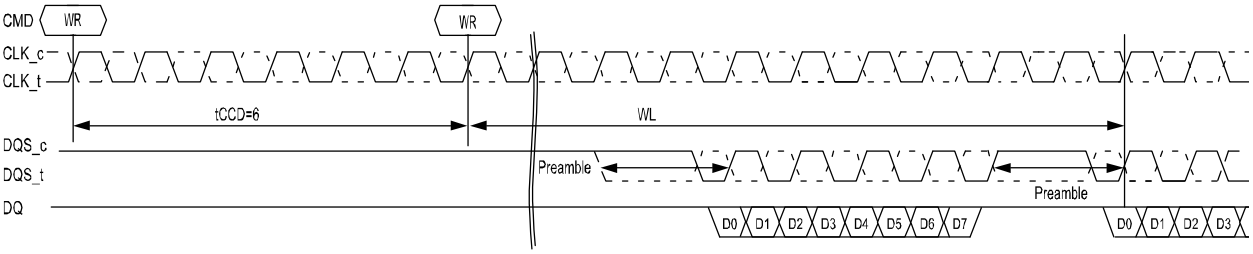
NOTE 1 tCCD__S and tCCD_L = 5 tCKs not allowed when in 2tCK Write Preamble Mode.

tCCD=6 (AL=PL=0)

1tCK mode



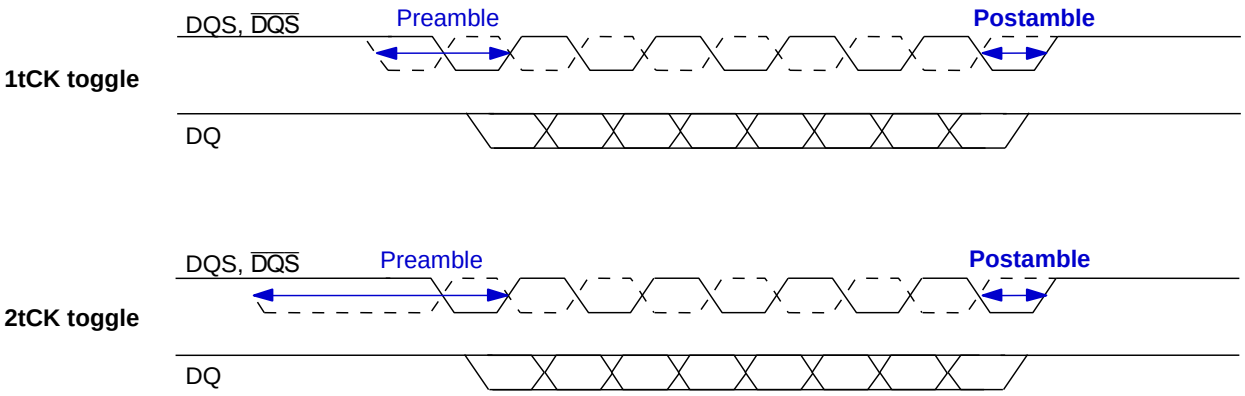
2tCK mode



Write Postamble

DDR4 will support a fixed Write postamble. Write postamble nominal is 0.5tCK for two Write Preamble Modes.

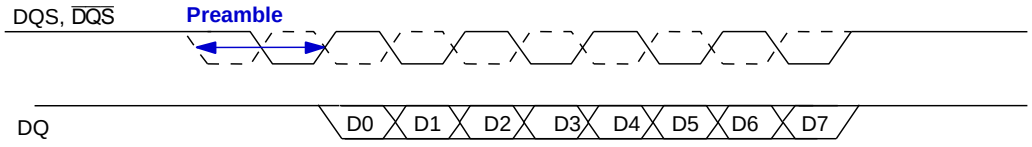
Write Postamble



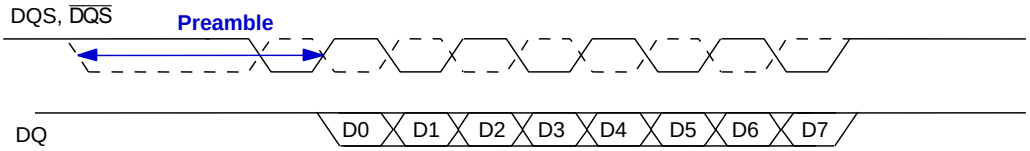
Read Preamble

MR4 A [11] = 0 selects 1 tCK Read Preamble Mode while MR4 [12] = 1 selects 2 tCK Read Preamble Mode, example in the figures below.

1tCK toggle



2tCK toggle

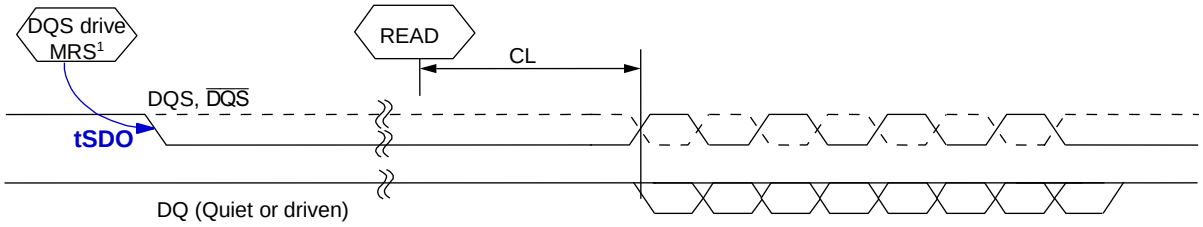


Read Preamble Training

DDR4 supports Read Preamble Training via MPR Reads; that is Read Preamble Training is allowed only when the DRAM is in the MPR access mode. The Read Preamble Training Mode can be used by the DRAM controller to train or "read level" its DQS receivers. Read Preamble Training is entered via an MRS command; MR4[10] = 1 enabled while MR4[10] = 0 is disabled. Once the MRS command is issued to enable Read Preamble Training, the DRAM DQS and $\overline{DQS}$ signals are driven to a valid level by time tSDO is satisfied. During this time, the data bus DQ signals are held quiet, i.e. driven HIGH. The DQS signal remain driven LOW and the $\overline{DQS}$ signal remain driven HIGH until an MPR Page1 READ (Page 0 through Page 3 determine which pattern is used) command is issued; and once CAS latency (CL) has expired, the DQS signals will toggle normally depending on the burst length setting. To exit Read Preamble Training Mode, an MRS command must be issued, MR4[10] = 0.

Parameter	Symbol	DDR4-1600,1866,2133,2400, 2666	
		Min	Max
Delay from MRS Command to Data Strobe Drive Out	tSDO	-	tMOD+9ns

NOTE 1: Read Preamble Training mode is enabled by MR4 A [10] = 1



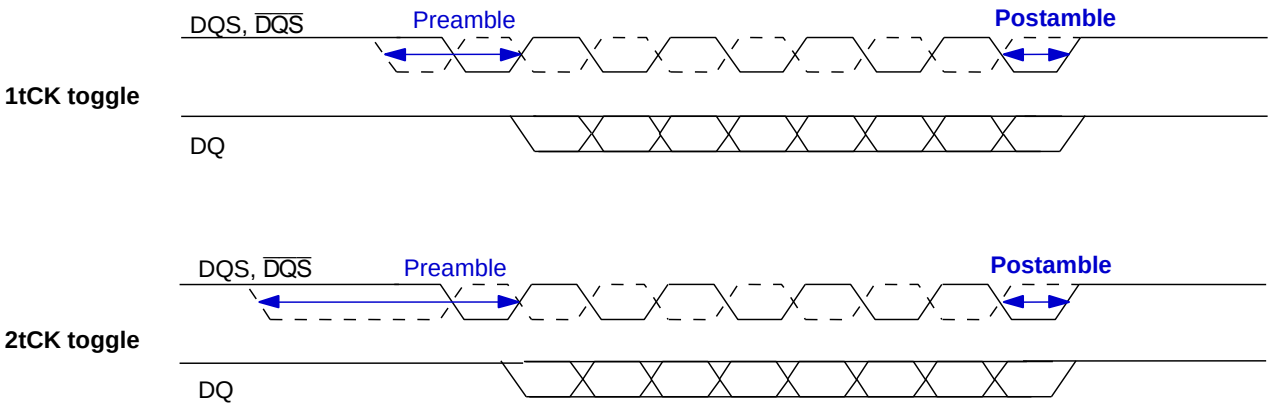
Read Postamble

Whether the 1 tCK or 2 tCK Read Preamble Mode is selected, the Read Postamble remains the same at 1/2 tCK.

DDR4 will support a fixed read postamble.

Read postamble of nominal 0.5tck for preamble modes 1,2 Tck are shown below:

Read Postamble



ACTIVATE Command

The ACTIVATE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BG0-BG1 in X4/8 and BG0 in X16 select the bankgroup; BA0-BA1 inputs selects the bank within the bankgroup, and the address provided on inputs A0-A17 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank or a precharge all command is issued. A bank must be precharged before opening a different row in the same bank.

PRECHARGE Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation for a specified time (tRP) after the PRECHARGE command is issued. An exception to this is the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

If A10 is High when Read or Write command is issued, then auto-precharge function is engaged. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon CAS latency) thus improving system performance for random data access. The RAS lockout circuit internally delays the precharge operation until the array restore operation has been completed (tRAS satisfied) so that the auto precharge command may be issued with any read. Auto-precharge is also implemented during Write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array. The bank will be available for a subsequent row activation a specified time (tRP) after hidden PRECHARGE command (AutoPrecharge) is issued to that bank.

Read Operation

Read Timing Definitions

Read timings are shown below and are applicable in normal operation mode, i.e. when the DLL is enabled and locked.

Rising data strobe edge parameters:

• tDQSCK MIN/MAX describes the allowed range for a rising data strobe edge relative to CK, $\overline{CK}$.

• tDQSCK is the actual position of a rising strobe edge relative to CK, $\overline{CK}$.

• tQSH describes the DQS, $\overline{DQS}$ differential output HIGH time.

• tDQSQ describes the latest valid transition of the associated DQ pins.

• tQH describes the earliest invalid transition of the associated DQ pins.

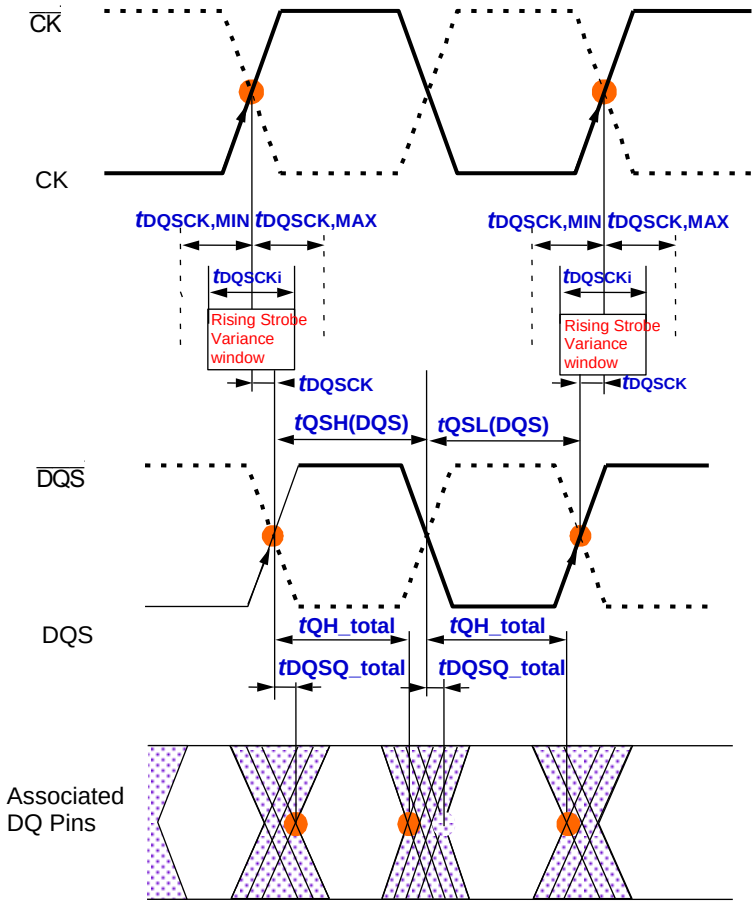
Falling data strobe edge parameters:

• tQSL describes the DQS, $\overline{DQS}$ differential output LOW time.

• tDQSQ describes the latest valid transition of the associated DQ pins.

• tQH describes the earliest invalid transition of the associated DQ pins.

tDQSQ; both rising/falling edges of DQS, no tAC defined.



READ Timing – Clock to Data Strobe Relationship

The clock to data strobe relationship is shown below and is applicable in normal operation mode, i.e. when the DLL is enabled and locked. Rising data strobe edge parameters:

• tDQSCK MIN/MAX describes the allowed range for a rising data strobe edge relative to CK, $\overline{CK}$.

• tDQSCK is the actual position of a rising strobe edge relative to CK, $\overline{CK}$.

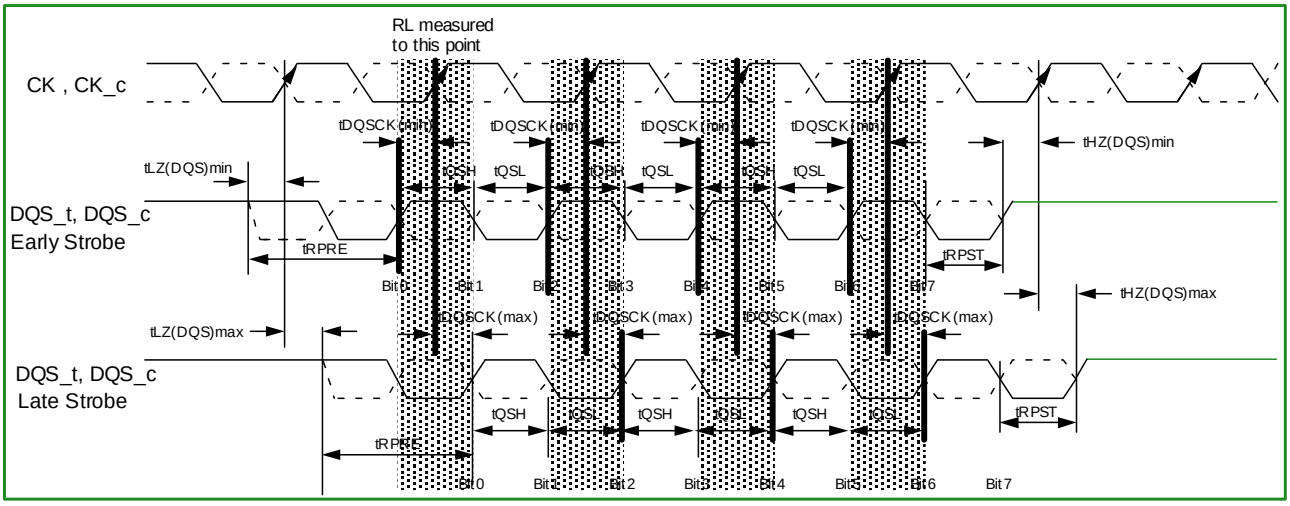
• tQSH describes the data strobe high pulse width.

Falling data strobe edge parameters:

• tQSL describes the data strobe low pulse width.

• tLZ(DQS), tHZ(DQS) for preamble/postamble

Clock to Data Strobe Relationship



NOTE 1 Within a burst, the rising strobe edge can be varying within tDQSCKi while at the same voltage and temperature. However, incorporate the device, voltage and temperature variation, rising strobe edge variance window, tDQSCKi can shift between tDQSCK(min) and tDQSCK(max). A timing of this window's right inside edge (latest) from rising CK, $\overline{CK}$ is limited by a device's actual tDQSCK(max). A timing of this window's left inside edge (earliest) from rising CK, $\overline{CK}$ is limited by tDQSCK(min).

NOTE 2 Notwithstanding Note 1, a rising strobe edge with tDQSCK (MAX) at T(n) cannot be immediately followed by a rising strobe edge with tDQSCK (MIN) at T(n+1) because other timing relationships (tQSH, tQSL) exist: if tDQSCK(n+1) < 0: tDQSCK(n) < 1.0 tCK - (tQSH (MIN) + tQSL (MIN) - | tDQSCK(n+1) |

NOTE 3 The DQS, $\overline{DQS}$ differential output HIGH time is defined by tQSH and the DQS, $\overline{DQS}$ differential output LOW time is defined by tQSL.

NOTE 4 Likewise, tLZ(DQS) MIN and tHZ(DQS) MIN are not tied to tDQSCK (MIN) (early strobe case) and tLZ(DQS) MAX and tHZ(DQS) MAX are not tied to tDQSCK (MAX) (late strobe case).

NOTE 5 The minimum pulse width of read preamble is defined by tRPRE (MIN).

NOTE 6 The maximum read postamble is bound by tDQSCK (MIN) plus tQSH (MIN) on the left side and tHZDSQ (MAX) on the right side.

NOTE 7 The minimum pulse width of read postamble is defined by tRPST (MIN).

NOTE 8 The maximum read preamble is bound by tLZDQS (MIN) on the left side and tDQSCK (MAX) on the right side.

READ Timing – Data Strobe to Data Relationship

The data strobe to data relationship is shown below and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

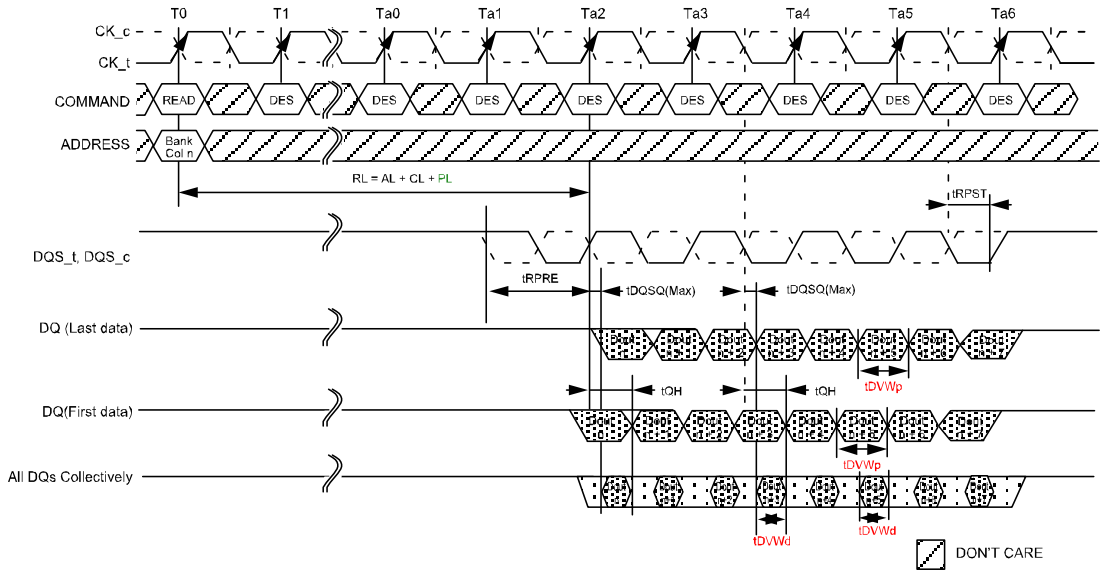
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

tDQSQ; both rising/falling edges of DQS, no tAC defined.

Data Valid Window:

- tDVWd is the Data Valid Window per device per UI and is derived from (tQH - tDQSQ) of each UI on a given DRAM. This parameter will be characterized and guaranteed by design.
- tDVWp is Data Valid Window per pin per UI and is derived from (tQH - tDQSQ) of each UI on a pin of a given DRAM. This parameter will be characterized and guaranteed by design.

Data Strobe to Data Relationship



NOTE 1 BL = 8, RL = 11 (AL = 0, CL = 1), Preamble = 1CK

NOTE 2 DOUTn = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0A [1:0] = 00or MR0A [1:0] = 01 and A12 = 1 during READ commands at T0.

NOTE 5 Output timings are referenced to VDDQ, and DLL on for locking.

NOTE 6 tDQSQ defines the skew between DQS, $\overline{DQS}$ to data and does not define DQS, $\overline{DQS}$ to clock.

NOTE 7 Early data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

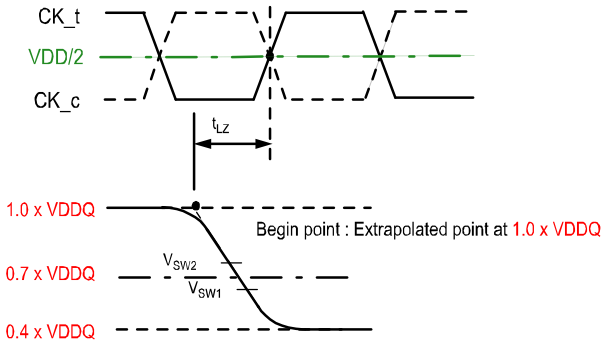
tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation

tHZ and tLZ transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ).

tLZ shows a method to calculate the point when the device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ), by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single ended.

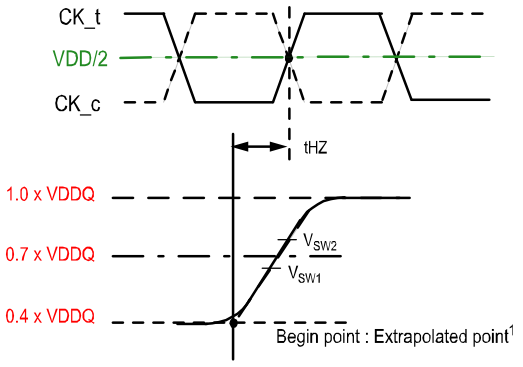
tLZ(DQ) and tHZ(DQ) method for calculating transitions and begin points

tLZ(DQ): CK_t - CK_c rising crossing at RL



tLZ(DQ) begin point is above-mentioned extrapolated point.

tHZ(DQ) with BL8: CK_t - CK_c rising crossing at RL + 4 nCK
tHZ(DQ) with BC4: CK_t - CK_c rising crossing at RL + 2 nCK



tHZ(DQ) is begin point is above-mentioned extrapolated point.

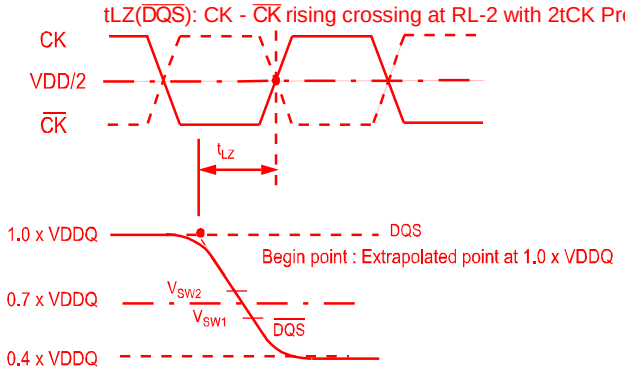
NOTE 1 Extrapolated point (Low Level) =VDDQ/(50+34) X 34
= VDDQ x 0.40
- A driver impedance : RZQ/7(34ohm)
- An effective test load : 50 ohm to VTT = VDDQ

Reference Voltage for tLZ(DQ), tHZ(DQ) Timing Measurements

Measured Parameter Symbol	Measured Parameter	Vsw1 [V]	Vsw2 [V]
tLZ(DQ)	DQ low-impedance time from CK, $\overline{CK}$	(0.70 – 0.04) x VDDQ	(0.70 + 0.04) x VDDQ
tHZ(DQ)	DQ high-impedance time from CK, $\overline{CK}$	(0.70 – 0.04) x VDDQ	(0.70 + 0.04) x VDDQ

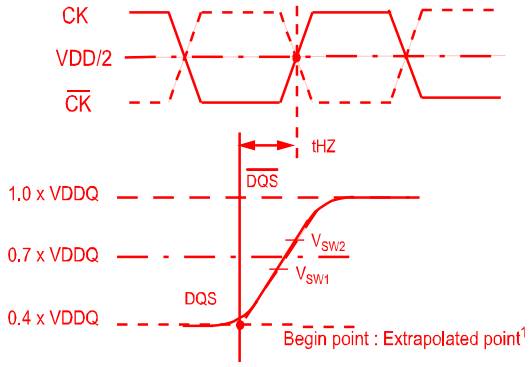
tLZ ($\overline{DQS}$) and tHZ(DQS) method for calculating transitions and begin points

tLZ($\overline{DQS}$): CK - $\overline{CK}$ rising crossing at RL-1 with 1tCK Preamble
tLZ($\overline{DQS}$): CK - $\overline{CK}$ rising crossing at RL-2 with 2tCK Preamble



tLZ($\overline{DQS}$) begin point is above-mentioned extrapolated point.

tHZ(DQS) with BL8: CK- $\overline{CK}$ rising crossing at RL + 4 nCK
tHZ(DQS) with BC4: CK - $\overline{CK}$ rising crossing at RL + 2 nCK



tHZ(DQS) begin point is above-mentioned extrapolated point.

NOTE 1 Extrapolated point (Low Level) = VDDQ/(50+34) X 34
= VDDQ x 0.40
- A driver impedance : RZQ/7(34ohm)
- An effective test load : 50 ohm to VTT = VDDQ

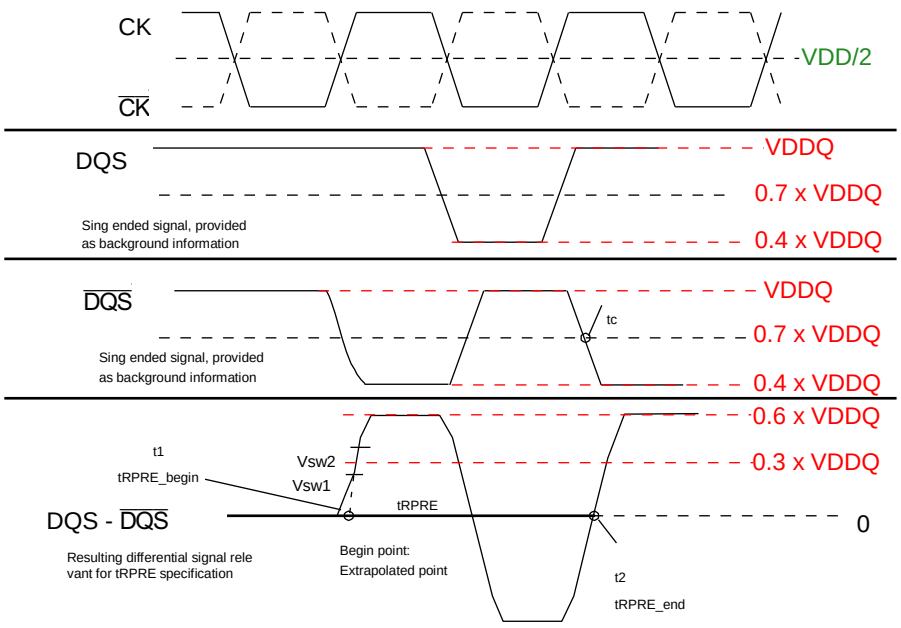
Reference Voltage for tLZ ($\overline{DQS}$), tHZ(DQS) Timing Measurements

Measured Parameter Symbol	Measured Parameter	Vsw1 [V]	Vsw2 [V]
tLZ($\overline{DQS}$)	$\overline{DQS}$ low-impedance time from CK, $\overline{CK}$	(0.70 – 0.04) x VDDQ	(0.70 + 0.04) x VDDQ
tHZ(DQS)	DQS high-impedance time from CK, $\overline{CK}$	(0.70 – 0.04) x VDDQ	(0.70 + 0.04) x VDDQ

tRPRE Calculation

The method for calculating differential pulse widths for tRPRE is shown in figure below

Method for calculating tRPRE transitions and endpoints



NOTE 1 Low Level of DQS and $\overline{DQS}$ = VDDQ/ (50+34) x 34 = VDDQ x 0.40
- A driver impedance: RZQ/7(34Ω)
- An effective test load: 50 Ω to VTT = VDDQ

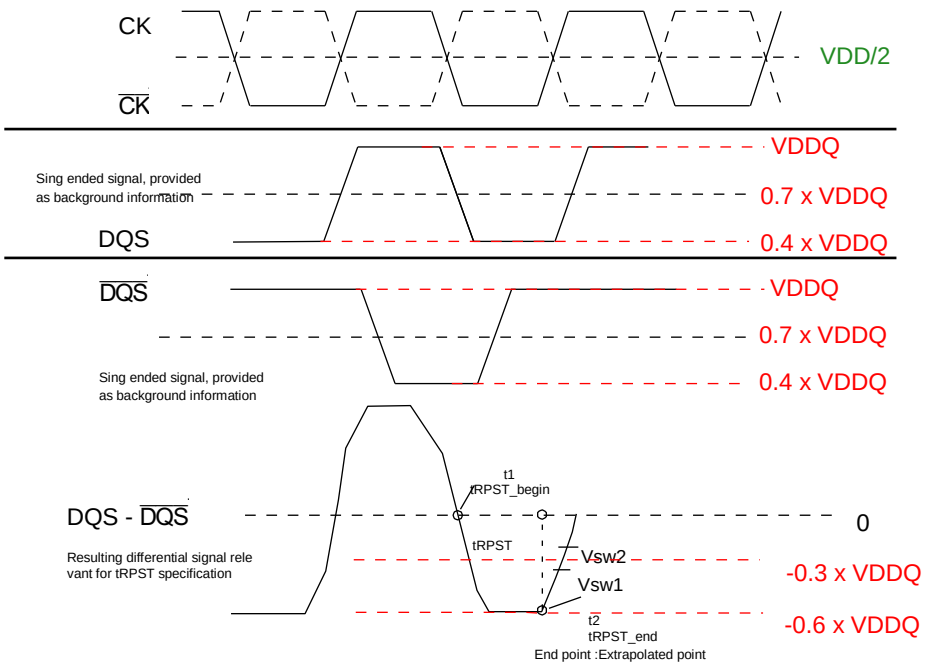
Reference Voltage for tRPRE Timing Measurements

Measured Parameter Symbol	Measured Parameter	Vsw1 [V]	Vsw2 [V]
tRPRE	DQS, $\overline{DQS}$ differential READ Preamble	(0.30 – 0.04) x VDDQ	(0.30 + 0.04) x VDDQ

tRPST Calculation

The method for calculating differential pulse widths for tRPST is shown in figure below

Method for calculating tRPST transitions and endpoints



NOTE 1 Low Level of DQS and $\overline{DQS}$ = VDDQ/ (50+34) x 34 = VDDQ x 0.40
- A driver impedance: RZQ/7(34 Ω)
- An effective test load: 50 Ω to VTT = VDDQ

Reference Voltage for tRPST Timing Measurements

Measured Parameter Symbol	Measured Parameter	Vsw1 [V]	Vsw2 [V]
tRPST	DQS, $\overline{DQS}$ differential READ Postamble	(-0.30 – 0.04) x VDDQ	(-0.30 + 0.04) x VDDQ

READ Burst Operation

DDR4 READ command supports bursts of BL8 (fixed), BC4 (fixed), and BL8/BC4 on-the-fly (OTF); OTF uses address A12 to control OTF during the READ or WRITE (AUTO PRECHARGE can be enabled or disabled).

• A12 = 0, BC4 (BC4 = burst chop)

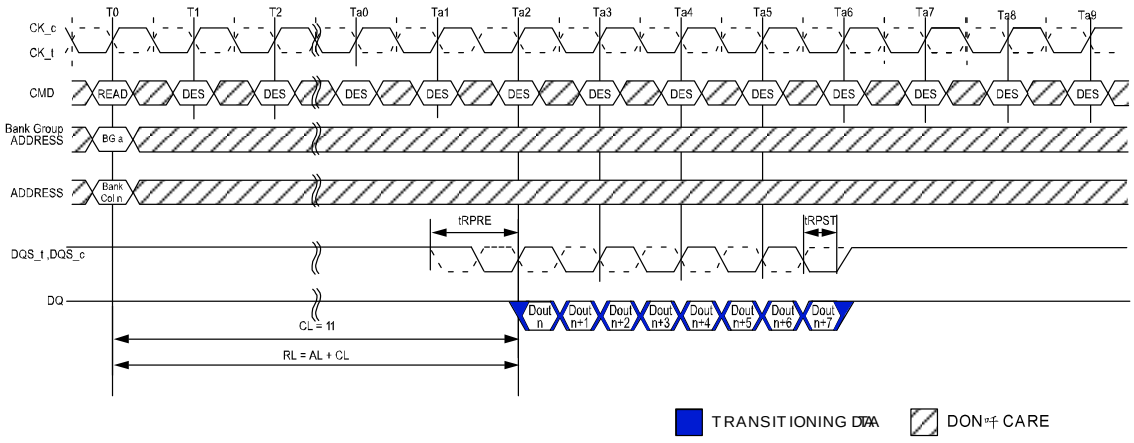
• A12 = 1, BL8

Read commands can issue precharge automatically with a read with auto-precharge command (RDA); and is enabled by A10 high.

• Read command with A10 = 0 (RD) performs standard Read, bank remains active after read burst.

• Read command with A10 = 1 (RDA) performs Read with auto-precharge, back goes in to precharge after read burst.

READ Burst Operation RL = 11 (AL = 0, CL = 11, BL8)



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 1tCK

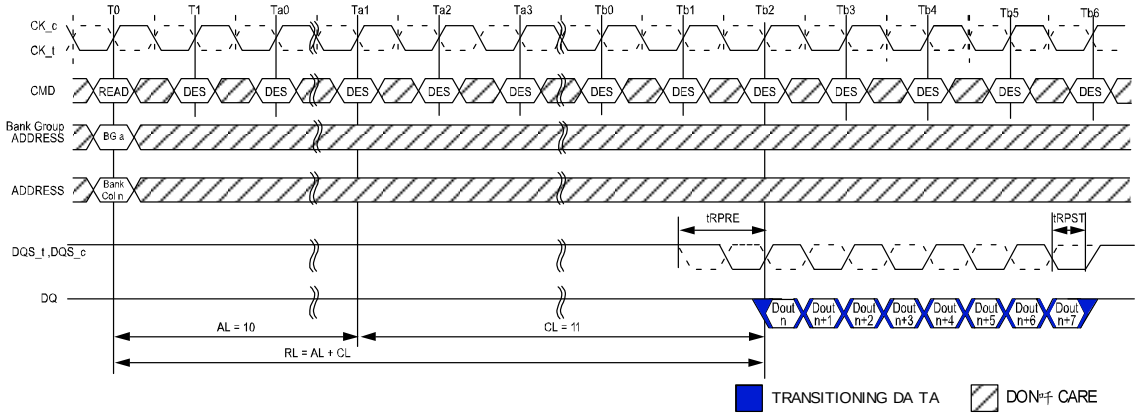
NOTE 2 DOUT n = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A [1:0] = 00 or MR0 A [1:0] = 01 and A12 = 1 during READ command at T0.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable

READ Burst Operation RL = 21 (AL = 10, CL = 11, BL8)



NOTE 1 BL = 8, RL = 21, AL = (CL-1), CL = 11, Preamble = 1tCK

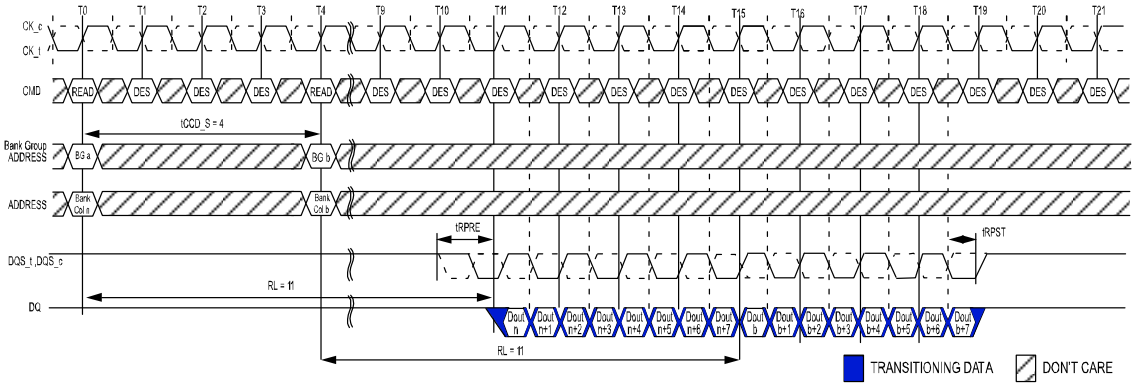
NOTE 2 DOUT n = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0A [1:0] = 00 or MR0A [1:0] = 01and A12 = 1 during READ command at T0.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable

Consecutive READ (BL8) with 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 1tCK

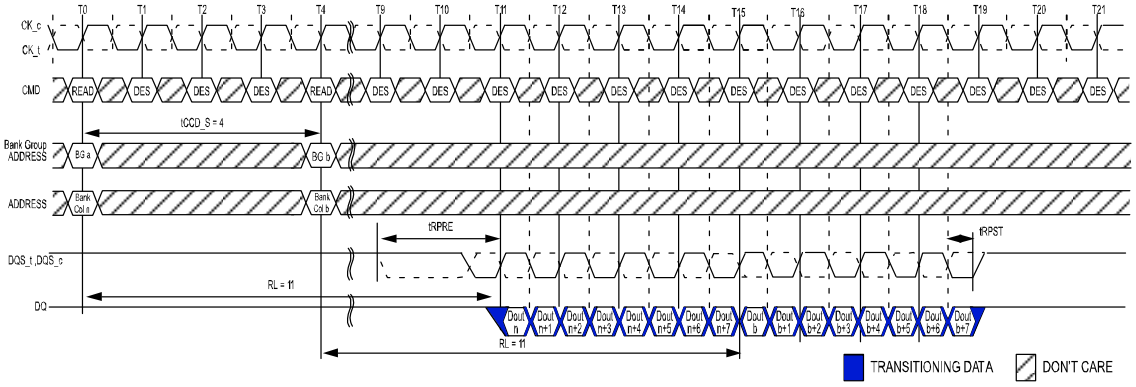
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A [1:0] = 00 or MR0 A [1:0] = 01 and A12 = 1 during READ command at T0 and T4.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable

Consecutive READ (BL8) with 2tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 2tCK

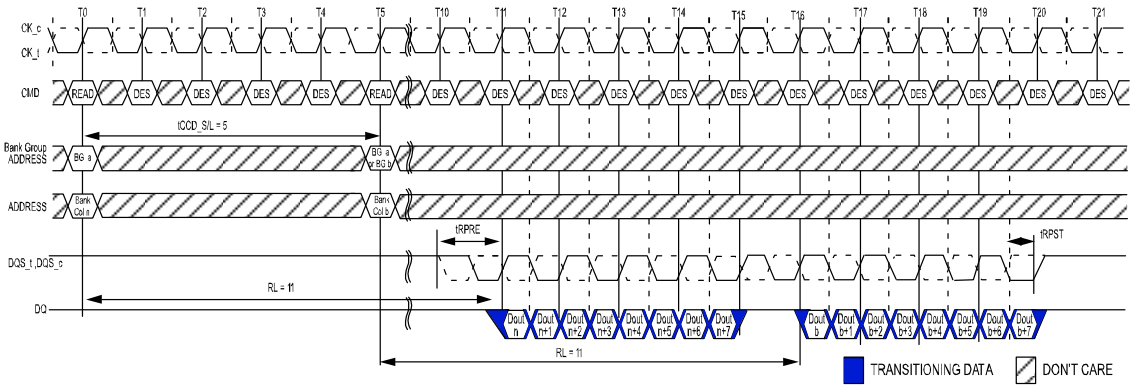
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A [1:0] = 00 or MR0 A [1:0] = 01 and A12 = 1 during READ command at T0 and T4.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable

Nonconsecutive READ (BL8) with 1tCK Preamble in Same or Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 1tCK, tCCD_S/L = 5

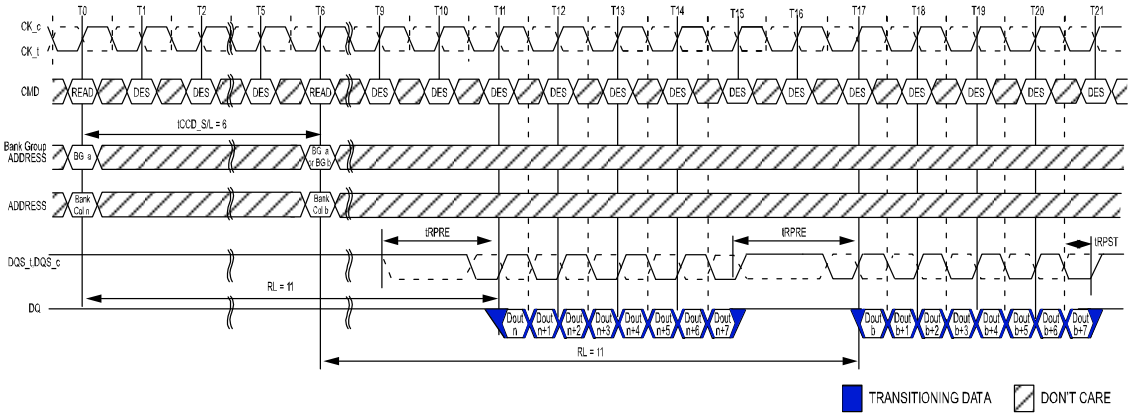
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A[1:0] = 00 or MR0 A[1:0] = 01 and A12 = 1 during READ command at T0 and T5.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable

Nonconsecutive READ (BL8) with 2tCK Preamble in Same or Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 2tCK, tCCD_S/L = 6

NOTE 2 DOUT n (or b) = data-out from column n (or column b).

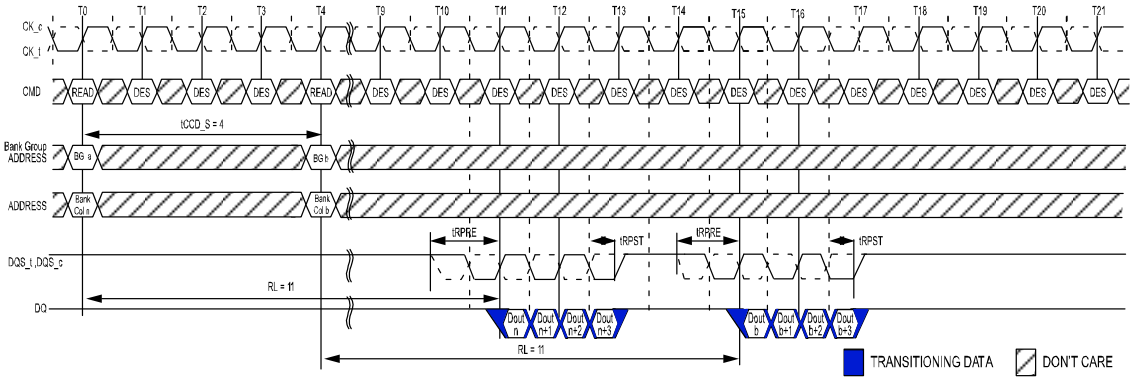
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A[1:0] = 00 or MR0 A[1:0] = 01 and A12 = 1 during READ command at T0 and T6.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable

NOTE 6 tCCD_S/L=5 isn't allowed in 2tCK preamble mode.

READ (BC4) to READ (BC4) with 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 1tCK

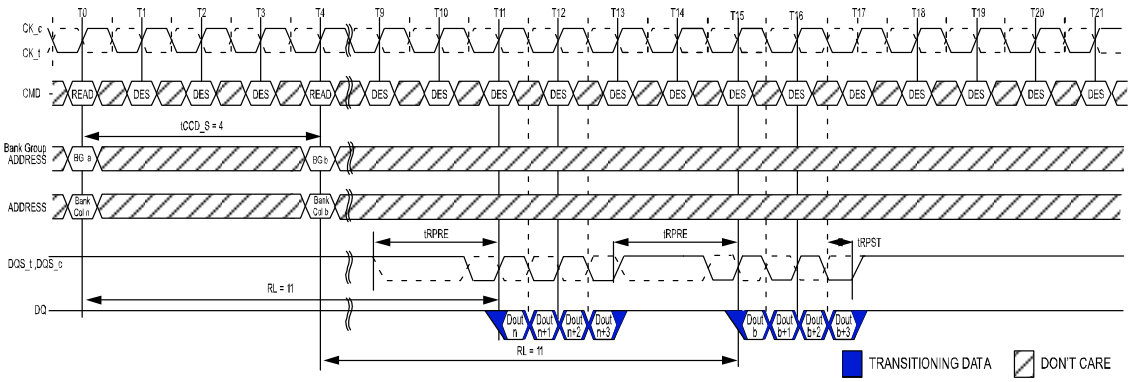
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by either MR0[A1:A0 = 1:0] or MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0 and T4.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable

READ (BC4) to READ (BC4) with 2tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 2tCK

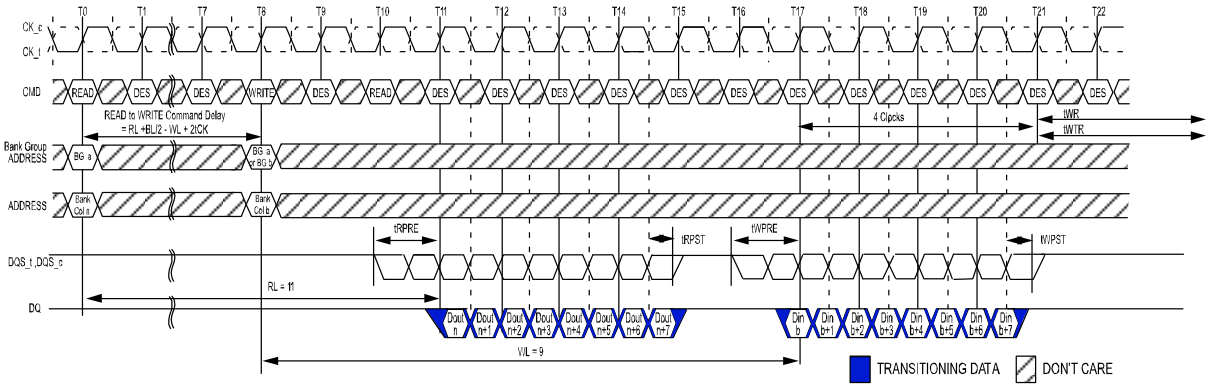
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by either MR0 A[1:0] = 10 or MR0 A[1:0] = 01 and A12 = 0 during READ command at T0 and T4.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable

READ (BL8) to WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group



NOTE 1 BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL =9 (CWL = 9, AL = 0), Write Preamble = 1tCK

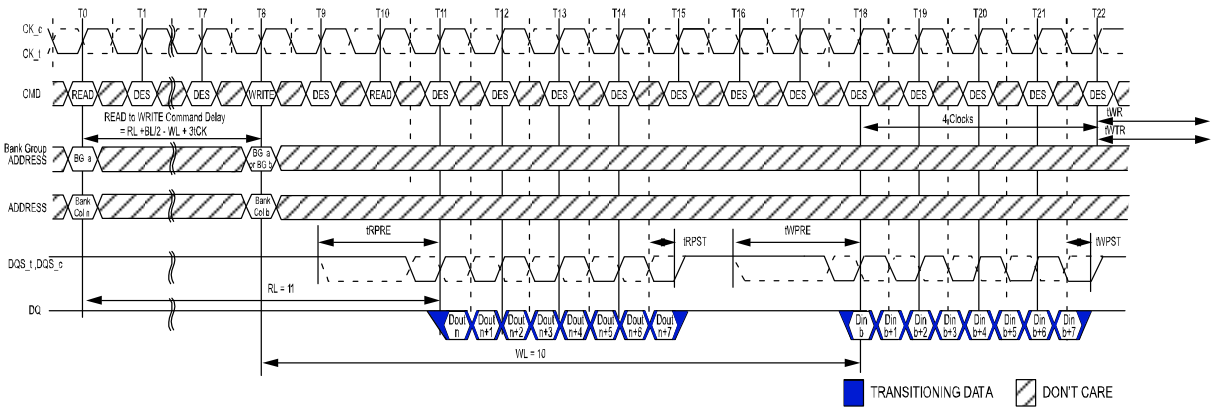
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A[1:0] = 00 or MR0 A[1:0] = 01 and A12 = 1 during READ command at T0 and WRITE command at T8.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BL8) to WRITE (BL8) with 2tCK Preamble in Same or Different Bank Group



NOTE 1 BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1[5], AL = 0), Write Preamble = 2tCK

NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

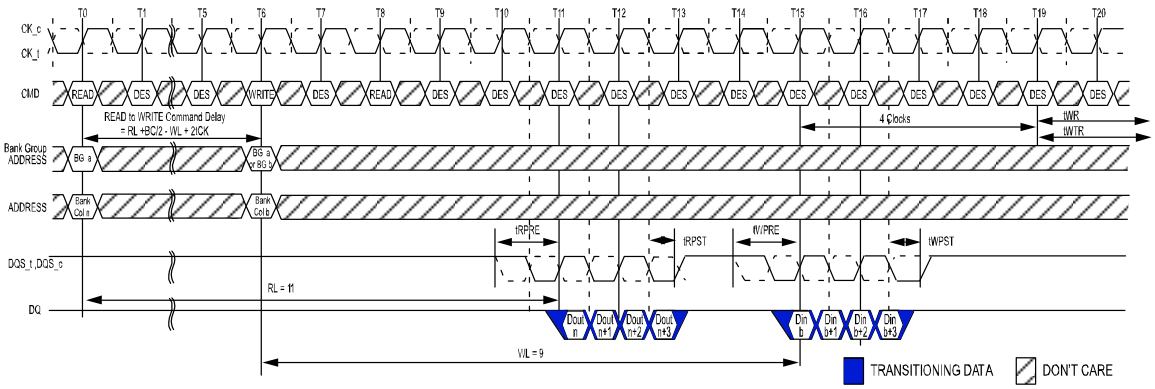
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A[1:0] = 00 or MR0 A[1:0] = 01 and A12 = 1 during READ command at T0 and WRITE command at T8.

NOTE 5 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.

NOTE 6 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable, Write $\overline{DBI}$ = Disable, Write CRC = Disable.

READ (BC4) OTF to WRITE (BC4) OTF with 1tCK Preamble in Same or Different Bank Group



NOTE 1 BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), Write Preamble = 1tCK

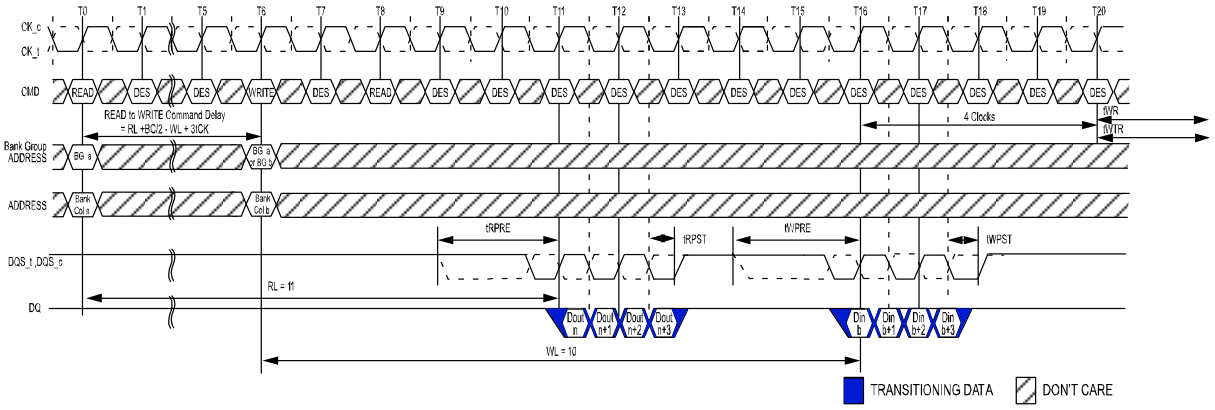
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4(OTF) setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0 and WRITE command at T6.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable, Write $\overline{DBI}$ = Disable, Write CRC = Disable.

READ (BC4) OTF to WRITE (BC4) OTF with 2tCK Preamble in Same or Different Bank Group



NOTE 1 BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1[5], AL = 0), Write Preamble = 2tCK

NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

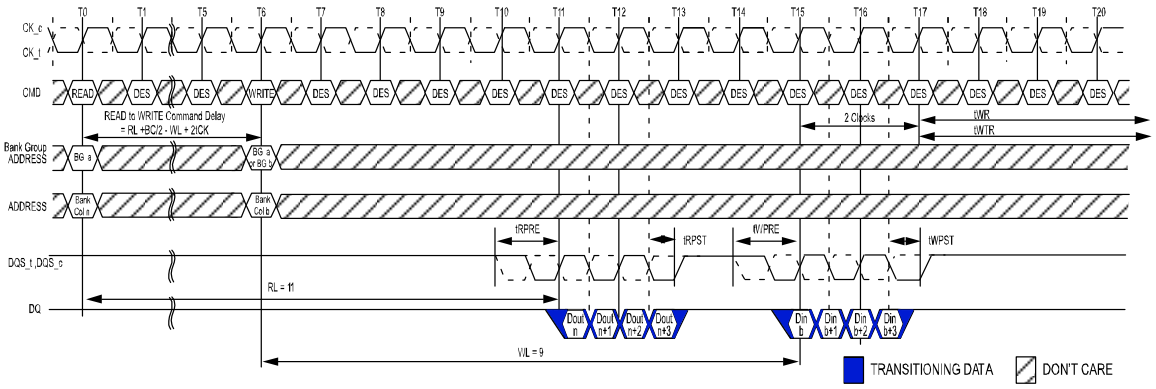
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4(OTF) setting activated by MR0 A[1:]0 = 01 and A12 = 0 during READ command at T0 and WRITE command at T6.

NOTE 5 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.

NOTE 6 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable, Write $\overline{DBI}$ = Disable, Write CRC = Disable.

READ (BC4) Fixed to WRITE (BC4) Fixed with 1tCK Preamble in Same or Different Bank Group



NOTE 1 BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), Write Preamble = 1tCK

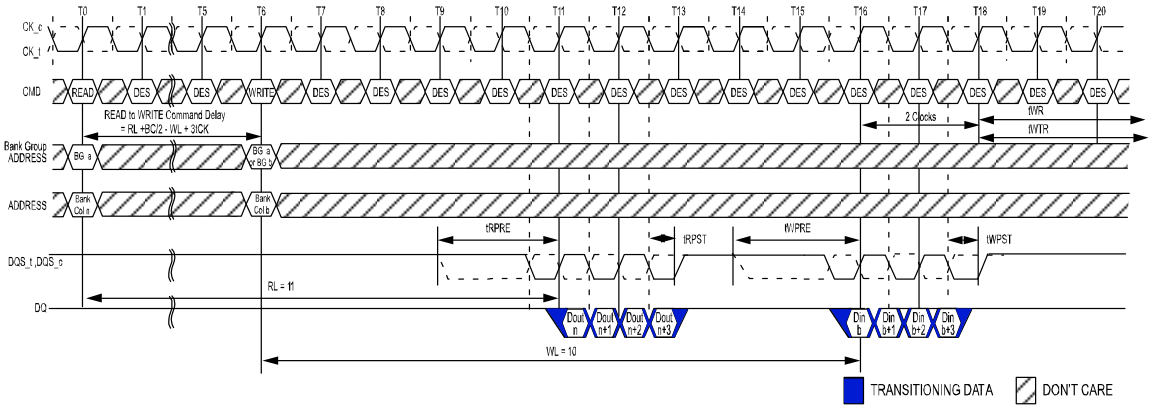
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4(Fixed) setting activated by MR0 A[1:0] = 10.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable, Write $\overline{DBI}$ = Disable, Write CRC = Disable.

READ (BC4) Fixed to WRITE (BC4) Fixed with 2tCK Preamble in Same or Different Bank Group



NOTE 1 BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1[5], AL = 0), Write Preamble = 2tCK

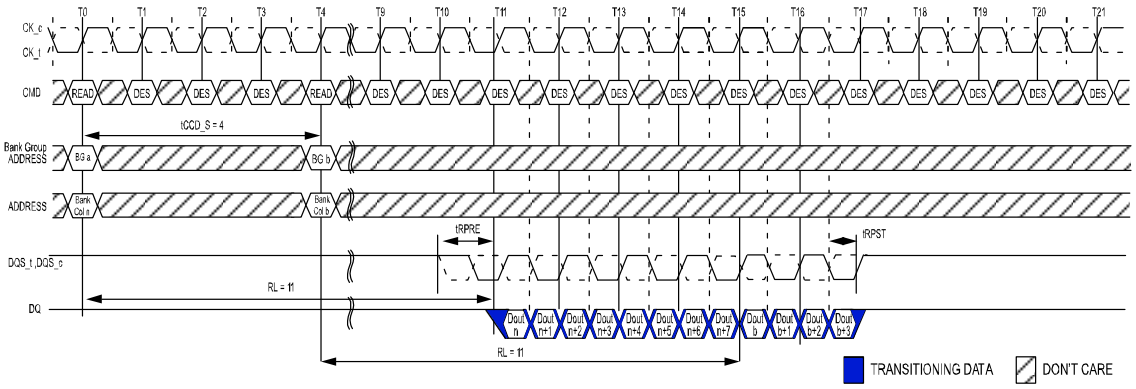
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4(Fixed) setting activated by MR0 A[1:0] = 10.

NOTE 5 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.

NOTE 6 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable, Write $\overline{DBI}$ = Disable, Write CRC = Disable.



NOTE 1 BL = 8, AL =0, CL = 11 ,Preamble = 1tCK

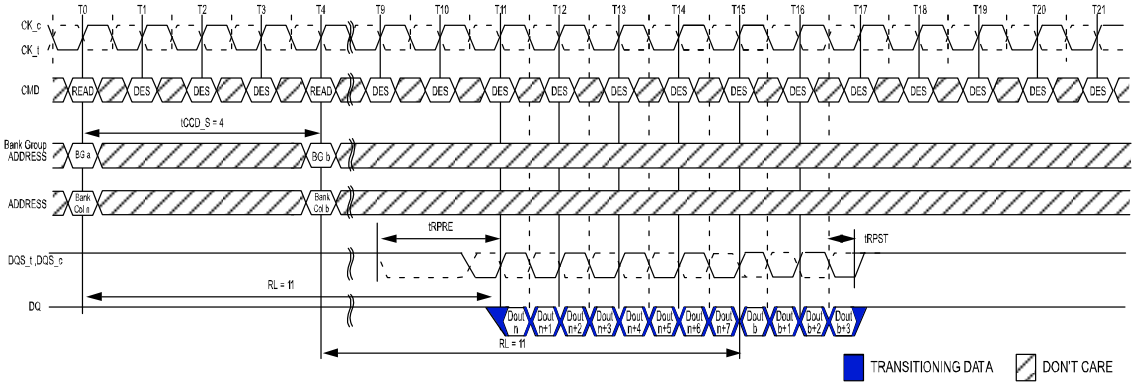
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by MR0 A[1:0] = 01 and A12 = 1 during READ command at T0.
BC4 setting activated by MR0 A[1:0] = 01 and A12 = 0 during READ command at T4.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable.

READ (BL8) to READ (BC4) OTF with 2tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL =0, CL = 11 ,Preamble = 2tCK

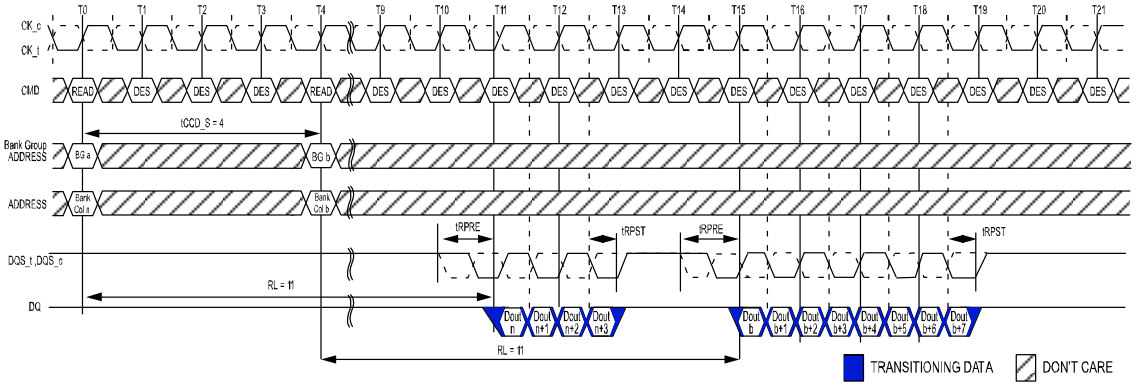
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by MR0 A[1:0] = 01 and A12 = 1 during READ command at T0.
BC4 setting activated by MR0 A[1:0] = 01 and A12 = 0 during READ command at T4.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable.

READ (BC4) to READ (BL8) OTF with 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL =0, CL = 11 ,Preamble = 1tCK

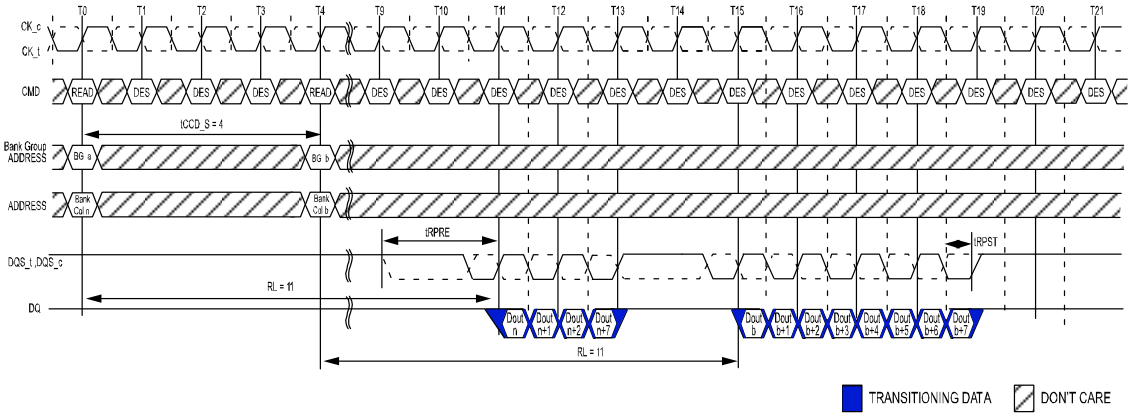
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0 A[1:0] = 01 and A12 = 0 during READ command at T0.
BL8 setting activated by MR0 A[1:0] = 01 and A12 = 1 during READ command at T4.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable.

READ (BC4) to READ (BL8) OTF with 2tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL =0, CL = 11, Preamble = 2tCK

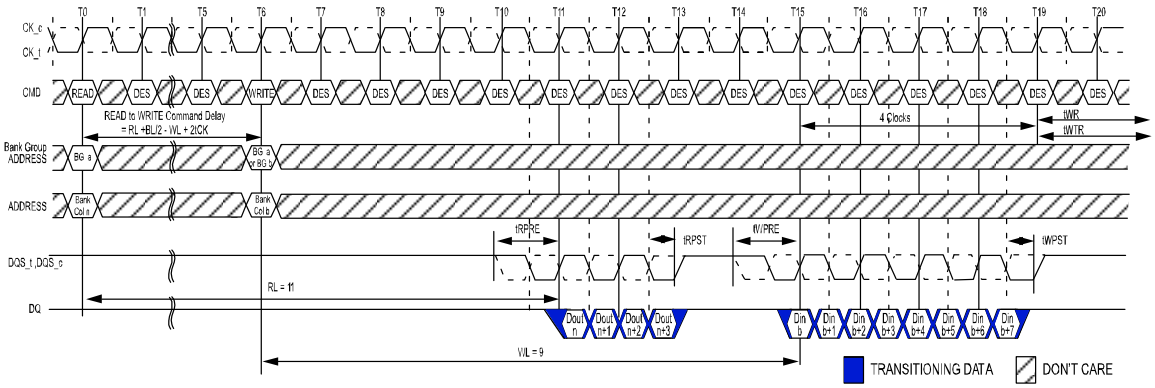
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0 A[1:0] = 01 and A12 = 0 during READ command at T0.
BL8 setting activated by MR0 A[1:0] = 01 and A12 = 1 during READ command at T4.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable.

READ (BC4) to WRITE (BL8) OTF with 1tCK Preamble in Same or Different Bank Group



NOTE 1 BC = 4, RL = 11(CL = 11 , AL = 0), Read Preamble = 1tCK, WL=9(CWL=9,AL=0), Write Preamble = 1tCK

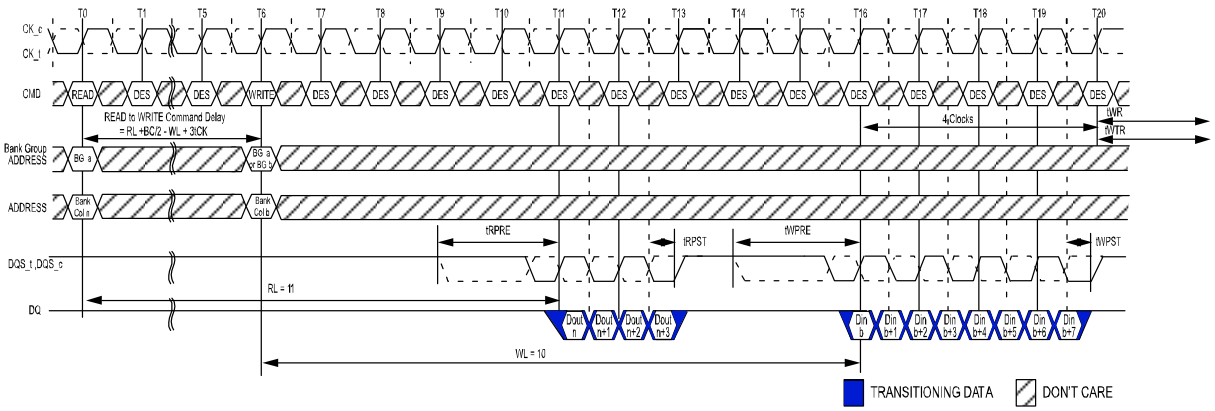
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0 A[1:0] = 01 and A12 = 0 during READ command at T0.
BL8 setting activated by MR0 A[1:0] = 01 and A12 = 1 during WRITE command at T6.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable, Write $\overline{DBI}$ = Disable, Write CRC = Disable.

READ (BC4) to WRITE (BL8) OTF with 2tCK Preamble in Same or Different Bank Group



NOTE 1 BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1[5], AL = 0), Write Preamble = 2tCK

NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

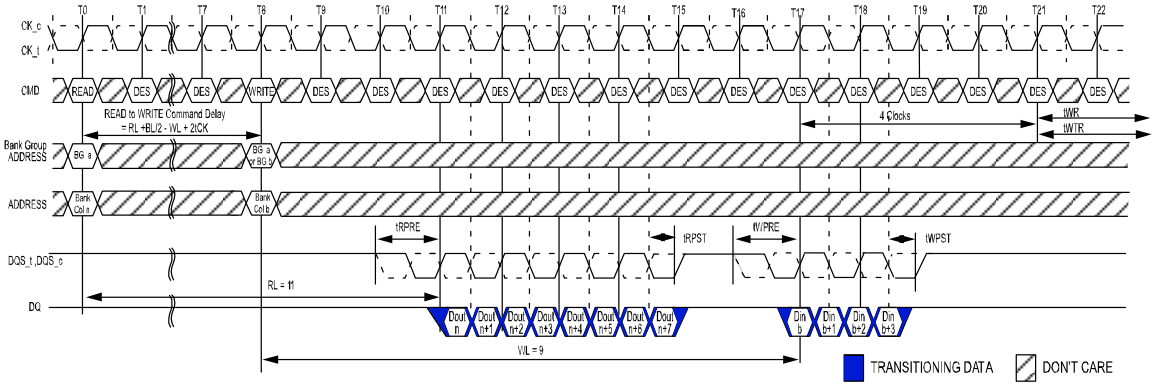
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0 A[1:0] = 01 and A12 = 0 during READ command at T0.
BL8 setting activated by MR0 A[1:0] = 01 and A12 = 1 during WRITE command at T6.

NOTE 5 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.

NOTE 6 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable, Write $\overline{DBI}$ = Disable, Write CRC = Disable.

READ (BL8) to WRITE (BC4) OTF with 1tCK Preamble in Same or Different Bank Group



NOTE 1 BL = 8, RL = 11(CL = 11 , AL = 0), Read Preamble = 1tCK, WL=9(CWL=9,AL=0), Write Preamble = 1tCK

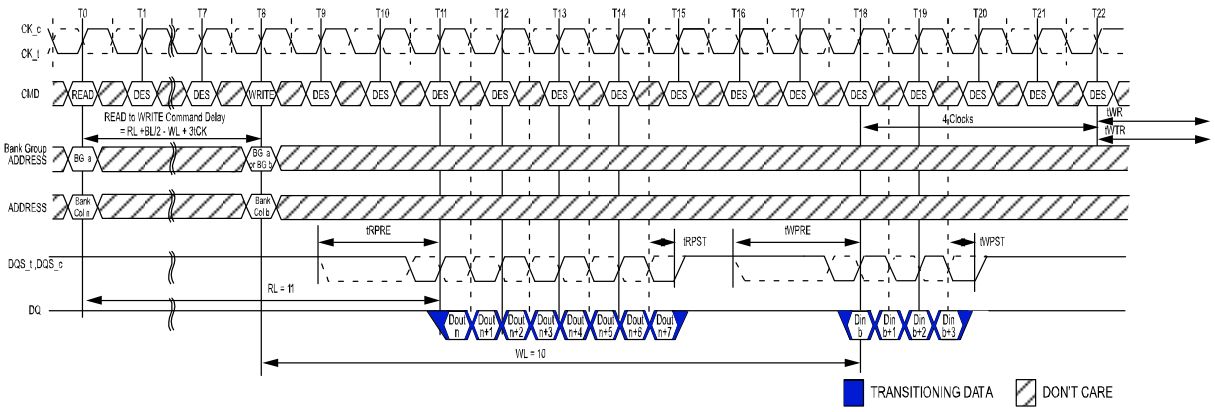
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by MR0 A[1:0] = 01 and A12 = 1 during READ command at T0.
BC4 setting activated by MR0 A[1:0] = 01 and A12 = 0 during WRITE command at T8.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable, Write $\overline{DBI}$ = Disable, Write CRC = Disable.

READ (BL8) to WRITE (BC4) OTF with 2tCK Preamble in Same or Different Bank Group



NOTE 1 BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1[5], AL = 0), Write Preamble = 2tCK

NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by MR0 A[1:0] = 01 and A12 = 1 during READ command at T0.
BC4 setting activated by MR0 A[1:0] = 01 and A12 = 0 during WRITE command at T8.

NOTE 5 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.

NOTE 6 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable, Write $\overline{DBI}$ = Disable, Write CRC = Disable.

Burst Read Operation followed by a Precharge

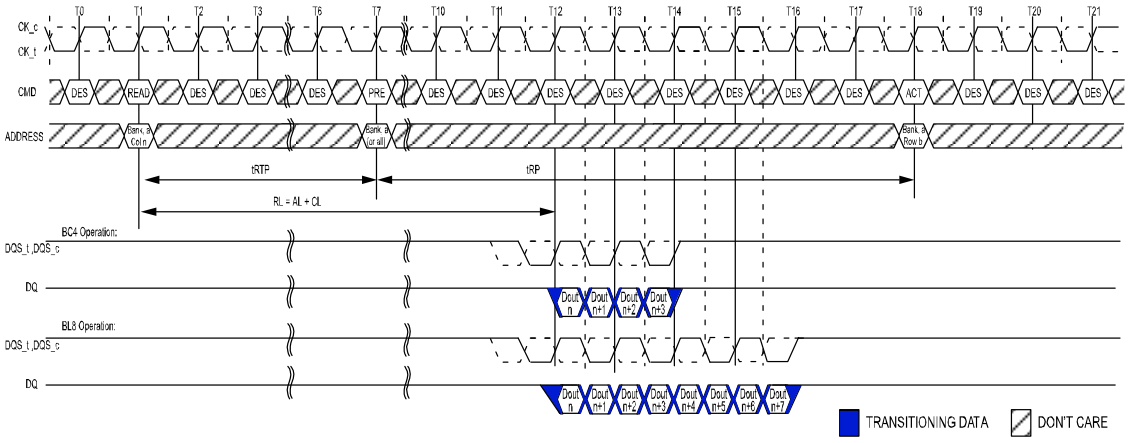
The minimum external Read command to Precharge command spacing to the same bank is equal to AL + tRTP with tRTP being the Internal Read Command to Precharge Command Delay. Note that the minimum ACT to PRE timing, tRAS, must be satisfied as well. The minimum value for the Internal Read Command to Precharge Command Delay is given by tRTP.min, A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously:

1. The minimum RAS precharge time (tRP.MIN) has been satisfied from the clock at which the precharge begins.

2. The minimum RAS cycle time (tRC.MIN) from the previous bank activation has been satisfied.

Examples of Read commands followed by Precharge are show in READ to PRECHARGE with 1tCK Preamble to READ to PRECHARGE with Additive Latency and 1tCK Preamble.

READ to PRECHARGE with 1tCK Preamble



NOTE 1 BL = 8, RL = 11(CL = 11 , AL = 0), Preamble = 1tCK, tRTP = 6, tRP = 11

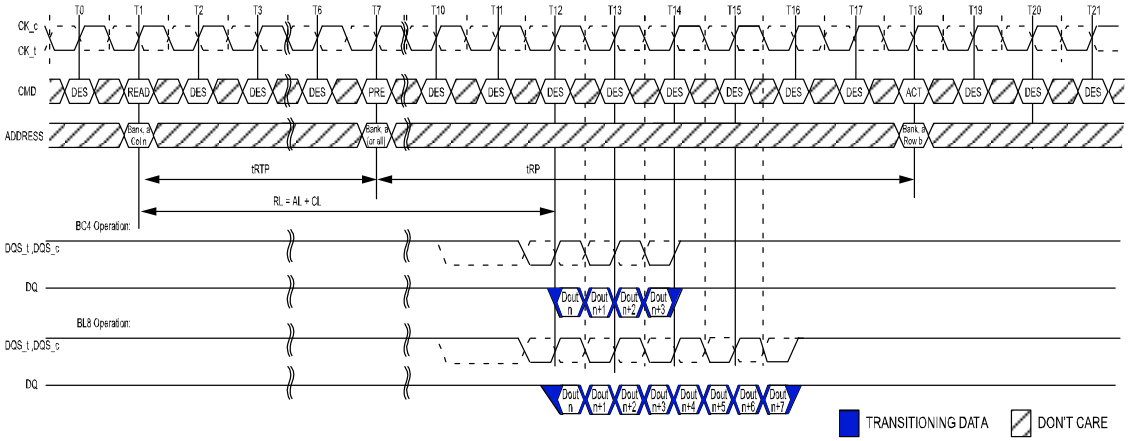
NOTE 2 DOUT n = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 The example assumes tRAS. MIN is satisfied at Precharge command time(T7) and that tRC. MIN is satisfied at the next Active command time(T18).

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable.

READ to PRECHARGE with 2tCK Preamble



NOTE 1 BL = 8, RL = 11(CL = 11 , AL = 0), Preamble = 2tCK, tRTP = 6, tRP = 11

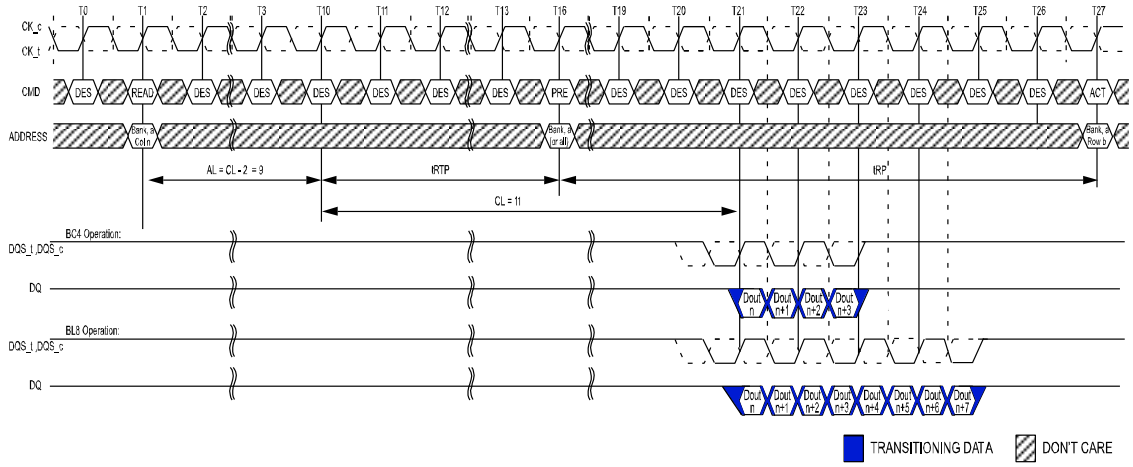
NOTE 2 DOUT n = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 The example assumes tRAS. MIN is satisfied at Precharge command time(T7) and that tRC. MIN is satisfied at the next Active command time(T18).

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable.

READ to PRECHARGE with Additive Latency and 1tCK Preamble



NOTE 1 BL = 8, RL = 20 (CL = 11 , AL = CL- 2), Preamble = 1tCK, tRTP = 6, tRP = 11

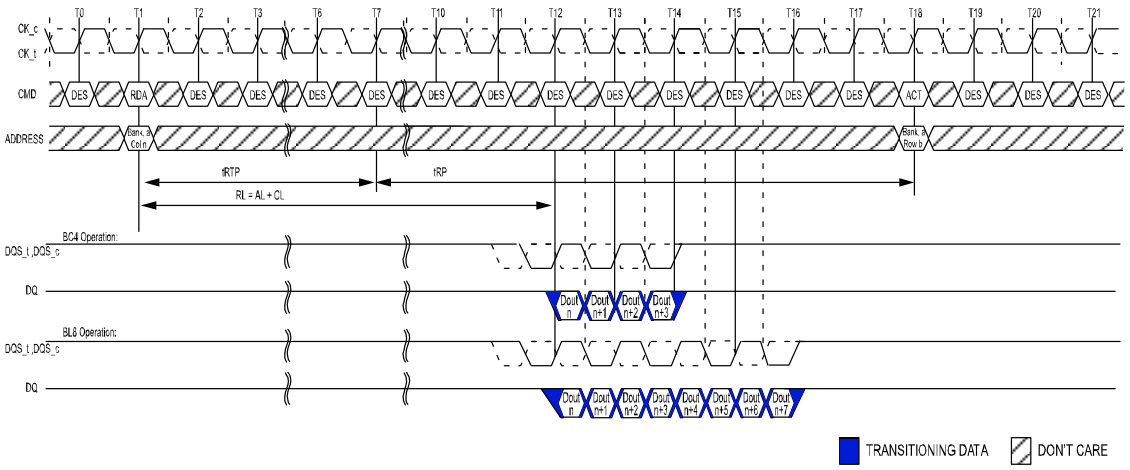
NOTE 2 DOUT n = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 The example assumes tRAS. MIN is satisfied at Precharge command time(T16) and that tRC. MIN is satisfied at the next Active command time(T27).

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable.

READ with Auto Precharge and 1tCK Preamble



NOTE 1 BL = 8, RL = 11 (CL = 11 , AL = 0), Preamble = 1tCK, tRTP = 6, tRP = 11

NOTE 2 DOUT n = data-out from column n.

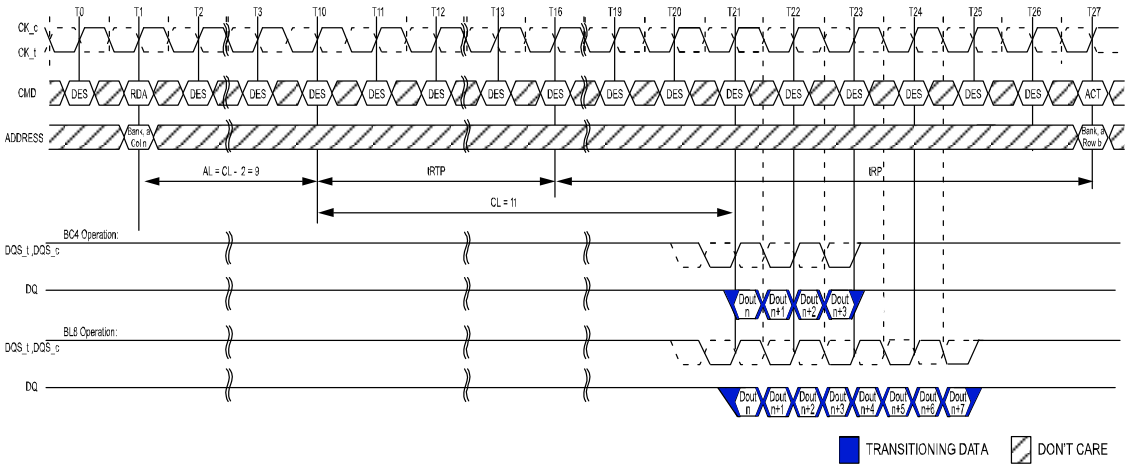
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 tRTP = 6 setting activated by MR0 A[11:9] = 001

NOTE 5 The example assumes tRC. MIN is satisfied at the next Active command time(T18).

NOTE 6 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable.

READ with Auto Precharge, Additive Latency and 1tCK Preamble



NOTE 1 BL = 8, RL = 20 (CL = 11, AL = CL- 2), Preamble = 1tCK, tRTP = 6, tRP = 11

NOTE 2 DOUT n = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

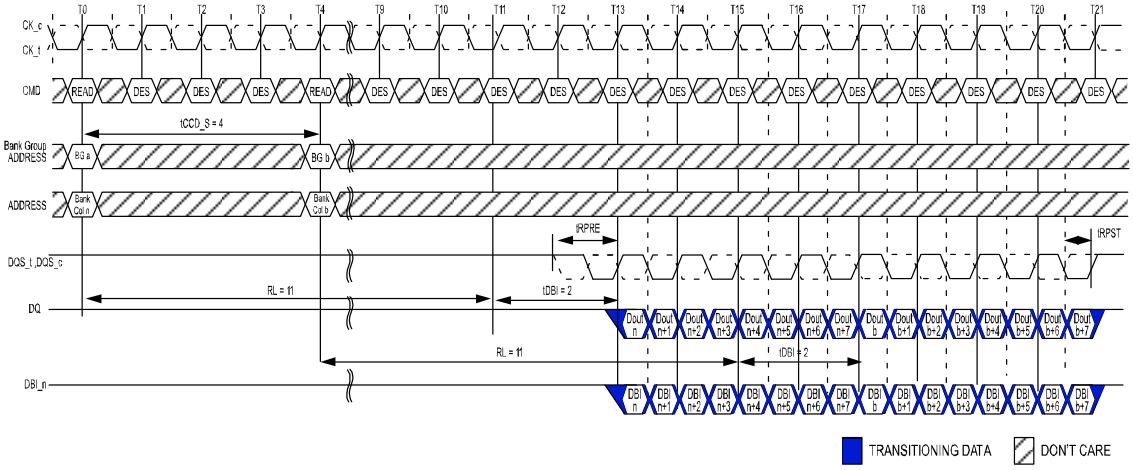
NOTE 4 tRTP = 6 setting activated by MR0 A [11:9] = 001

NOTE 5 The example assumes tRC. MIN is satisfied at the next Active command time(T27).

NOTE 6 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable.

Burst Read Operation with Read DBI (Data Bus Inversion)

Consecutive READ (BL8) with 1tCK Preamble and DBI in Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 1tCK, tDBI = 2tCK

NOTE 2 DOUT n (or b) = data-out from column n (or column b).

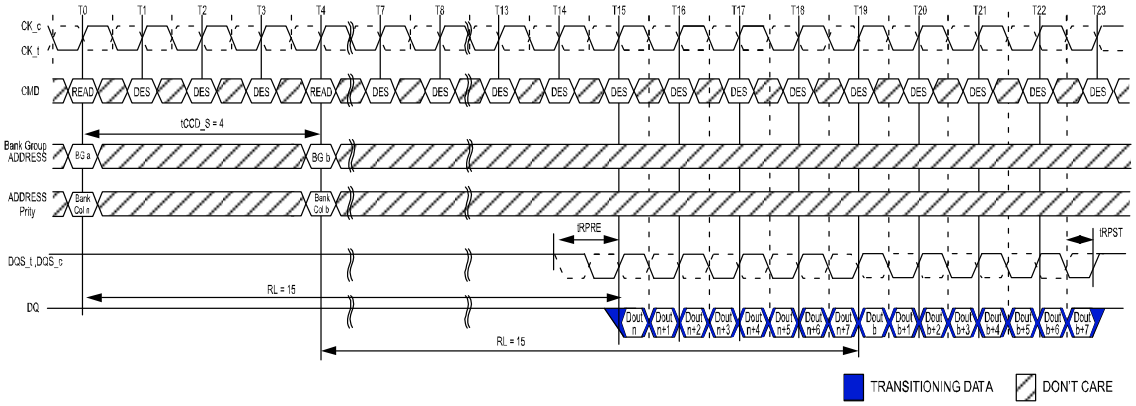
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A [1:0] = 00 or MR0 A [1:0] = 01 and A12 = 1 during READ command at T0 and T4.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, read $\overline{DBI}$ = Enable.

Burst Read Operation with Command/Address Parity

Consecutive READ (BL8) with 1tCK Preamble and CA Parity in Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, PL = 4, (RL = CL + AL + PL = 15), Preamble = 1tCK

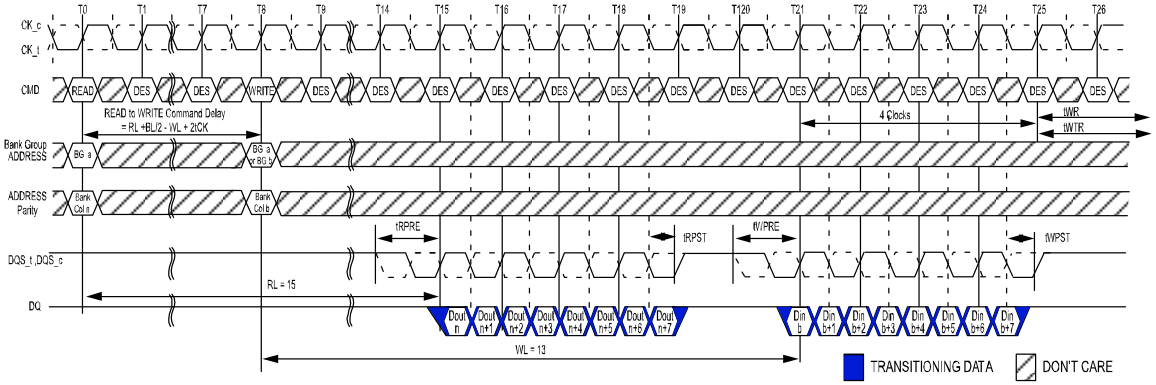
NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A [1:0] = 00 or MR0 A [1:0] = 01 and A12 = 1 during READ command at T0 and T4.

NOTE 5 CA Parity =Enable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable.

READ (BL8) to WRITE (BL8) with 1tCK Preamble and CA parity in Same or Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, PL = 4, (RL = CL + AL + PL = 15), Read Preamble = 1tCK, CWL=9, AL=0, PL=4, (WL=CWL+AL+PL=13), Write Preamble = 1tCK

NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.

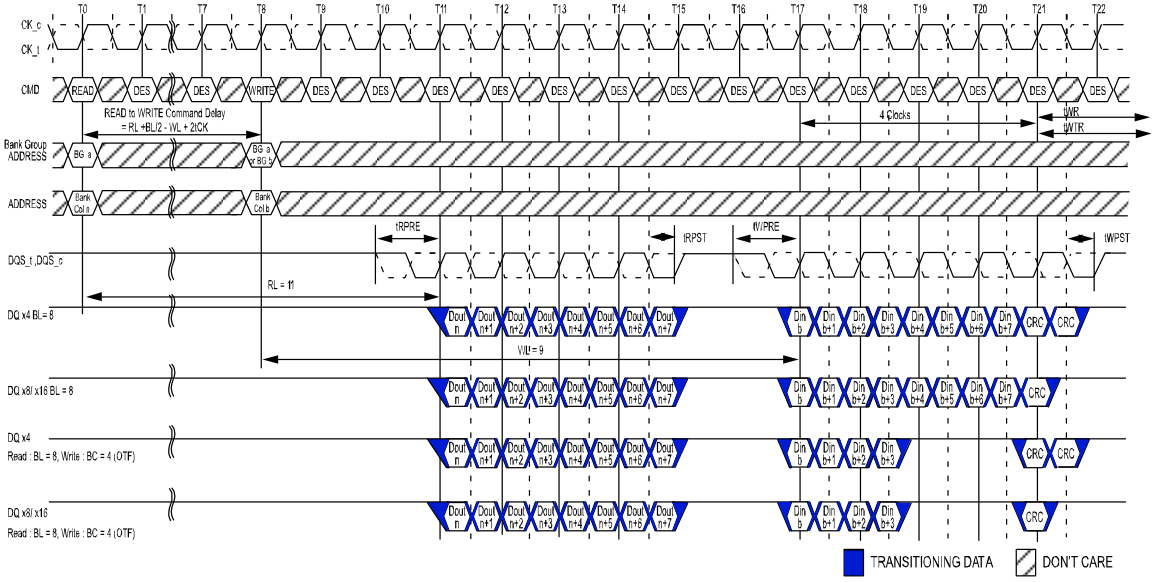
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A [1:0] = 00 or MR0 A [1:0] = 01 and A12 = 1 during READ command at T0 and Write command at T8.

NOTE 5 CA Parity = Enable, $\overline{CS}$ to CA Latency = Disable, Read $\overline{DBI}$ = Disable, Write $\overline{DBI}$ = Disable, Write CRC = Disable.

Read to Write with Write CRC

READ (BL8) to WRITE (BL8 or BC4:OTF) with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE 1 BL = 8 (or BC = 4: OTF for Write), RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL=9 (CWL=9, AL=0), Write Preamble = 1tCK

NOTE 2 DOUT n = data-out from column n. DIN b = data-in to column b.

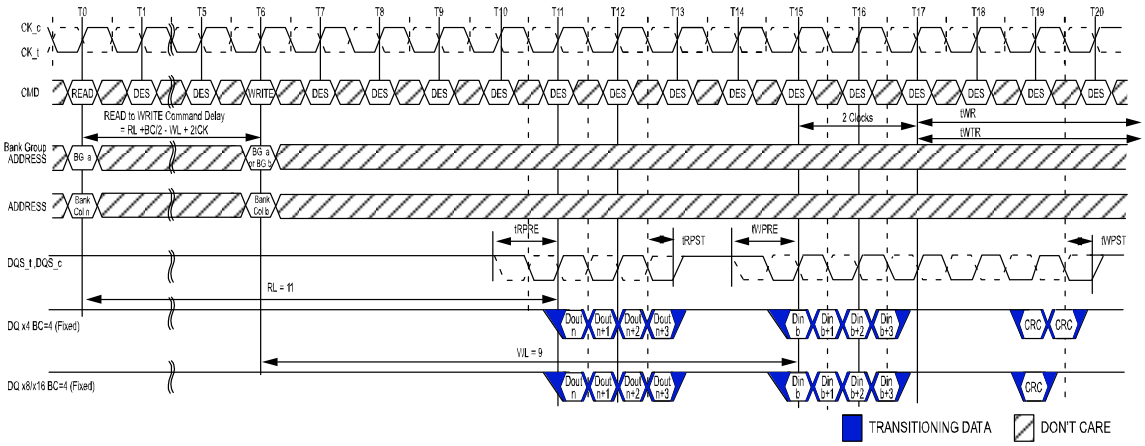
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A [1:0] = 00 or MR0 A [1:0] = 01 and A12 = 1 during READ command at T0 and Write command at T8.

NOTE 5 BC4 setting activated by MR0 A [1:0] = 01 and A12 = 0 during Write command at T8.

NOTE 6 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Enable.

READ (BC4: Fixed) to WRITE (BC4: Fixed) with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE 1 BC = 4 (Fixed), RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL=9 (CWL=9, AL=0), Write Preamble = 1tCK

NOTE 2 DOUT n = data-out from column n. DIN b = data-in to column b.

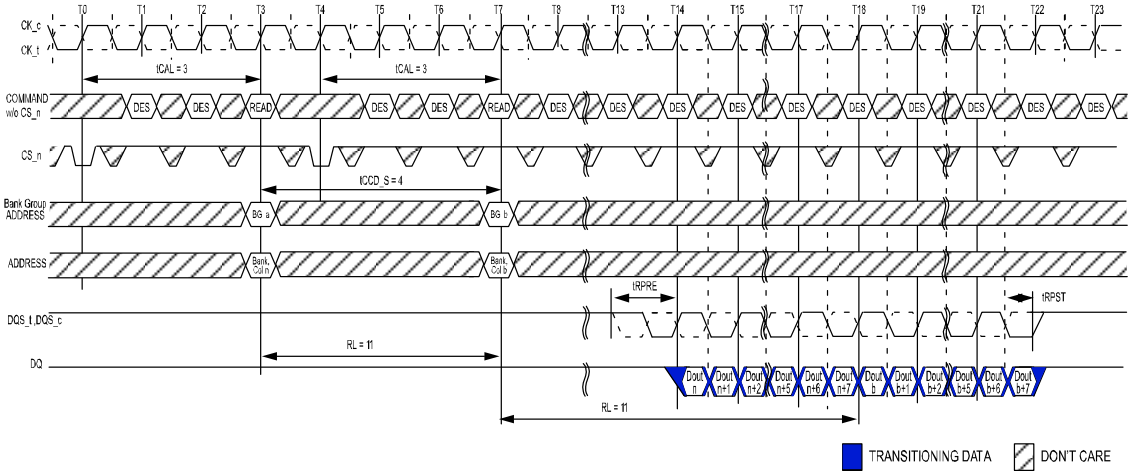
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0 A [1:0] = 10.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, read $\overline{DBI}$ = Disable, Write $\overline{DBI}$ = Disable, Write CRC = Enable.

Read to Read with $\overline{CS}$ to CA Latency

Consecutive READ (BL8) with CAL (3) and 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8 ,AL = 0, CL = 11, CAL = 3, Preamble = 1tCK

NOTE 2 DOUT n (or b) = data-out from column n (or column b).

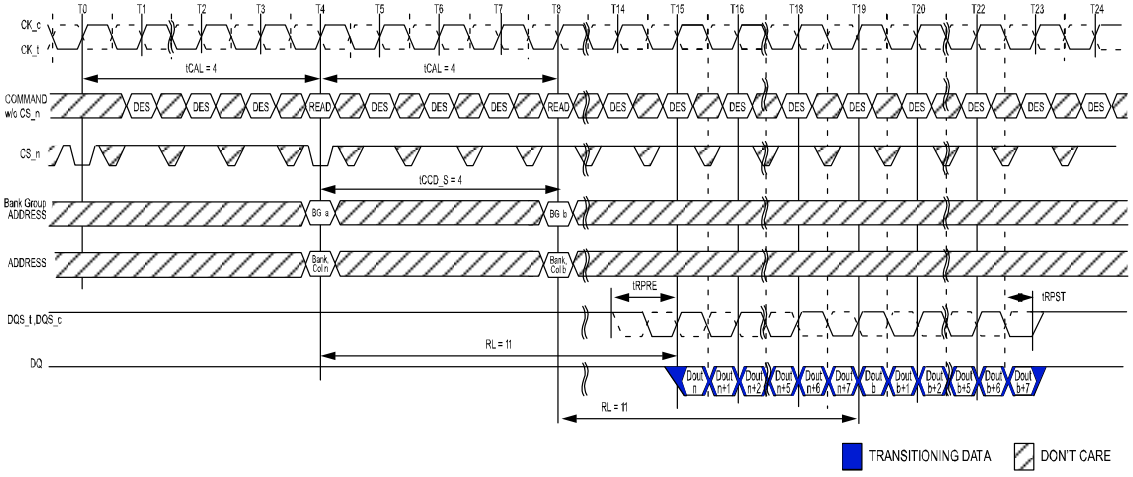
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A [1:0] = 00 or MR0 A [1:0] = 01 and A12 = 1 during READ command at T3 and T7.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Enable, Read $\overline{DBI}$ = Disable.

NOTE 6 Enabling of CAL mode does not impact ODT control timings. Users should maintain the same timing relationship relative to the command/ address bus as when CAL is disabled.

Consecutive READ (BL8) with CAL (4) and 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8, AL = 0, CL = 11, CAL = 4, Preamble = 1tCK

NOTE 2 DOUT n (or b) = data-out from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A [1:0] = 00 or MR0 A [1:0] = 01 and A12 = 1 during READ command at T4 and T8.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Enable, Read DBI = Disable.

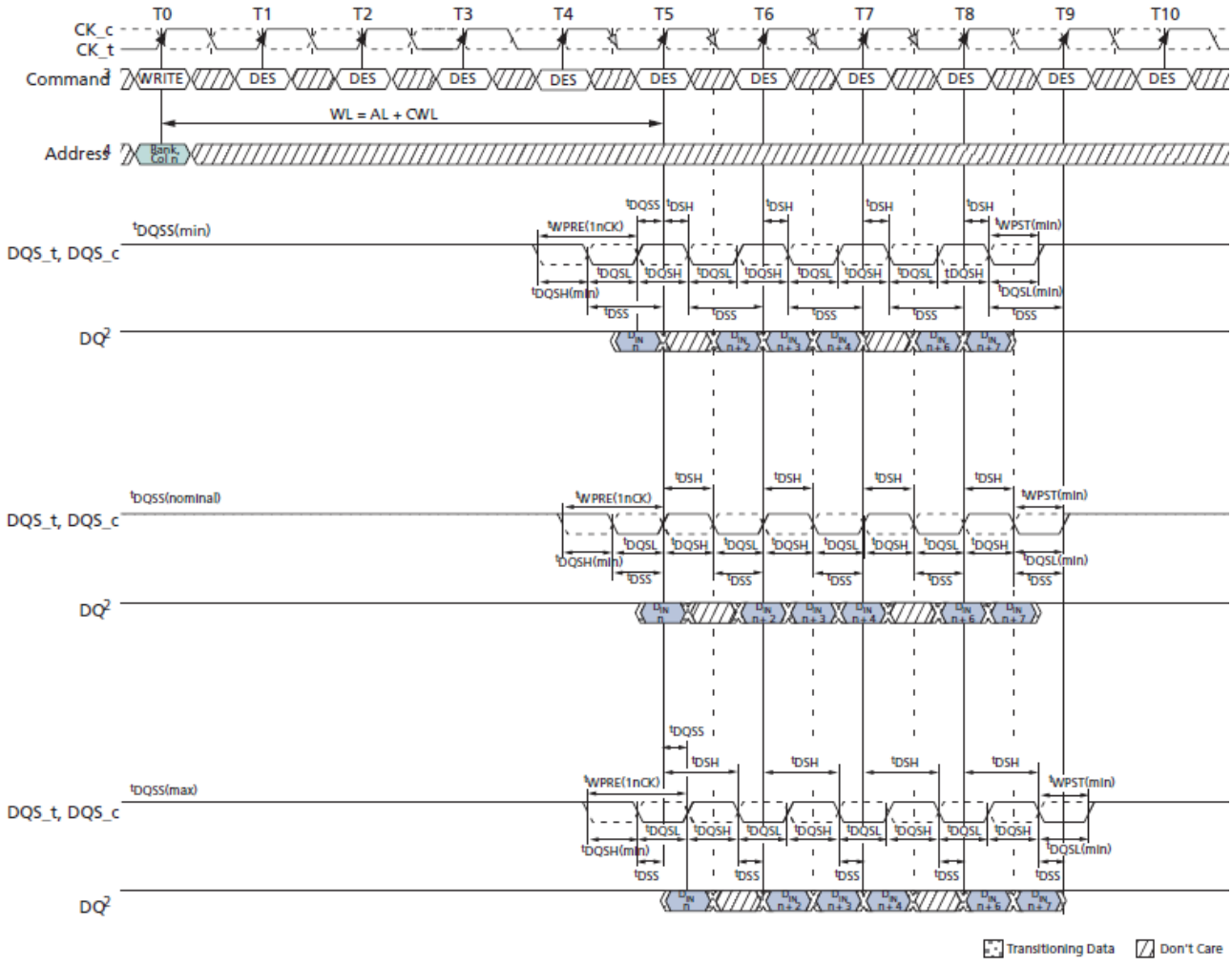
NOTE 6 Enabling of CAL mode does not impact ODT control timings. Users should maintain the same timing relationship relative to the command/ address bus as when CAL is disabled.

WRITE Operation

Write Timing Parameters

This drawing is for example only to enumerate the strobe edges that “belong” to a Write burst. No actual timing violations are shown here. For a valid burst all timing parameters for each edge of a burst need to be satisfied (not only for one edge - as shown).

Write Timing Definition and Parameters with 1tCK Preamble



NOTE 1 BL8, WL = 9 (AL = 0, CWL = 9).

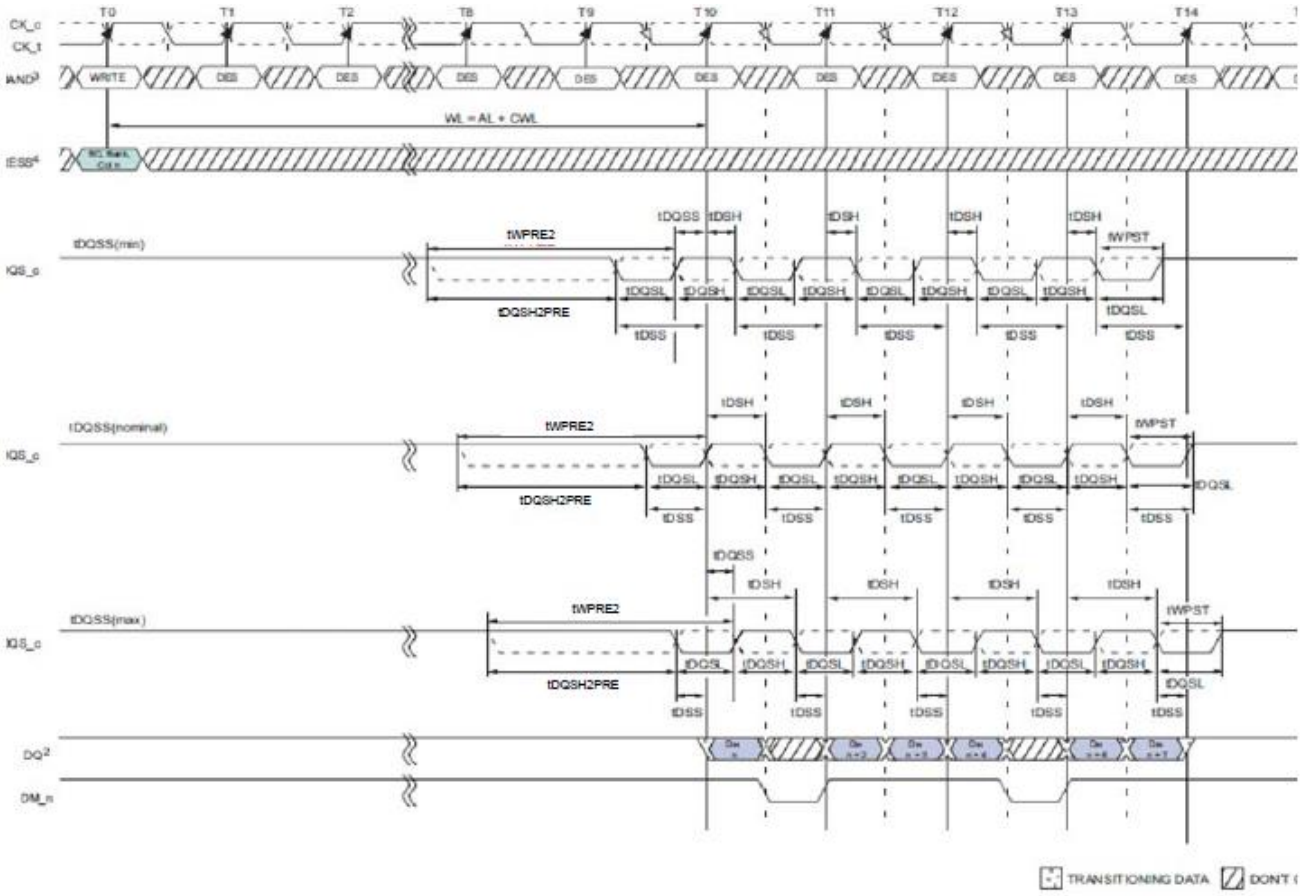
NOTE 2 DINn = data-in from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A [1:0] = 00 or MR0 A[1:0] = 01 and A12 = 1 during WRITE command at T0.

NOTE 5 tDQSS must be met at each rising clock edge.

Write Timing Definition and Parameters with 2tCK Preamble

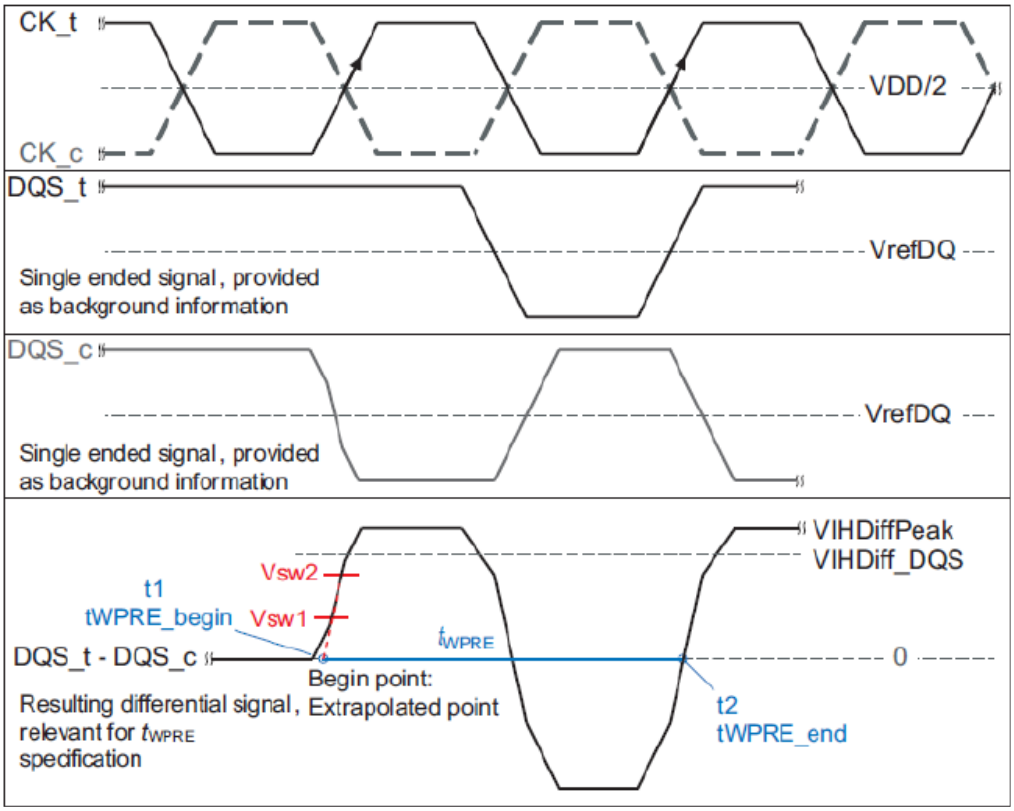


Write Data Mask

One write data mask ($\overline{DM}$) pin for each 8 data bits (DQ) will be supported on DDR4 SDRAMs, consistent with the implementation on DDR3 SDRAMs. It has identical timings on write operations as the data bits as shownabove, and though used in a unidirectional manner, is internally loaded identically to data bits to ensure matched system timing. $\overline{DM}$ is not used during read cycles for any bit organizations including x4, x8, and x16, however, $\overline{DM}$ of x8 bit organization can be used as TDQS_t during write cycles if enabled by the MR1[A11] setting and x8 /x16 organization as $\overline{DBI}$ during write cycles if enabled by the MR5[A11] setting. See "$\overline{TDQS}$, TDQS" on page TBD for more details on TDQS vs. $\overline{DM}$ operations and $\overline{DBI}$ on page TBD for more detail on $\overline{DBI}$ vs. $\overline{DM}$ operations.

tWPRE Calculation

Method for calculating tWPRE transitions and endpoints



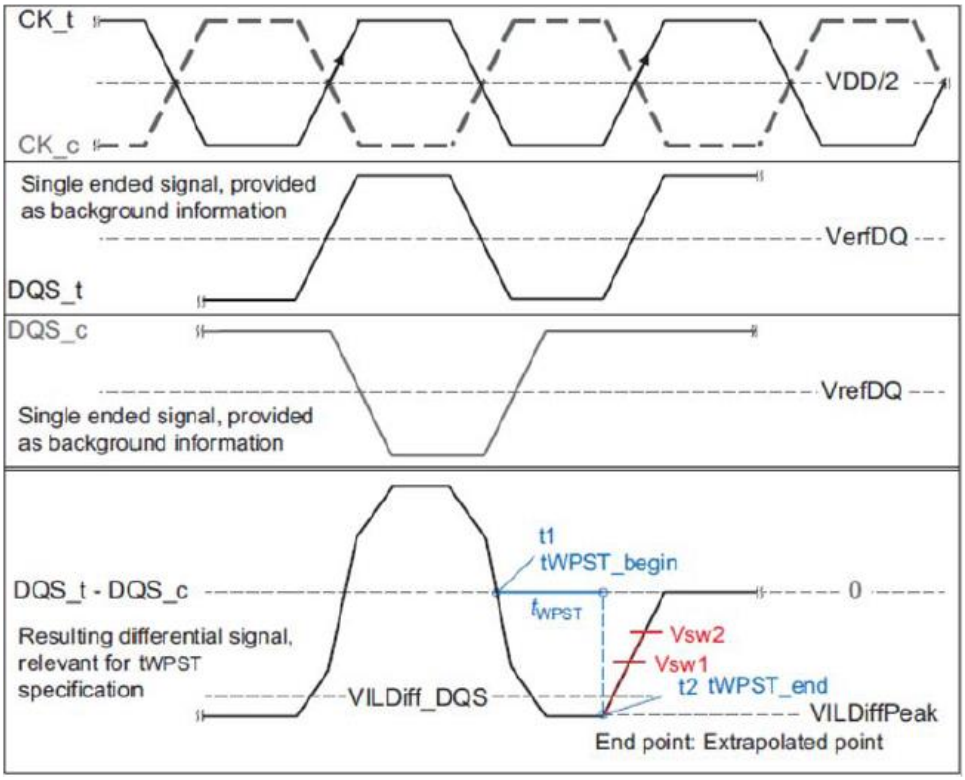
Reference Voltage for tWPRE Timing Measurements

Measured Parameter Symbol	Measured Parameter	Vsw1[V]	Vsw2[V]
tWPRE	DQS, $\overline{DQS}$ differential WRITE Preamble	VIHDiff_DQS x 0.1	VIHDiff_DQS x 0.9

NOTE 1 The method for calculating differential pulse widths for tWPRE2 is same as tWPRE.

tWPST Calculation

Method for calculating tWPST transitions and endpoints



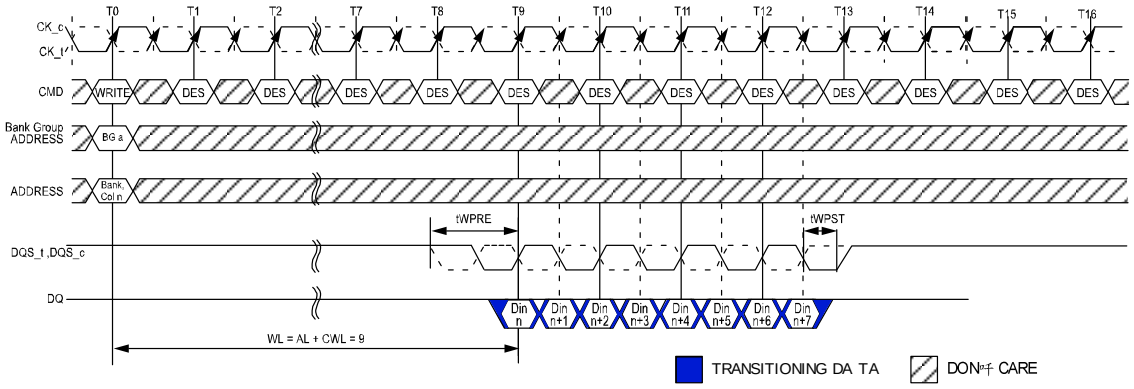
Reference Voltage for tWPST Timing Measurements

Measured Parameter Symbol	Measured Parameter	Vsw1[V]	Vsw2[V]
tWPST	DQS, $\overline{DQS}$ differential WRITE Postamble	VILDiff_DQS x 0.9	VILDiff_DQS x 0.1

WRITE Burst Operation

The following write timing diagrams are to help understanding of each write parameter's meaning and are just examples. The details of the definition of each parameter will be defined separately. In these write timing diagram, CK and DQS are shown aligned and also DQS and DQ are shown center aligned for illustration purpose.

WRITE Burst Operation, WL = 9 (AL = 0, CWL = 9, BL8)



NOTE 1 BL8, WL = 0, AL = 0, CWL = 9, Preamble = 1 tCK.

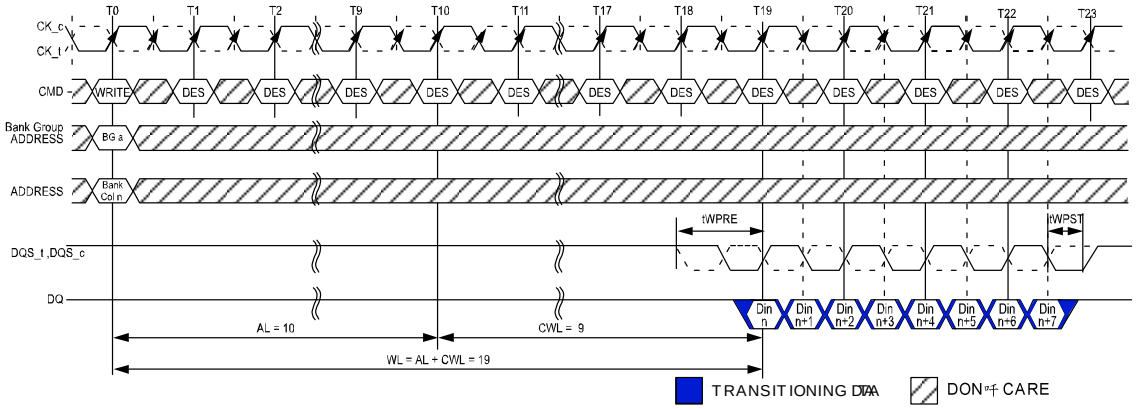
NOTE 2 DINn = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A [1:0] = 00 or MR0 A [1:0] = 01 and A12 = 1 during WRITE command at T0.

NOTE 5 C/A Parity = Disable, $\overline{CS}$ to C/A Latency = Disable, Read $\overline{DBI}$ = Disable.

WRITE Burst Operation, WL = 19 (AL = 10, CWL = 9, BL8)



NOTE 1 BL8, WL = 19, AL = 10 (CL - 1), CWL = 9, Preamble = 1 tCK.

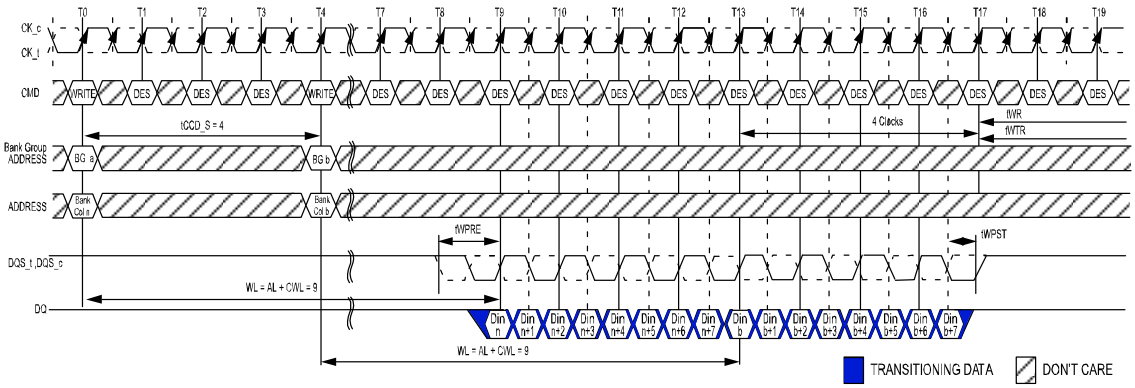
NOTE 2 DINn = data-out from column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A [1:0] = 00 or MR0 A [1:0] = 01 and A12 = 1 during WRITE command at T0.

NOTE 5 C/A Parity = Disable, $\overline{CS}$ to C/A Latency = Disable, Read DBI = Disable.

Consecutive WRITE (BL8) with 1tCK Preamble in Different Bank Group



NOTE 1 BL8, AL = 0, CWL = 9, Preamble = 1 tCK.

NOTE 2 DIN n (or b) = data-in from column n (or column b).

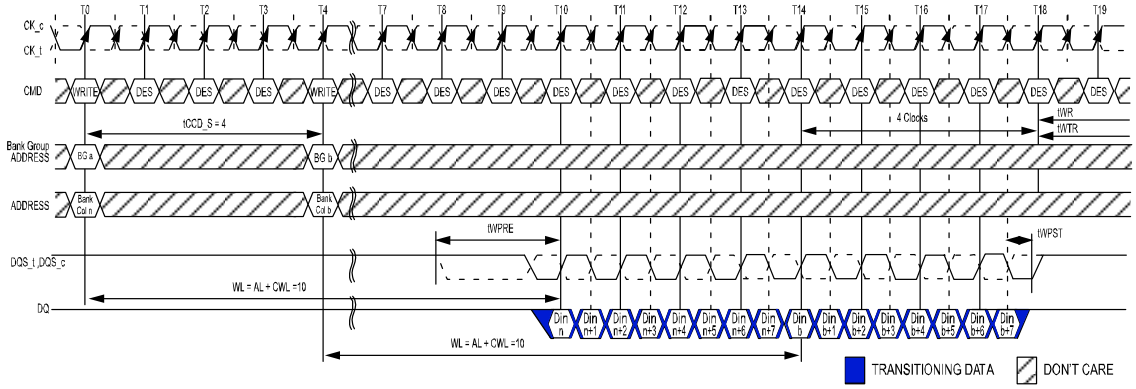
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A [1:0] = 00 or MR0 A [1:0] = 01 and A12 = 1 during WRITE commands at T0 and T4.

NOTE 5 CA parity = disable, $\overline{CS}$ to CA latency = disable, Write $\overline{DBI}$ = disable

NOTE6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

Consecutive WRITE (BL8) with 2tCK Preamble in Different Bank Group



NOTE 1 BL8, AL = 0, CWL = 9+1=10[7], Preamble = 2 tCK.

NOTE 2 DIN n (or b) = data-in from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

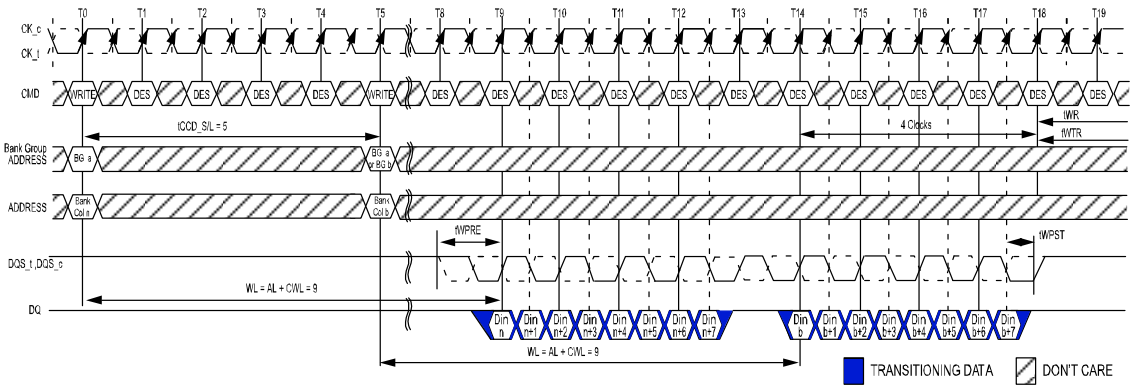
NOTE 4 BL8 setting activated by either MR0 A [1:0] = 00 or MR0 A [1:0] = 01 and A12 = 1 during WRITE commands at T0 and T4.

NOTE 5 CA parity = disable, $\overline{CS}$ to CA latency = disable, Write $\overline{DBI}$= disable

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

NOTE 7 When operating in 2tCK Write Preamble Mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

Nonconsecutive WRITE (BL8) with 1 tCK Preamble in Same or Different Bank Group



NOTE 1 BL8, AL = 0, CWL = 9, Preamble = 1 tCK, tCCD_S/L = 5 tCK.

NOTE 2 DIN n (or b) = data-in from column n (or column b).

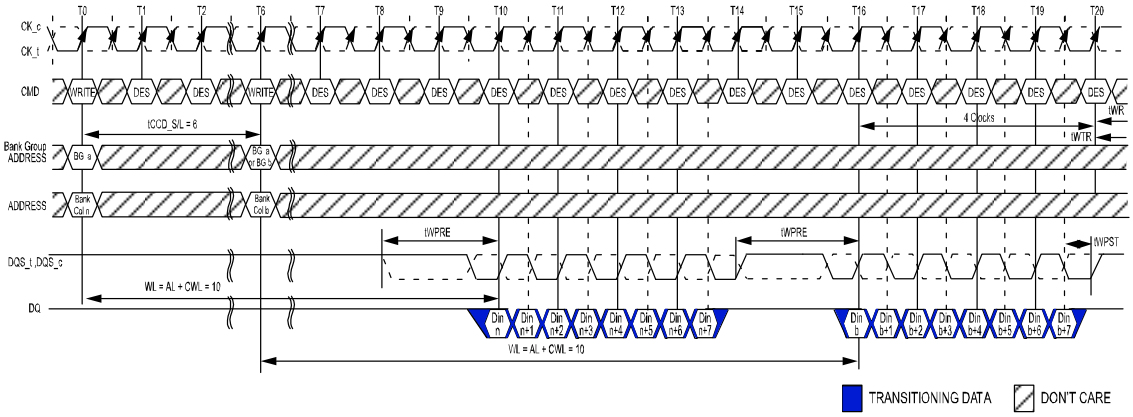
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A [1:0] = 00 or MR0 A [1:0] = 01 and A12 = 1 during WRITE commands at T0 and T5.

NOTE 5 CA parity = disable, $\overline{CS}$ to CA latency = disable, Write $\overline{DBI}$ = disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.

Nonconsecutive WRITE (BL8) with 2 tCK Preamble in Same or Different Bank Group



NOTE 1 BL8, AL = 0, CWL = 9+1=10[8], Preamble = 2 tCK, tCCD_S/L = 6 tCK.

NOTE 2 DIN n (or b) = data-in from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A [1:0] = 00 or MR0 A [1:0] = 01 and A12 = 1 during WRITE commands at T0 and T6.

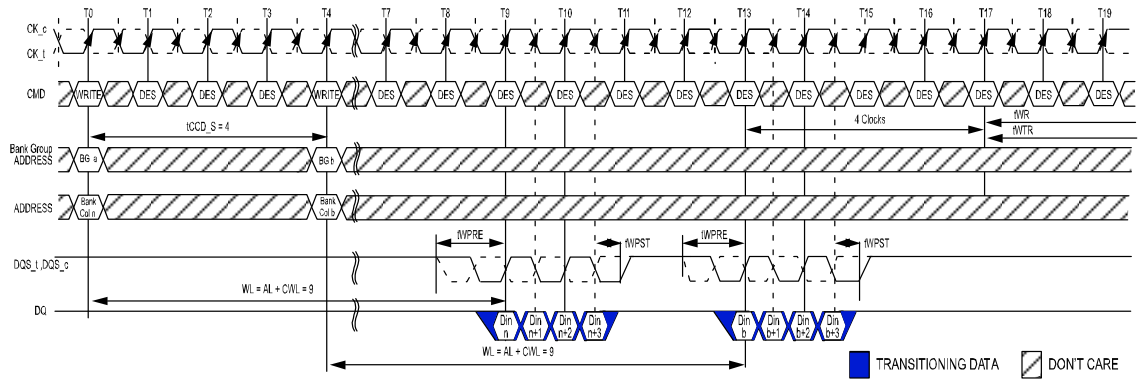
NOTE 5 CA parity = disable, $\overline{CS}$ to CA latency = disable, Write DBI = disable.

NOTE 6 tCCD_S/L = 5 isn't allowed in 2tCK preamble mode.

NOTE 7 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T20.

NOTE 8 When operating in 2tCK Write Preamble Mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

WRITE (BC4) OTF to WRITE (BC4) OTF with 1 tCK Preamble in Different Bank Group



NOTE 1 BC4, AL = 0, CWL = 9, Preamble = 1 tCK.

NOTE 2 DIN n (or b) = data-in from column n (or column b).

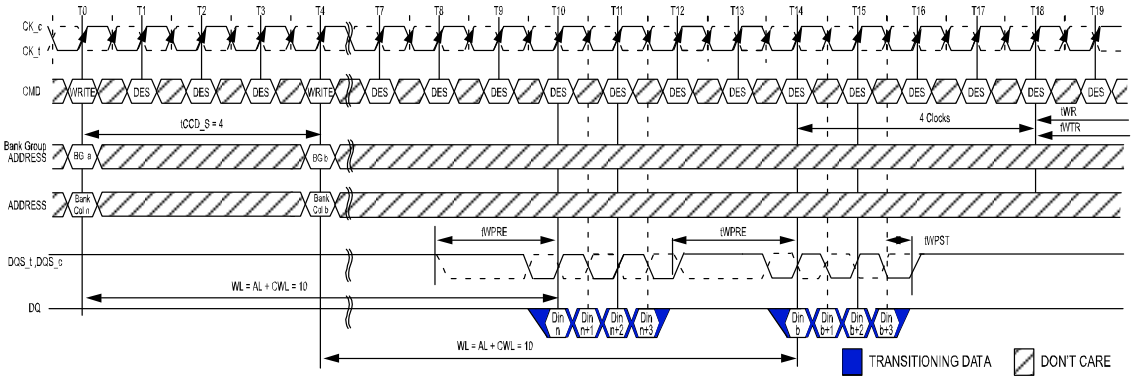
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0 A [1:0] = 01 and A12 = 0 during WRITE commands at T0 and T4.

NOTE 5 CA parity = disable, $\overline{CS}$ to CA latency = disable, Write $\overline{DBI}$ = disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

WRITE (BC4) OTF to WRITE (BC4) OTF with 2 tCK Preamble in Different Bank Group



NOTE 1 BC=4, AL = 0, CWL = 9+1=10[7], Preamble = 2 tCK.

NOTE 2 DIN n (or b) = data-in from column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

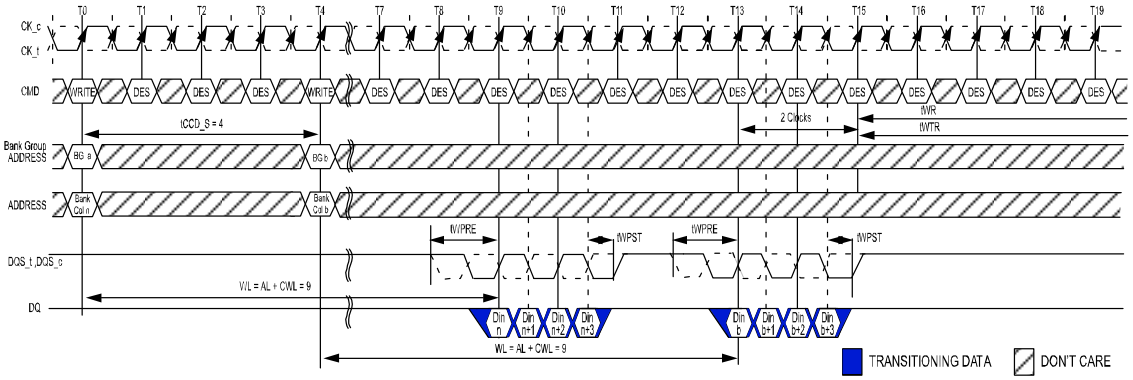
NOTE 4 BC4 setting activated by MR0 A [1:0] = 01 and A12 = 0 during WRITE commands at T0 and T4.

NOTE 5 CA parity = disable, $\overline{CS}$ to CA latency = disable, Write $\overline{DBI}$ = disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.

NOTE 7 When operating in 2tCK Write Preamble Mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

WRITE (BC4) Fixed to WRITE (BC4) Fixed with 1 tCK Preamble in Different Bank Group



NOTE 1 BC = 4, AL = 0, CWL = 9, Preamble = 1 tCK.

NOTE 2 DIN n (or b) = data-in from column n (or column b).

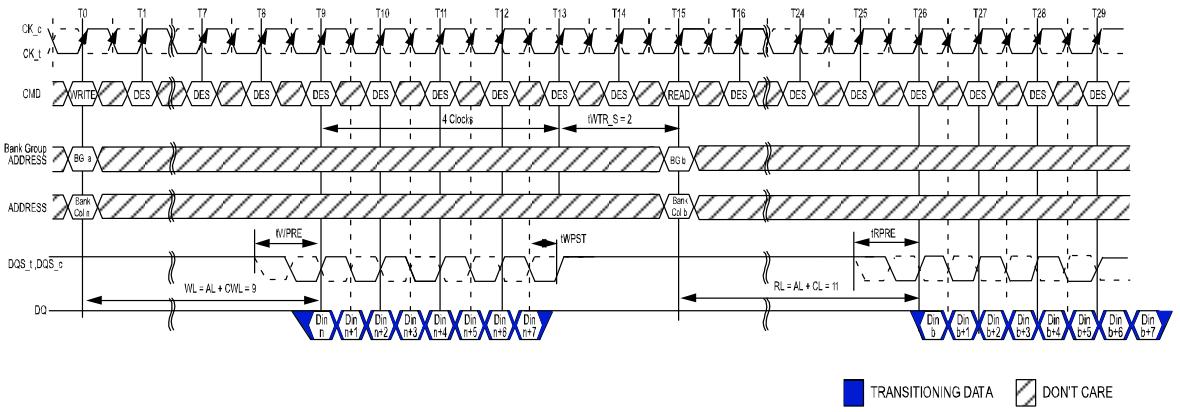
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0 A [1:0] = 10 and A12 = 0 during WRITE commands at T0 and T4.

NOTE 5 CA parity = disable, $\overline{CS}$ to CA latency = disable, Write $\overline{DBI}$ = disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T15.

WRITE (BL8) to READ (BL8) with 1tCK Preamble in Different Bank Group



NOTE 1 BL=8, AL =0, CWL = 9, CL = 11, Preamble = 1 tCK

NOTE 2 DIN n (or b) = data-in from column n (or column b).

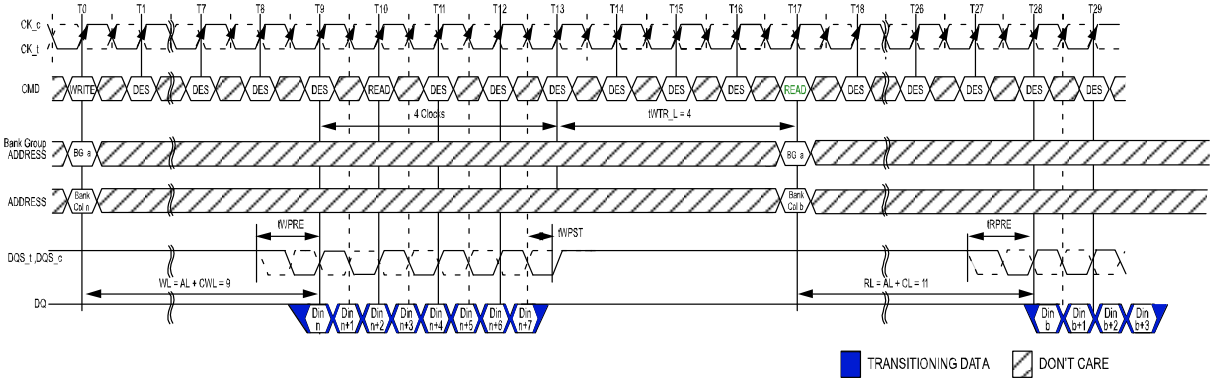
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and READ command at T15.

NOTE 5 CA parity = disable, $\overline{CS}$ to CA latency = disable, Write $\overline{DBI}$ = disable.

NOTE 6 The write timing parameter (tWTR_S) are referenced from the first rising clock edge after the last write data shown at T13. When AL is non-zero, the external read command at T15 can be pulled in by AL.

WRITE (BL8) to READ (BL8) with 1tCK Preamble in Same Bank Group



NOTE 1 BL = 8, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n (or column b). DOUT b = data-out from column b.

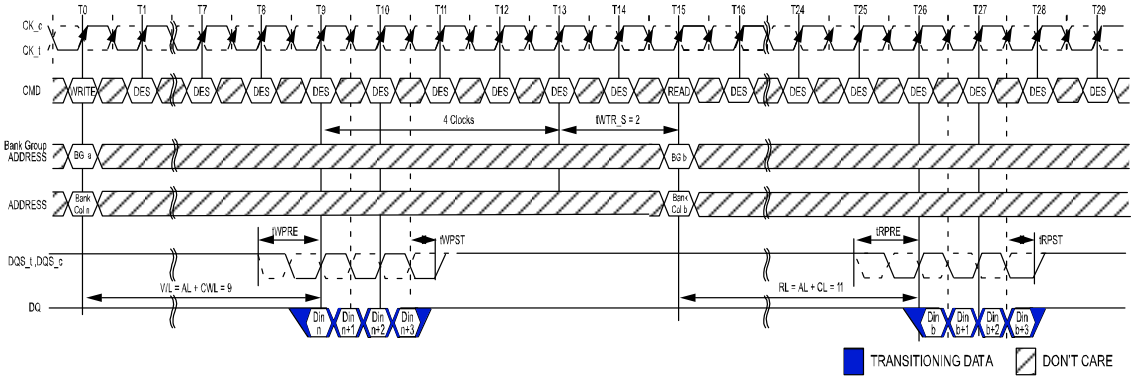
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A[1:0] = 00 or MR0 A[1:0] = 01 and A12 = 1 during WRITE command at T0 and READ command at T17.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write $\overline{DBI}$ = Disable.

NOTE 6 The write timing parameter (tWTR_L) are referenced from the first rising clock edge after the last write data shown at T13. When AL is non-zero, the external read command at T17 can be pulled in by AL.

WRITE (BC4) OTF to READ (BC) OTF with 1tCK Preamble in Different Bank Group



NOTE 1 BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n (or column b). DOUT b = data-out from column b.

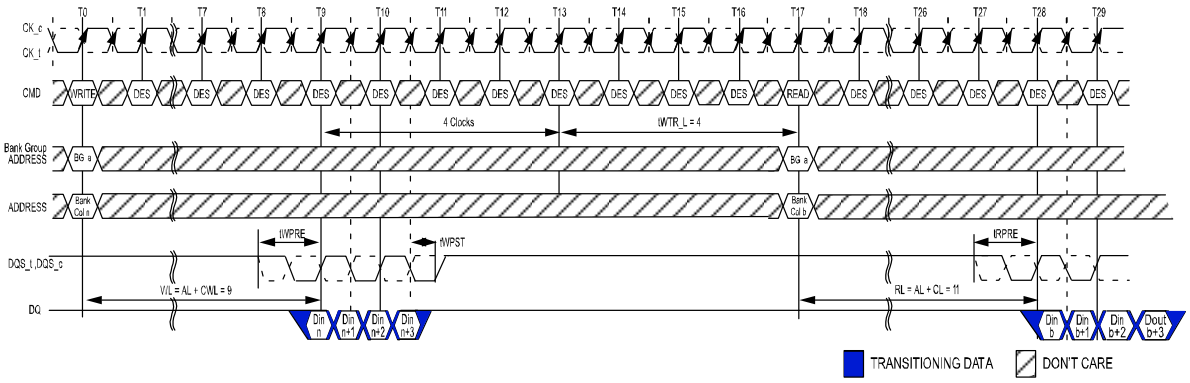
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0 A[1:0] = 01 and A12 = 0 during WRITE command at T0 and READ command at T15.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write $\overline{DBI}$= Disable.

NOTE 6 The write timing parameter (tWTR_S) are referenced from the first rising clock edge after the last write data shown at T13.

WRITE (BC4)OTF to READ (BC4)OTF with 1tCK Preamble in Same Bank Group



NOTE 1 BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n (or column b). DOUT b = data-out from column b.

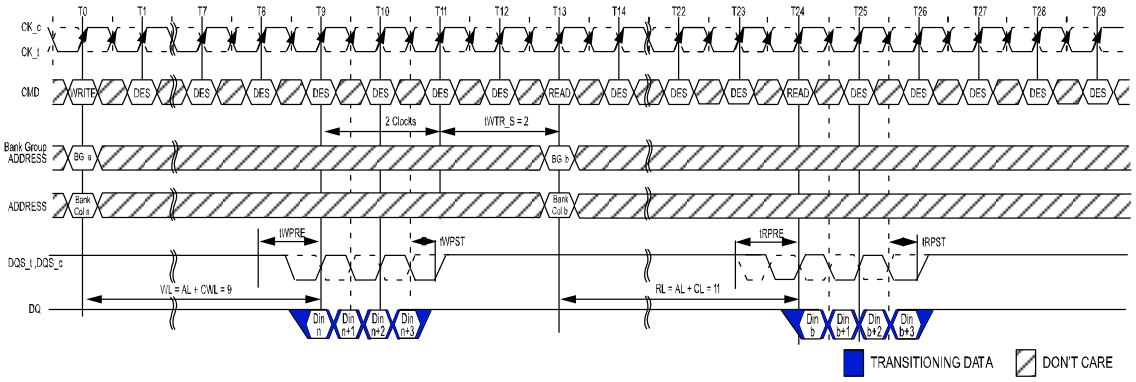
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0 A[1:0] = 01 and A12 = 0 during WRITE command at T0 and READ command at T17.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write DBI = Disable.

NOTE 6 The write timing parameter (tWTR_L) are referenced from the first rising clock edge after the last write data shown at T13. When AL is non-zero, the external read command at T17 can be pulled in by AL.

WRITE (BC4) Fixed to READ (BC4) Fixed with 1tCK Preamble in Different Bank Group



NOTE 1 BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n (or column b). DOUT b = data-out from column b.

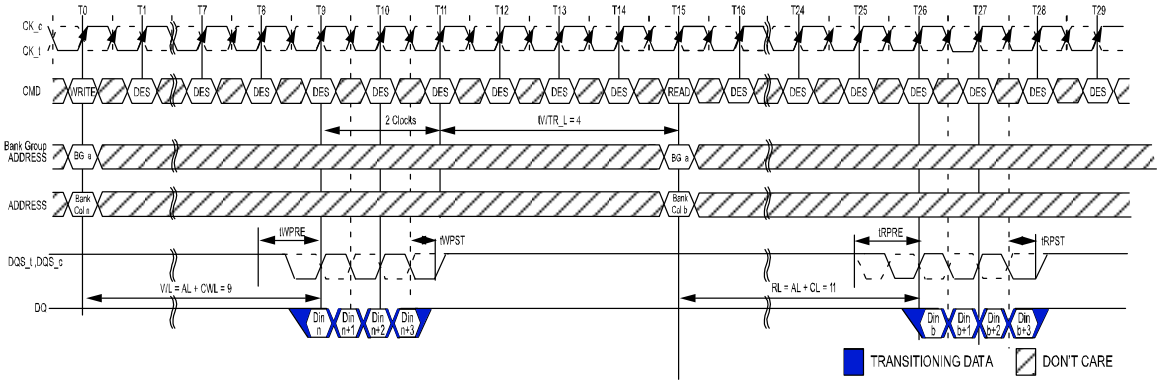
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0 A [1:0] = 10.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write $\overline{DBI}$ = Disable.

NOTE 6 The write timing parameter (tWTR_S) are referenced from the first rising clock edge after the last write data shown at T11. When AL is non-zero, the external read command at T13 can be pulled in by AL

WRITE (BC4) Fixed to READ (BC4) Fixed with 1tCK Preamble in Same Bank Group



NOTE 1 BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n (or column b). DOUT b = data-out from column b.

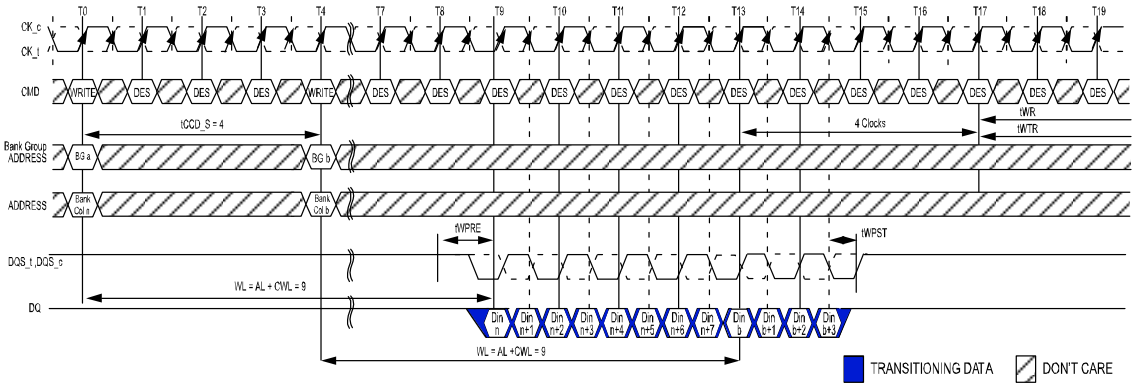
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0 A [1:0] = 10.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write $\overline{DBI}$ = Disable.

NOTE 6 The write timing parameter (tWTR_L) are referenced from the first rising clock edge after the last write data shown at T11. When AL is non-zero, the external read command at T15 can be pulled in by AL.

WRITE (BL8) to WRITE (BC4) OTF with 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK

NOTE 2 DIN n (or b) = data-in to column n (or column b).

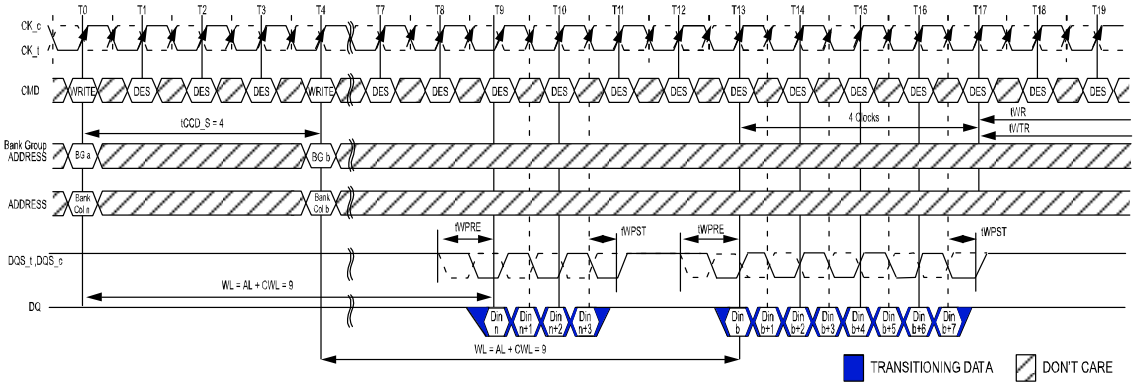
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by MR0 A[1:0] = 01 and A12 =1 during WRITE command at T0.
BC4 setting activated by MR0 A[1:0] = 01 and A12 =0 during WRITE command at T4.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write $\overline{DBI}$ = Disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17

WRITE (BC4) OTF to WRITE (BL8) with 1tCK Preamble in Different Bank Group



NOTE 1 BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK

NOTE 2 DIN n (or b) = data-in to column n (or column b).

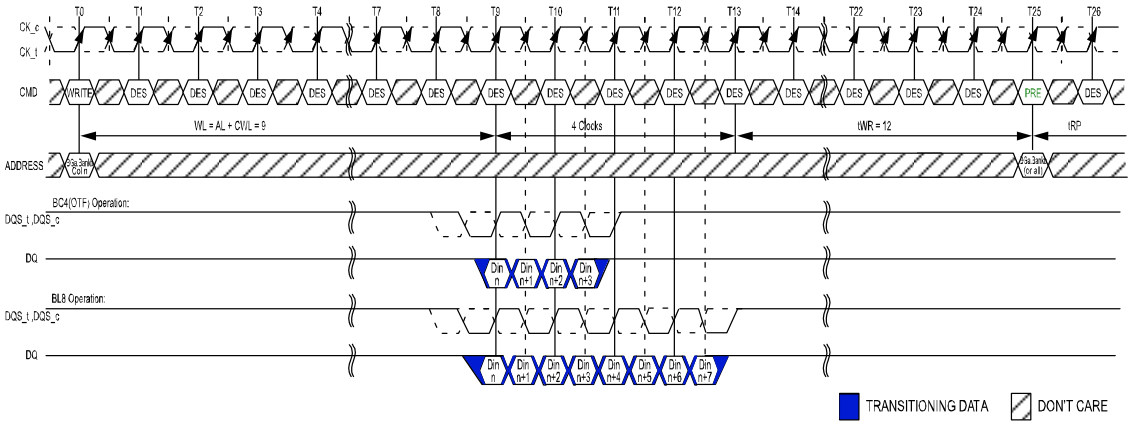
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0 A [1:0] = 01 and A12 =0 during WRITE command at T0.
BL8 setting activated by MR0 A[1:0] = 01 and A12 =1 during WRITE command at T4.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write $\overline{DBI}$ = Disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17

WRITE (BL8/BC4) OTF to PRECHARGE Operation with 1tCK Preamble



NOTE 1 BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, tWR = 12

NOTE 2 DIN n = data-in to column n.

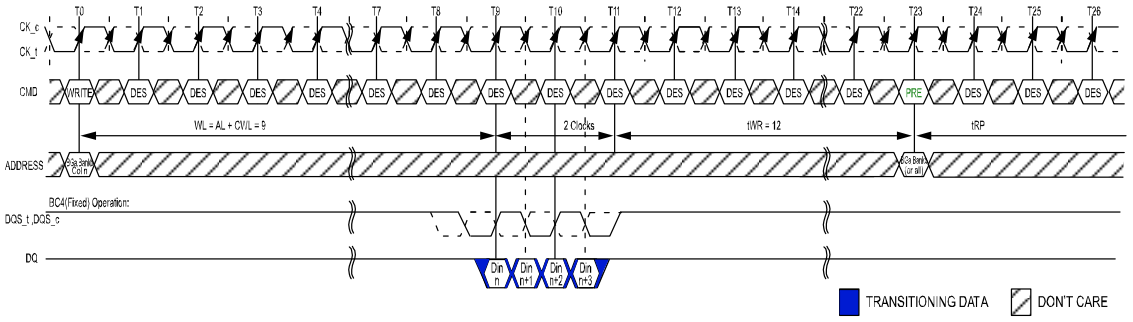
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0 A[1:0] = 01 and A12 =0 during WRITE command at T0.
BL8 setting activated by MR0 A[1:0] = 00 or MR0 A[1:0] = 01 and A12 =1 during WRITE command at T0.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write $\overline{DBI}$ = Disable.

NOTE 6 The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T13. tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.

WRITE (BC4) Fixed to PRECHARGE Operation with 1tCK Preamble



NOTE 1 BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, tWR = 12

NOTE 2 DIN n = data-in to column n.

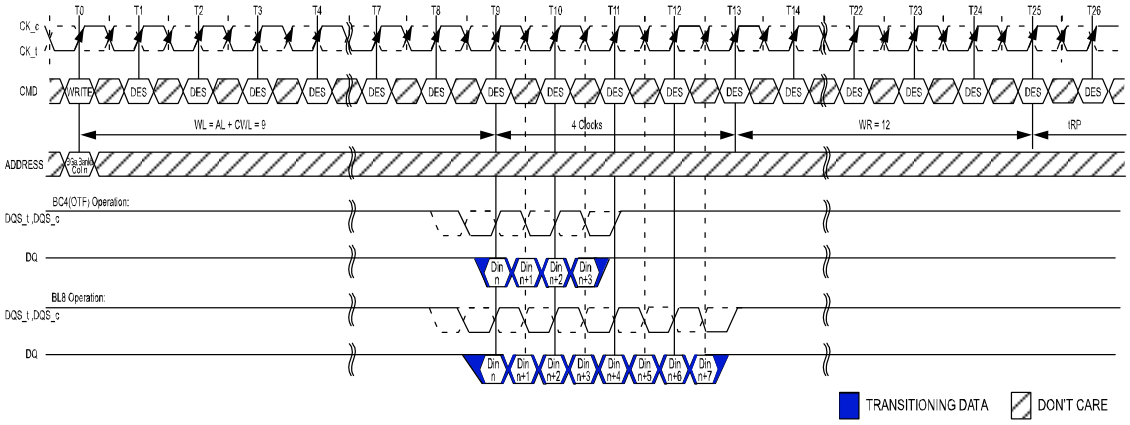
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0 A[1:0] = 10.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write $\overline{DBI}$ = Disable.

NOTE 6 The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T11. tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.

WRITE (BL8/BC4) OTF with Auto PRECHARGE Operation and 1tCK Preamble



NOTE 1 BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, WR = 12

NOTE 2 DIN n = data-in to column n.

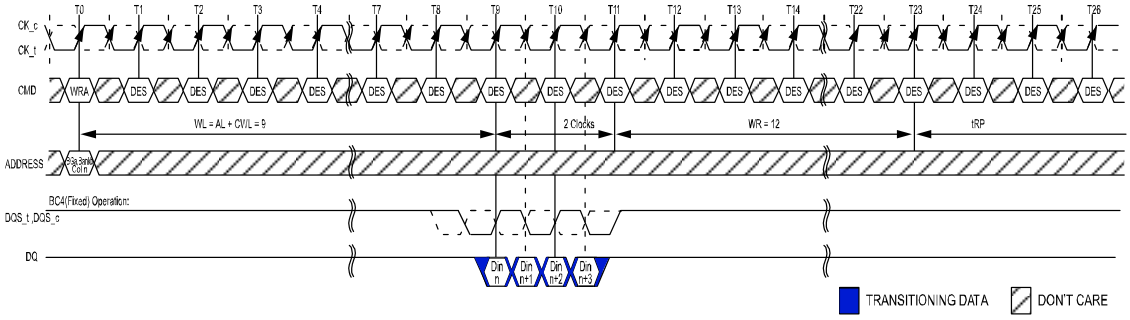
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0 A[1:0] = 01 and A12 =0 during WRITE command at T0.
BL8 setting activated by either MR0 A[1:0] = 00 or MR0 A[1:0] = 01 and A12 =1 during WRITE command at T0.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write $\overline{DBI}$ = Disable.

NOTE 6 The write recovery time (WR) is referenced from the first rising clock edge after the last write data shown at T13. WR specifies the last burst write cycle until the precharge command can be issued to the same bank.

WRITE (BC4) Fixed with Auto PRECHARGE Operation and 1tCK Preamble



NOTE 1 BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, WR = 12

NOTE 2 DIN n = data-in to column n.

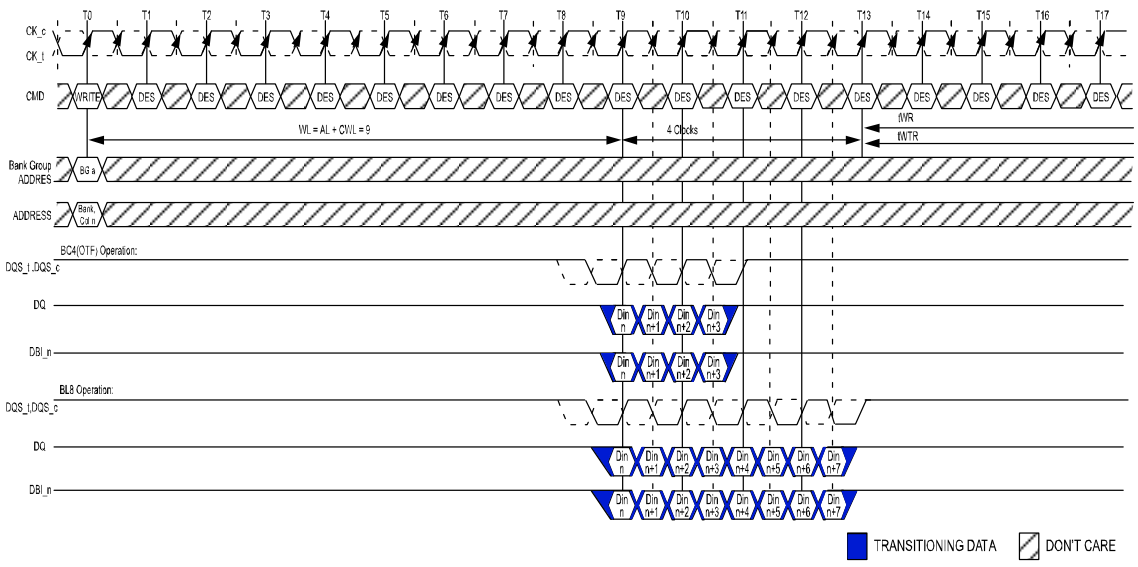
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0 A[1:0] = 10.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write $\overline{DBI}$ = Disable.

NOTE 6 The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T11. WR specifies the last burst write cycle until the precharge command can be issued to the same bank.

WRITE (BL8/BC4) OTF with 1tCK Preamble and DBI



NOTE 1 BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n.

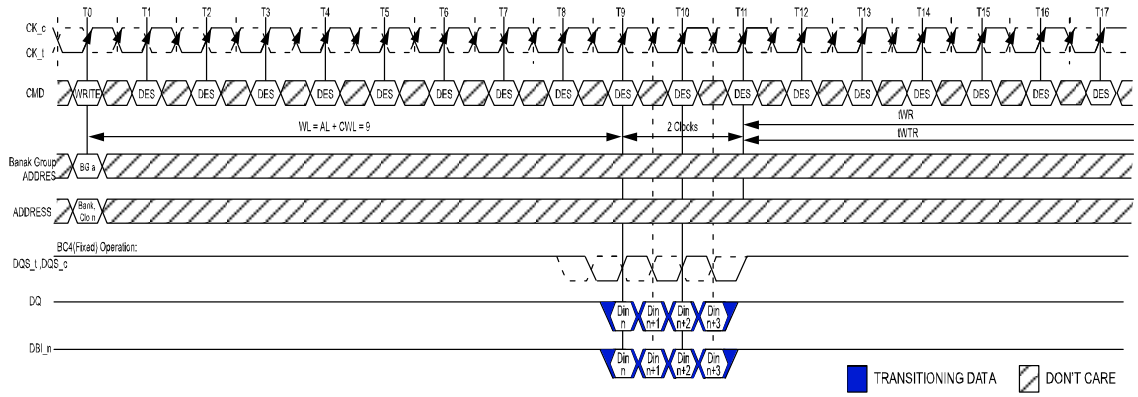
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0 A[1:0] = 01 and A12 =0 during WRITE command at T0.
BL8 setting activated by either MR0 A [1:0] = 00 or MR0 A [1:0] = 01 and A12 =1 during WRITE command at T0.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write $\overline{DBI}$ = Enable.

NOTE 6 The write recovery time (tWR_DBI) and write timing parameter (tWTR_DBI) are referenced from the first rising clock edge after the last write data shown at T13.

WRITE (BC4) Fixed with 1tCK Preamble and DBI



NOTE 1 BC = 4, AL = 0, CWL = 9, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n.

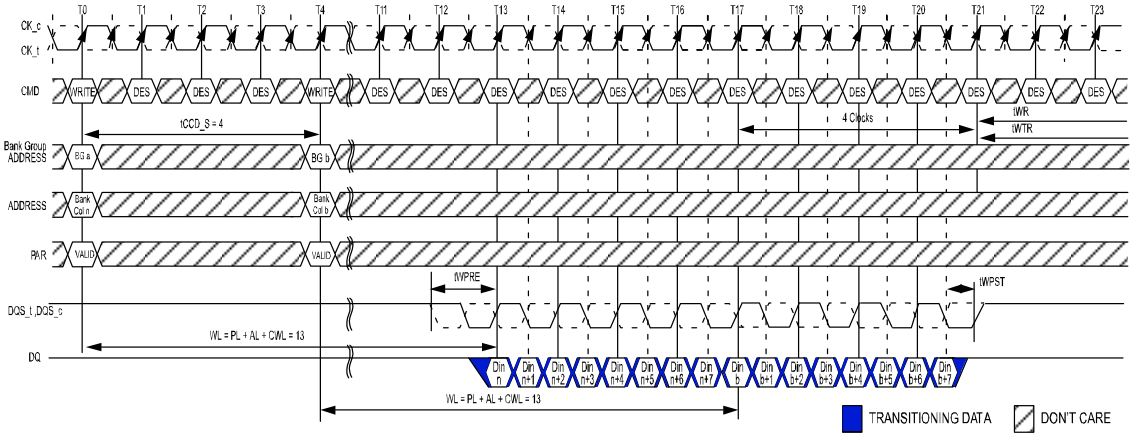
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0 A [1:0] = 10.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write $\overline{DBI}$ = Enable, CRC = Disable.

NOTE 6 The write recovery time (tWR_DBI) and write timing parameter (tWTR_DBI) are referenced from the first rising clock edge after the last write data shown at T11.

Consecutive WRITE (BL8) with 1tCK Preamble and CA Parity in Different Bank Group



NOTE 1 BL = 8, AL = 0, CWL = 9, PL = 4, Preamble = 1tCK

NOTE 2 DIN n (or b) = data-in to column n (or column b).

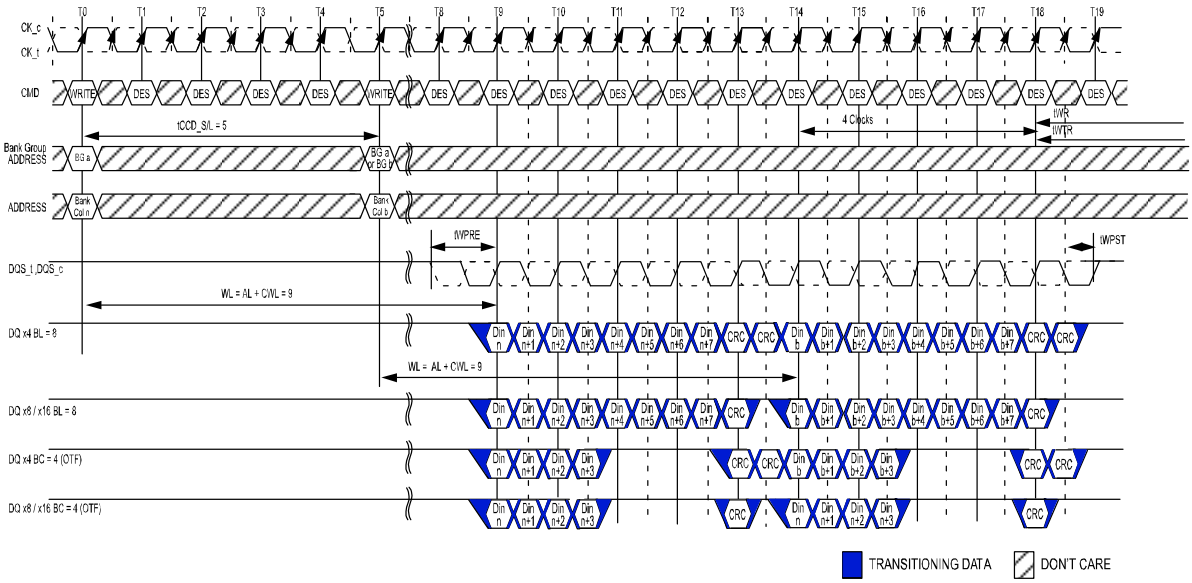
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A [1:0] = 00 or MR0 A[1:0] = 01 and A12 =1 during WRITE command at T0 and T4.

NOTE 5 CA Parity = Enable, $\overline{CS}$ to CA Latency = Disable, Write $\overline{DBI}$ = Disable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T21.

Consecutive WRITE (BL8/BC4) OTF with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE 1 BL = 8/BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 5

NOTE 2 DIN n (or b) = data-in to column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

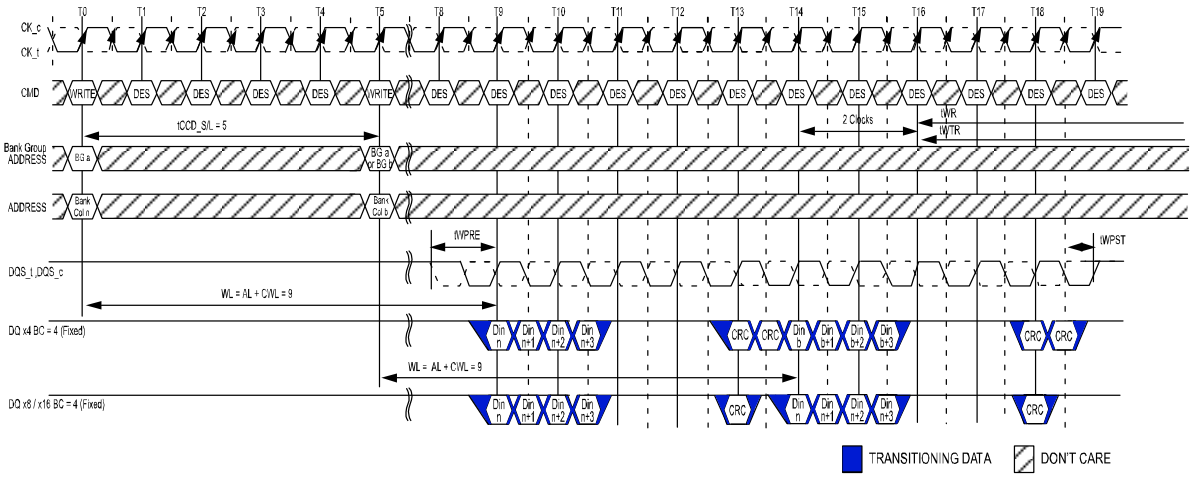
NOTE 4 BL8 setting activated by either MR0 A [1:0] = 00 or MR0 A [1:0] = 01 and A12 = 1 during WRITE command at T0 and T5.

NOTE 5 BC4 setting activated by MR0 A [1:0] = 01 and A12 = 0 during WRITE command at T0 and T5.

NOTE 6 C/A Parity = Disable, $\overline{CS}$ to C/A Latency = Disable, Write $\overline{DBI}$ = Disable, Write CRC = Enable.

NOTE 7 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18

Consecutive WRITE (BC4) Fixed with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE 1 BL = 8, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 5

NOTE 2 DIN n (or b) = data-in to column n (or column b).

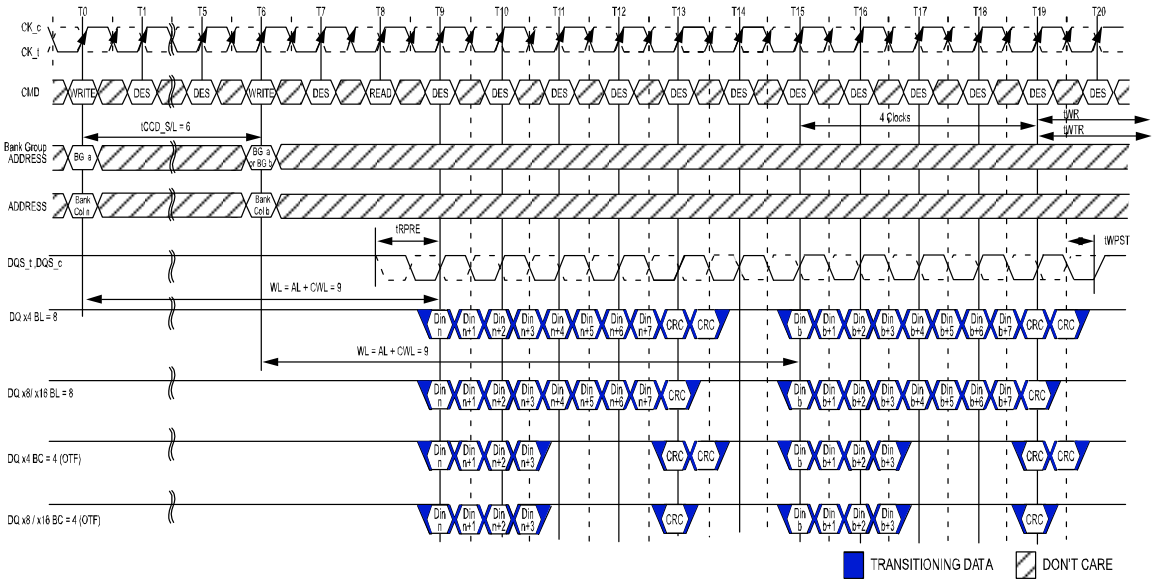
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BC4 setting activated by MR0 A [1:0] = 10 at T0 and T5.

NOTE 5 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write DBI = Disable, Write CRC = Enable.

NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T16.

Nonconsecutive WRITE (BL8/BC4) OTF with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE 1 BL = 8, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 6

NOTE 2 DIN n (or b) = data-in to column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

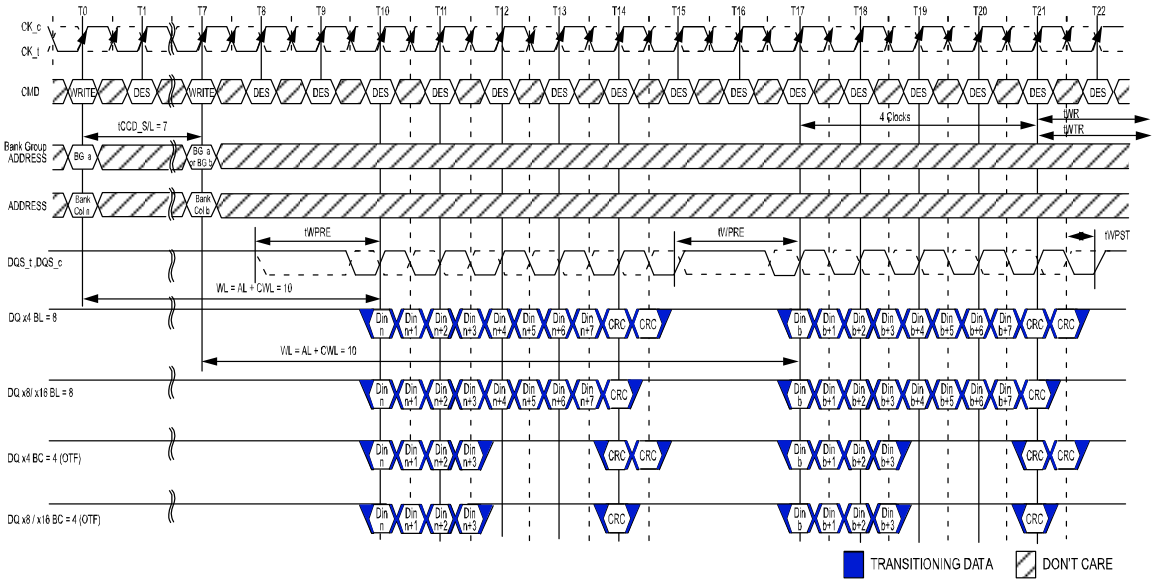
NOTE 4 BL8 setting activated by either MR0 A [1:0] = 00 or MR0 A[1:0] = 01 and A12 =1 during WRITE command at T0 and T6.

NOTE 5 BC4 setting activated by MR0 A [1:0] = 01 and A12 =0 during WRITE command at T0 and T6.

NOTE 6 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write $\overline{DBI}$ = Disable, Write CRC = Enable.

NOTE 7 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T19.

Nonconsecutive WRITE (BL8/BC4) OTF with 2tCK Preamble and Write CRC in Same or Different Bank Group



NOTE 1 BL = 8, AL = 0, CWL = 9 + 1 = 10^{9}, Preamble = 2tCK, tCCD_S/L = 7

NOTE 2 DIN n (or b) = data-in to column n (or column b).

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A [1:0] = 00 or MR0 A [1:0] = 01 and A12 =1 during WRITE command at T0 and T7.

NOTE 5 BC4 setting activated by MR0 A [1:0] = 01 and A12 =0 during WRITE command at T0 and T7.

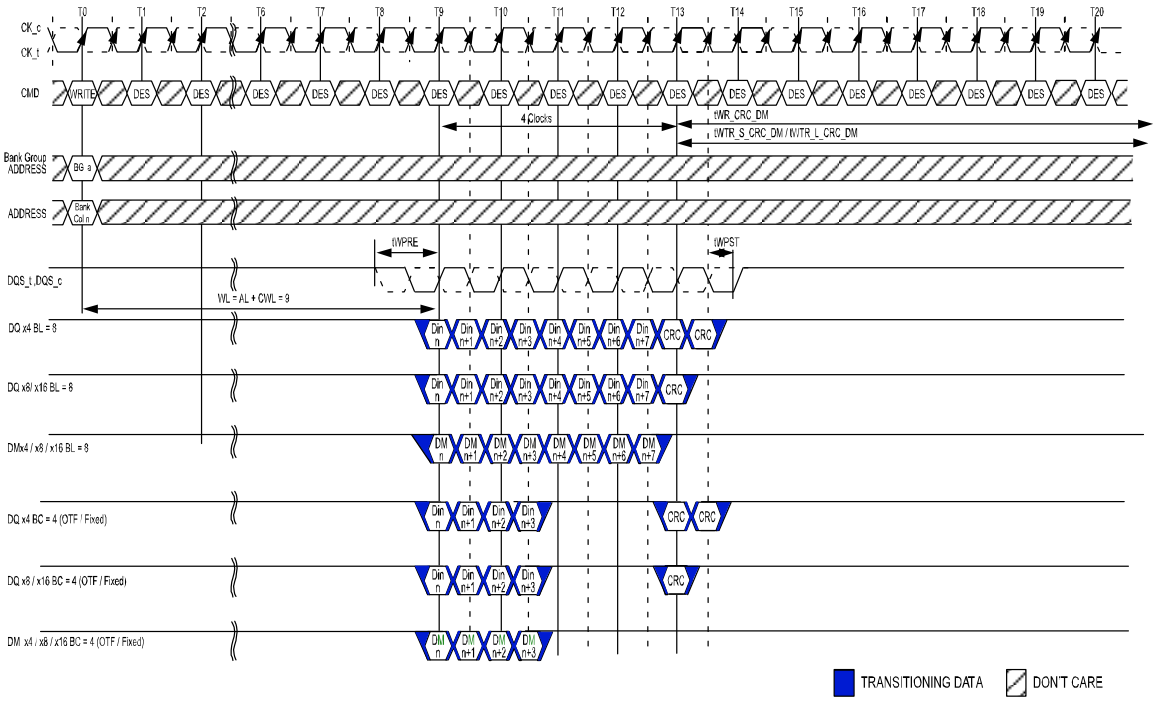
NOTE 6 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write $\overline{DBI}$ = Disable, Write CRC = Enable.

NOTE 7 tCCD_S/L = 6 isn't allowed in 2tCK preamble mode.

NOTE 8 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T21.

NOTE 9 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode

WRITE (BL8/BC4)OTF/Fixed with 1tCK Preamble and Write CRC and DM in Same or Different Bank Group



NOTE 1 BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK

NOTE 2 DIN n = data-in to column n.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 BL8 setting activated by either MR0 A [1:0] = 00 or MR0 A [1:0] = 01 and A12 = 1 during WRITE command at T0.

NOTE 5 BC4 setting activated by either MR0 A [1:0] = 10 or MR0 A [1:0] = 01 and A12 = 0 during READ command at T0.

NOTE 6 CA Parity = Disable, $\overline{CS}$ to CA Latency = Disable, Write $\overline{DBI}$ = Disable, Write CRC = Enable, DM = Enable.

NOTE 7 The write recovery time (tWR_CRC_ DM) and write timing parameter (tWR_S_CRC_ DM/tWR_L_CRC_ DM) are referenced from the first rising clock edge after the last write data shown at T13.

Read and Write Command Interval

Minimum Read and Write Command Timings

Bank Group	Access type	Timing Parameter	note
same	Minimum Read to Write	CL - CWL + RBL / 2 + 1 tCK + tWPRE	1, 2
	Minimum Read after Write	CWL + WBL / 2 + tWTR_L	1, 3
different	Minimum Read to Write	CL - CWL + RBL / 2 + 1 tCK + tWPRE	1, 2
	Minimum Read after Write	CWL + WBL / 2 + tWTR_S	1, 3

NOTE 1 These timings require extended calibrations times tZQinit and tZQCS.

NOTE 2 RBL : Read burst length associated with Read command

RBL = 8 for fixed 8 and on-the-fly mode 8

RBL = 4 for fixed BC4 and on-the-fly mode BC4

NOTE 3 WBL : Write burst length associated with Write command

WBL = 8 for fixed 8 and on-the-fly mode 8 or BC4

WBL = 4 for fixed BC4 only

Write Timing Violations

Motivation

Generally, if Write timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure that the DRAM works properly. However, it is desirable, for certain violations as specified below, the DRAM is guaranteed to not “hang up,” and that errors are limited to that particular operation.

For the following, it will be assumed that there are no timing violations with regards to the Write command itself (including ODT, etc.) and that it does satisfy all timing requirements not mentioned below.

Data Setup and Hold Offset Violations

Should the data to strobe timing requirements (tDQS_off, tDQH_off, tDQS_dd_off, tDQH_dd_off) be violated, for any of the strobe edges associated with a write burst, then wrong data might be written to the memory locations addressed with this WRITE command.

In the example (WRITE Burst Operation WL = 9 (AL = 0, CWL = 9, BL8)), the relevant strobe edges for write burst A are associated with the clock edges: T9, T9.5, T10, T10.5, T11, T11.5, T12, T12.5.

Subsequent reads from that location might results in unpredictable read data, however the DRAM will work properly otherwise.

Strobe and Strobe to Clock Timing Violations

Should the strobe timing requirements (tDQSH, tDQSL, tWPRE, tWPST) or the strobe to clock timing requirements (tDSS, tDSH, tDQSS) be violated for any of the strobe edges associated with a Write burst, then wrong data might be written to the memory location addressed with the offending WRITE command. Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise with the following constraints:

(1) Both Write CRC and data burst OTF are disabled; timing specifications other than tDQSH, tDQSL, tWPRE, tWPST, tDSS, tDSH, tDQSS are not violated.

(2) The offending write strobe (and preamble) arrive no earlier or later than six DQS transition edges from the Write-Latency position.

(3) A Read command following an offending Write command from any open bank is allowed.

(4) One or more subsequent WR or a subsequent WRA {to same bank as offending WR} may be issued tCCD_L later but incorrect data could be written; subsequent WR and WRA can be either offending or non-offending Writes. Reads from these Writes may provide incorrect data.

(5) One or more subsequent WR or a subsequent WRA {to a different bank group} may be issued tCCD_S later but incorrect data could be written; subsequent WR and WRA can be either offending or non-offending Writes. Reads from these Writes may provide incorrect data.

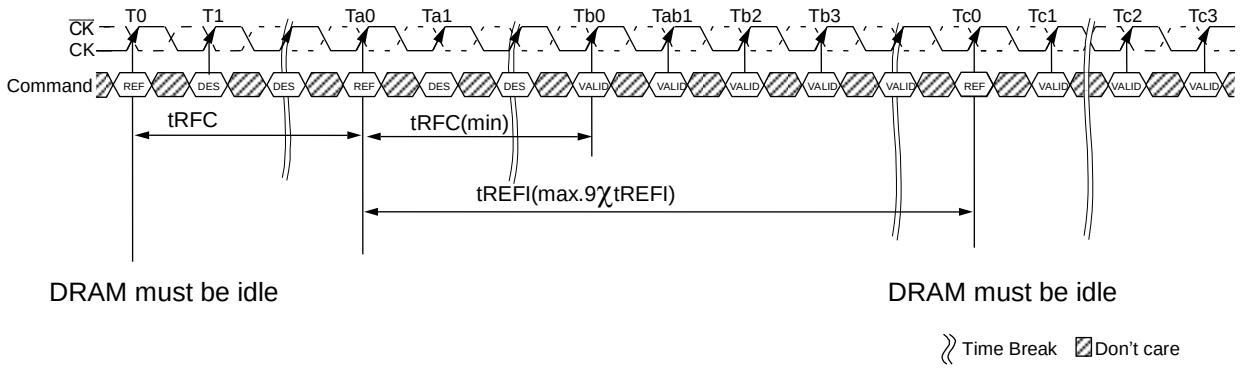
(6) Once one or more precharge commands (PRE or PREA) are issued to DDR4 after offending WRITE command and all banks become precharged state (idle state), a subsequent, non-offending WR or WRA to any open bank shall be able to write correct data.

REFRESH Command

The REFRESH command (REF) is used during normal operation of the device. This command is not persistent, so it must be issued each time a refresh is required. The device requires REFRESH cycles at an average periodic interval of tREFI. When $\overline{CS}$, $\overline{RAS}$/A16 and $\overline{CAS}$/A15 are held LOW and $\overline{WE}$/A14 and $\overline{ACT}$ are held HIGH at the rising edge of the clock, the chip enters a REFRESH cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time tRP (MIN) before the REFRESH command can be applied. The refresh addressing is generated by the internal DRAM refresh controller. This makes the address bits “Don’t Care” during a REFRESH command. An internal address counter supplies the addresses during the REFRESH cycle. No control of the external address bus is required once this cycle has started. When the REFRESH cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the REFRESH command and the next valid command, except DES, must be greater than or equal to the minimum REFRESH cycle time tRFC (MIN) as shown in Refresh Command Timing (Example of 1x Refresh mode). The tRFC timing parameter depends on memory density.

In general, a REFRESH command needs to be issued to the device regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided for postponing and pulling in the refresh command. A maximum of 8 Refresh commands can be postponed when DRAM is in 1X refresh mode and for 2X/4X refresh mode, 16/32 Refresh commands can be postponed respectively during operation of the DDR4 SDRAM, meaning that at no point in time more than a total of 8,16,32 Refresh commands are allowed to be postponed for 1X,2X,4X Refresh mode respectively. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to 9 × tREFI (see Refresh Command Timing (Example of 1x Refresh mode)). In 2X and 4X Refresh mode, it’s limited to 17 x tREFI2 and 33 x tREFI4. A maximum of 8 additional Refresh commands can be issued in advance (“pulled in”) in 1X refresh mode and for 2X/4X refresh mode, 16/32 Refresh commands can be pulled in respectively, with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8/16/32, depending on Refresh mode, Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to 9 × tREFI, 17 x tRFEI2 and 33 x tREFI4 respectively. At any given time, a maximum of 16 REF/32REF 2/64REF 4 commands can be issued within 2 x tREFI/ 4 x tREFI2/ 8 x tREFI4

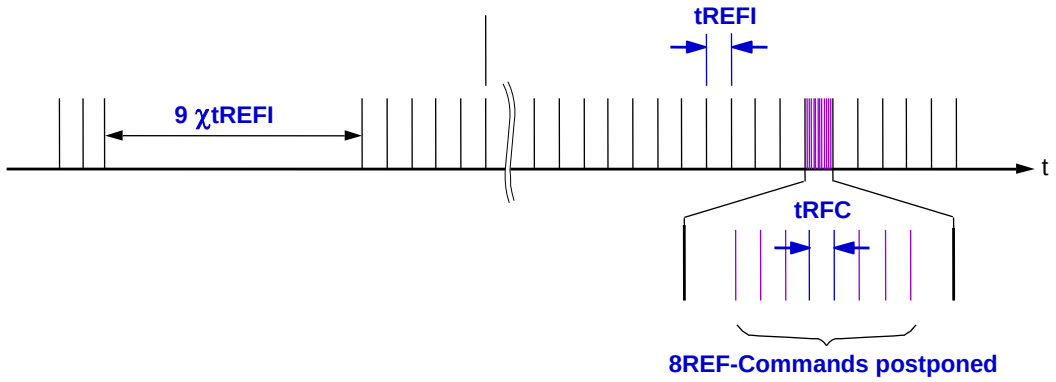
Refresh Command Timing (Example of 1x Refresh mode)



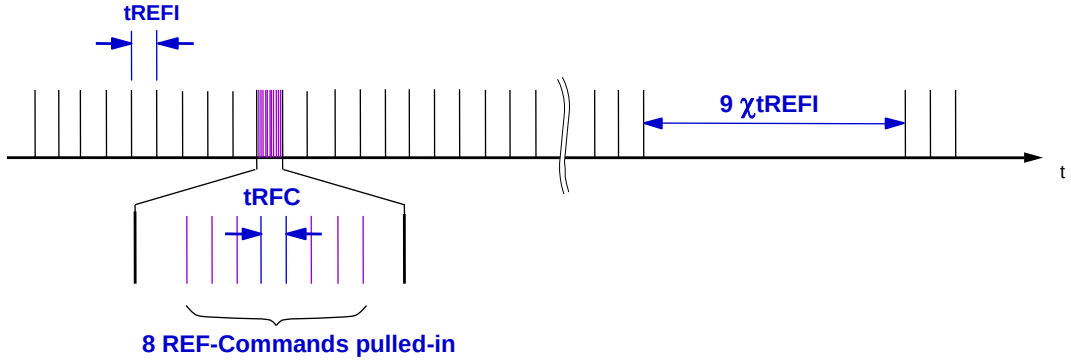
NOTE 1 Only DES commands allowed after REFRESH command registered until tRFC (MIN) expires.

NOTE 2 Time interval between two REFRESH commands may be extended to a maximum of 9 x tREFI.

Postponing REFRESH Commands (Example of 1X Refresh mode)



Pulling In REFRESH Commands (Example of 1X Refresh mode)



Self Refresh Operation

The SELF REFRESH command can be used to retain data in the DDR4 SDRAM, even if the rest of the system is powered down. When in self refresh mode, the device retains data without external clocking. The device has a built-in timer to accommodate SELF REFRESH operation. The Self-Refresh-Entry(SRE) command is defined by having $\overline{CS}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, and CKE held LOW with $\overline{WE}$/A14 and $\overline{ACT}$ HIGH at the rising edge of the clock.

Before issuing the Self-Refresh-Entry command, the device must be idle with all banks in the precharge state and tRP satisfied. Idle state is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is HIGH, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.). Deselect command must also be registered at the next positive clock edge. Once the Self-Refresh Entry command is registered, CKE must be held low to keep the device in Self-Refresh mode. DRAM automatically disables ODT termination and set Hi-Z as termination state regardless of ODT pin and RTT_PARK set when it enters in Self-Refresh mode. Upon exiting Self-Refresh, DRAM automatically enables ODT termination and set RTT_PARK asynchronously during tXSDLL when RTT_PARK is enabled. During normal operation (DLL on) the DLL is automatically disabled upon entering Self-Refresh and is automatically enabled (including a DLL-Reset) upon exiting Self-Refresh.

When the device has entered self refresh mode, all of the external control signals, except CKE and $\overline{RESET}$, are “Don’t Care.”. For proper SELF REFRESH operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VPP, and VREFCA) must be at valid levels.

If DRAM internal VrefDQ circuitry is turned off in self refresh, when DRAM exits from self refresh state, it ensures that VrefDQ generator circuitry is powered up and stable within tXS period. First Write operation or first Write Leveling activity may not occur earlier than tXS after exit from Self Refresh. The DRAM initiates a minimum of one Refresh command internally within tCKE period once it enters Self-Refresh mode.

The clock is internally disabled during a SELF REFRESH operation to save power. The minimum time that the device must remain in self refresh mode is tCKESR. The user may change the external clock frequency or halt the external clock tCKSRE after self refresh entry is registered; however, the clock must be restarted and stable tCKSRX before the device can exit Self-Refresh operation.

The procedure for exiting self refresh requires a sequence of events. First, the clock must be stable prior to CKE going back HIGH. Once a SELF REFRESH EXIT command (SRX, combination of CKE going HIGH and DESELECT on the command bus) is registered, the following timing delay must be satisfied:

(1) Commands that do not require locked DLL:

- tXS - ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8.
- tXSFast - ZQCL, ZQCS, MRS commands. For an MRS command, only DRAM CL and WR/RTP register and DLL Reset in MR0, RTT_NOM register in MR1, CWL and RTT_WR register in MR2 and geardown mode in MR3, Write and Read Preamble register in MR4, RTT_PARK register in MR5, tCCD_L/tDLLK and VrefDQ Training Value in MR6 are allowed to be accessed provided DRAM is not in per DRAM addressability mode. Access to other DRAM mode registers must satisfy tXS timing.

Note that synchronous ODT for write commands (WR, WRS4, WRS8, WRA, WRAS4 and WRAS8) and dynamic ODT controlled by write command require locked DLL.

(2) Commands that require locked DLL:

- tXSDLL - RD, RDS4, RDS8, RDA, RDAS4, RDAS8.

Depending on the system environment and the amount of time spent in self refresh, ZQ CALIBRATION commands may be required to compensate for the voltage and temperature drift described in the ZQ Calibration Commands section. To issue ZQ CALIBRATION commands, applicable timing requirements must be satisfied.

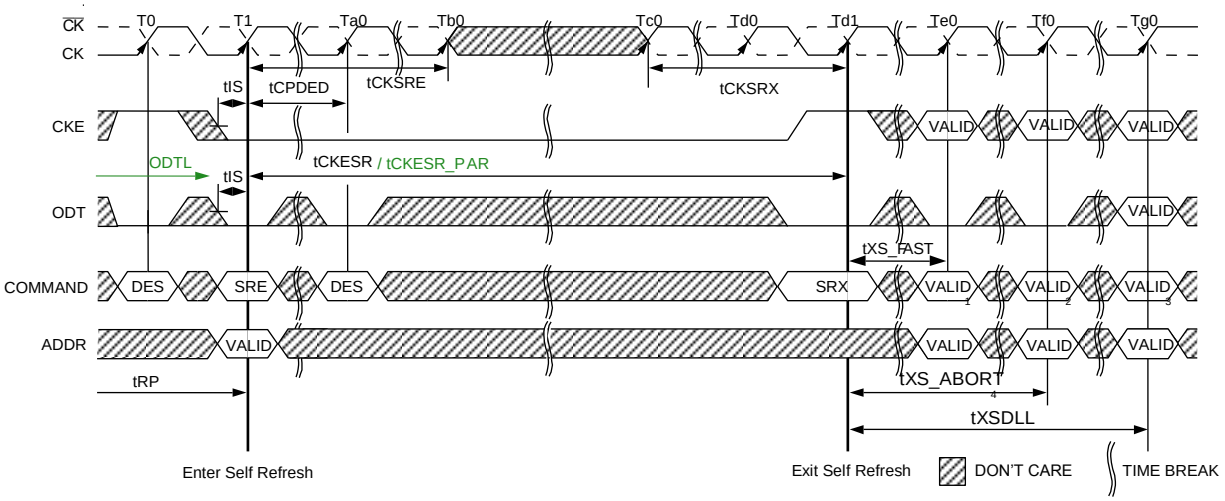
CKE must remain HIGH for the entire self refresh exit period tXSDLL for proper operation except for self refresh re-entry. Upon exit from self refresh, the device can be put back into self refresh mode or power-down mode after waiting at least tXS period and issuing one REFRESH command (refresh period of tRFC). The DESELECT command must be registered on each positive clock edge during the self refresh exit interval tXS. Low level of ODT pin must be registered on each positive clock edge during tXSDLL when normal mode (DLL-on) is set. Under DLL-off mode, asynchronous ODT function might be allowed. The use of Self-Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self-Refresh mode. Upon exit from Self-Refresh, the DDR4 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode.

The exit timing from self-refresh exit to first valid command not requiring a locked DLL is tXS.

The value of tXS is (tRFC+10ns). This delay is to allow for any refreshes started by the DRAM to complete. tRFC continues to grow with higher density devices so tXS will grow as well.

A Bit A9 in MR4 is defined to enable the self refresh abort mode. If the bit is disabled, then the controller uses tXS timings. If the bit is enabled, then the DRAM aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command not requiring a locked DLL after a delay of tXS_abort. Upon exit from Self-Refresh, the DDR4 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode. This requirement remains the same irrespective of the setting of the MRS bit for self refresh abort.

Self Refresh Entry/Exit Timing



NOTE 1 Only MRS (limited to those described in the Self-Refresh Operation section). ZQCS or ZQCL command allowed.

NOTE 2 Valid commands not requiring a locked DLL

NOTE 3 Valid commands requiring a locked DLL

NOTE 4 Only DES is allowed during tXS_ABORT

Low-Power Auto Self Refresh Mode (LPASR)

An auto self refresh mode is provided for application ease. Auto self refresh mode is enabled by setting MR2[6] = 1 and MR2[7] = 1. The device will manage self refresh entry over the supported temperature range of the DRAM. In this mode, the device will change its self refresh rate as the DRAM operating temperature changes, going lower at low temperatures and higher at high temperatures.

Manual Self Refresh Mode

If auto self refresh mode is not enabled, the low-power auto self refresh mode register must be manually programmed to one of the three self refresh operating modes. This mode provides the flexibility to select a fixed self refresh operating mode at the entry of the self refresh, according to the system memory temperature conditions. The user is responsible to maintain the required memory temperature condition for the mode selected during the self refresh operation. The user may change the selected mode after exiting self refresh and before entering the next self refresh. If the temperature condition is exceeded for the mode selected, there is a risk to data retention resulting in loss of data.

MR2 definitions for Low Power Auto Self-Refresh mode- Function table

MR2 A[7]	MR2 A[6]	Low-Power Auto Self Refresh Mode	Allowed Operating temp. range for Self Refresh Mode	Self Refresh Operation
0	0	Manual Mode-Normal	(0°C – 85°C)	Fixed normal self refresh rate maintains data retention at the normal operating temperature. User is required to ensure that 85°C DRAM $T_{CASEMAX}$ is not exceeded to avoid any risk of data loss. ForI/T-grade,temp. range is -40 to 85°C
0	1	Manual Mode-Extended Temp	(0°C – 95°C)	Fixed high self refresh rate optimizes data retention to support the extended temperature range. ForI/T-grade,temp. range is -40 to 95°C
1	0	Manual Mode-Reduced Temp	(0°C – 45°C)	Variable or fixed self refresh rate or any other DRAM power consumption reduction control for the reduced temperature range. User is required to ensure 45°C DRAM TCASEMAX is not exceeded to avoid any risk of data loss. ForI/T-grade,temp. range is -40 to 45°C
1	1	Auto Self Refresh	All of the above	Auto self refresh mode enabled. Self refresh power consumption and data retention are optimized for any given operating temperature condition.

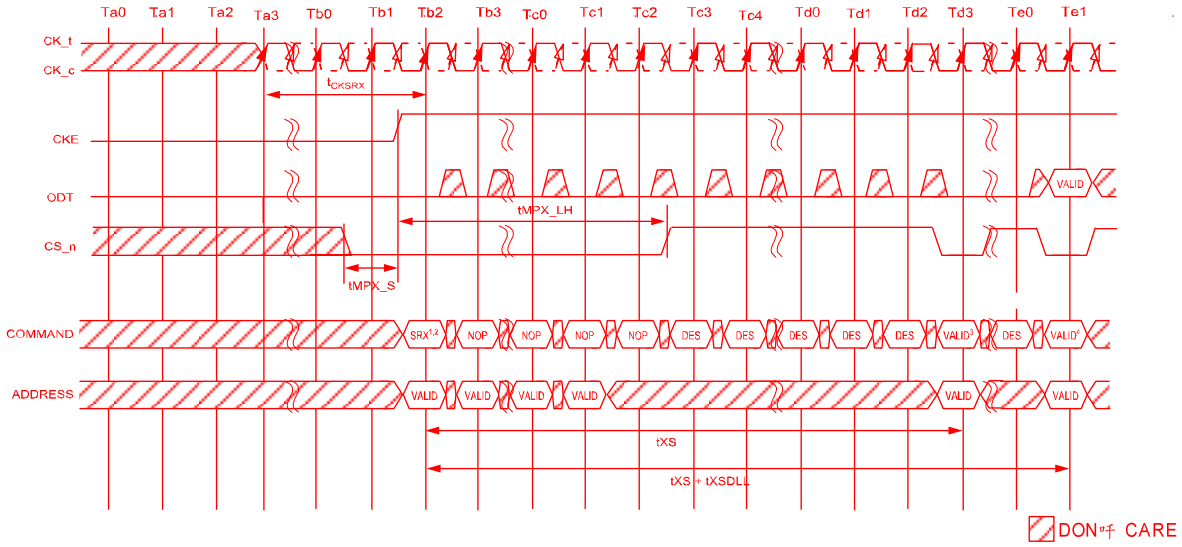
Self Refresh Exit with No Operation command

Self Refresh Exit with No Operation command (NOP) allows for a common command/address bus between active DRAM and DRAM in Max Power Saving Mode. Self Refresh Mode may exit with No Operation commands (NOP) provided:

(1) The DRAM entered Self Refresh Mode with CA Parity and CAL disabled.

(2) tMPX_S and tMPX_LH are satisfied.

(3) NOP commands are only issued during tMPX_LH window. No other command is allowed during tMPX_LH window after SRX command is issued.



NOTE 1 $\overline{CS}$ = L, $\overline{ACT}$ = H, $\overline{RAS}$/A16 = H, $\overline{CAS}$/A15 = H, $\overline{WE}$/A14 = H at Tb2 (No Operation command)

NOTE 2 SRX at Tb2 is only allowed when DRAM shared Command/Address bus is under exiting Max Power Saving Mode.

NOTE 3 Valid commands not requiring a locked DLL

NOTE 4 Valid commands requiring a locked DLL

NOTE 5 tXS_FAST and tXS_ABORT are not allowed this case.

NOTE 6 Duration of $\overline{CS}$ Low around CKE rising edge must satisfy tMPX_S and tMPX_LH as defined by Max Power Saving Mode AC parameters.

Power-Down Mode

Power-Down Entry and Exit

Power-down is synchronously entered when CKE is registered LOW (along with a DESELECT command). CKE is not allowed to go LOW when the following operations are in progress: MODE REGISTER SET command, MPR operations, ZQCAL operations, DLL locking, or READ/WRITE operations. CKE is allowed to go LOW while any other operations, such as ROW ACTIVATION, PRECHARGE or auto precharge, or REFRESH, are in progress, but the power-down IDD spec will not be applied until those operations are complete. Timing diagrams below illustrate entry and exit of power-down. The DLL should be in a locked state when power-down is entered for fastest powerdown exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper read operation and synchronous ODT operation. DRAM design provides all AC and DC timing and voltage specification as well as proper DLL operation with any CKE intensive operations as long as the DRAM controller complies with DRAM specifications.

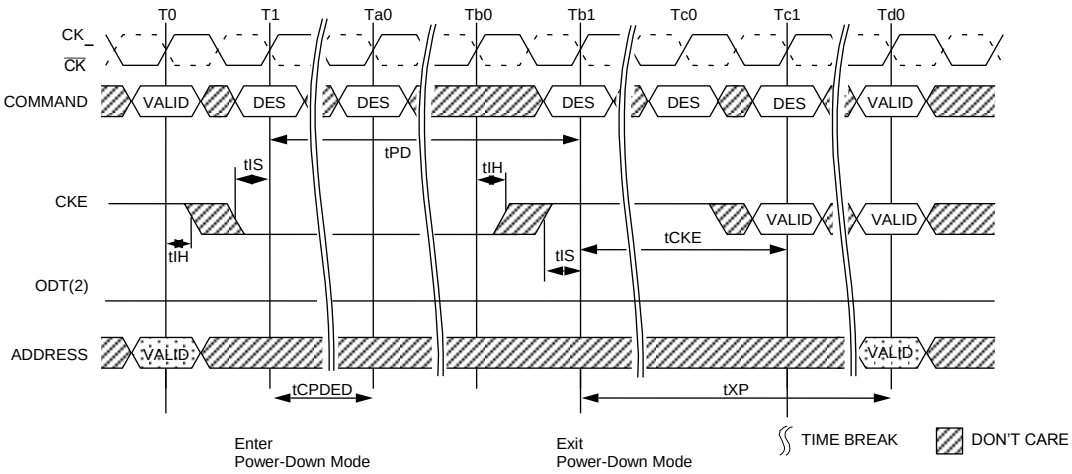
During power-down, if all banks are closed after any in-progress commands are completed, the device will be in precharge power-down mode; if any bank is open after in progress commands are completed, the device will be in active power-down mode. Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$, CKE and $\overline{RESET}$. In power-down mode, DRAM ODT input buffer deactivation is based on MRx bit Y. If it is configured to 0b, the ODT input buffer remains on and ODT input signal must be at valid logic level. If it is configured to 1b, ODT input buffer is deactivated and DRAM ODT input signal may be floating and DRAM does not provide RTT_NOM termination. Note that the device continues to provide RTT_PARK termination if it is enabled in the mode register MRa bit B. To protect internal delay on the CKE line to block the input signals, multiple DES commands are needed during the CKE switch off and on cycle(s); this timing period is defined as tCPDED. CKE_low will result in deactivation of command and address receivers after tCPDED has expired.

Power-Down Entry Definitions

Status of DRAM	DLL	PD Exit	Relevant Parameters
Active (A bank or more Open)	On	Fast	tXP to any valid command
Precharged (All banks Precharged)	On	Fast	tXP to any valid command.

The DLL is kept enabled during precharge power-down or active power-down. In power-down mode, CKE is LOW, $\overline{RESET}$ is HIGH, and a stable clock signal must be maintained at the inputs of the device. ODT should be in a valid state, but all other input signals are "Don't Care." (If $\overline{RESET}$ goes LOW during power-down, the device will be out of power-down mode and in the reset state.) CKE LOW must be maintained until tCKE has been satisfied. Power-down duration is limited by 9 x tREFI. The power-down state is synchronously exited when CKE is registered HIGH (along with DES command). CKE HIGH must be maintained until tCKE has been satisfied. The ODT input signal must be at a valid level when the device exits from power-down mode, independent of MRx bit Y if RTT_NOM is enabled in the mode register. If RTT_NOM is disabled, then the ODT input signal may remain floating. A valid, executable command can be applied with power-down exit latency, tXP and/or tXPDLL after CKE goes HIGH. Power-down exit latency is defined in the AC Specifications table.

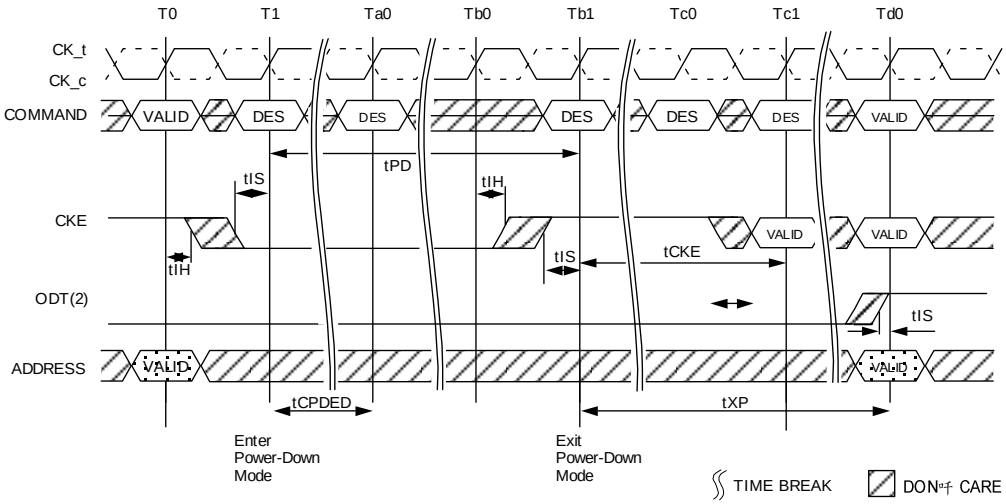
Active Power-Down Entry and Exit (MR5 bit A5 =0)



NOTE 1 Valid commands at T0 are ACT, DES, or PRE with one bank remaining open after completion of the PRECHARGE command.

NOTE 2 ODT pin driven to a valid state; MR5 [5] = 0 (normal setting).

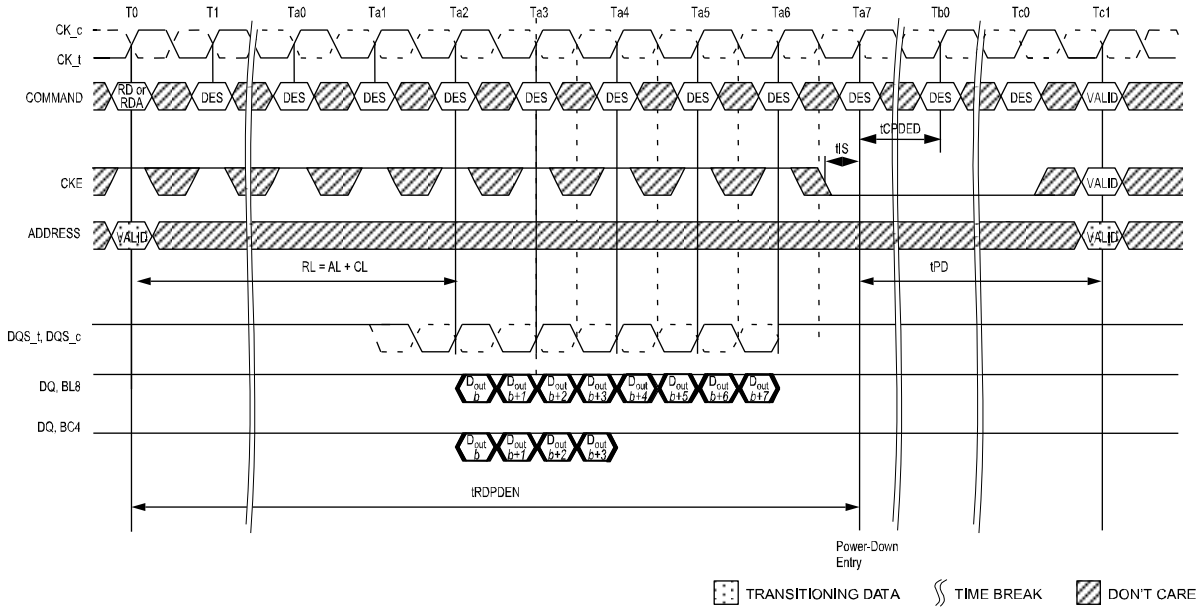
Active Power-Down Entry and Exit (MR5 bit A5 =1)



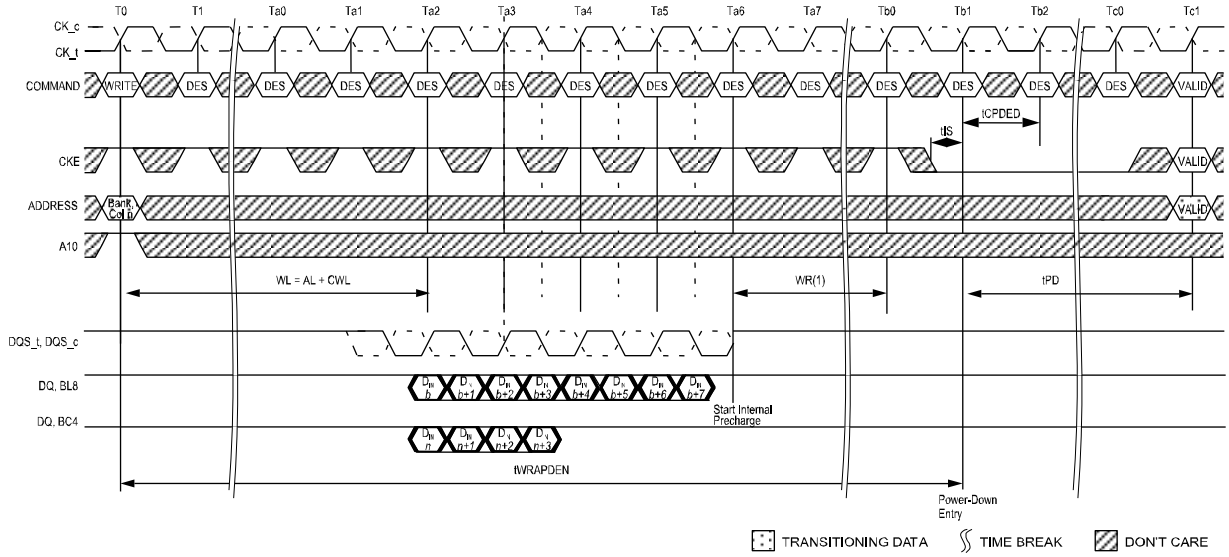
NOTE 1 Valid commands at T0 are ACT, DES, or PRE with one bank remaining open after completion of the PRECHARGE command.

NOTE 2 ODT pin driven to a valid state; MR5 [5] = 1.

Power-Down Entry After Read and Read with Auto Precharge

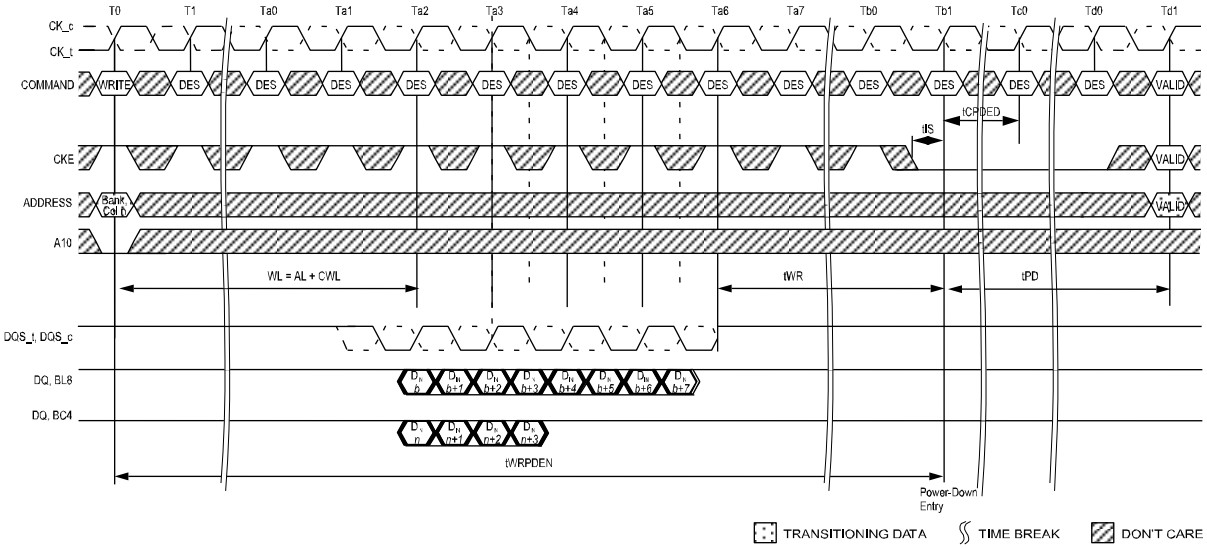


Power-Down Entry After Write with Auto Precharge

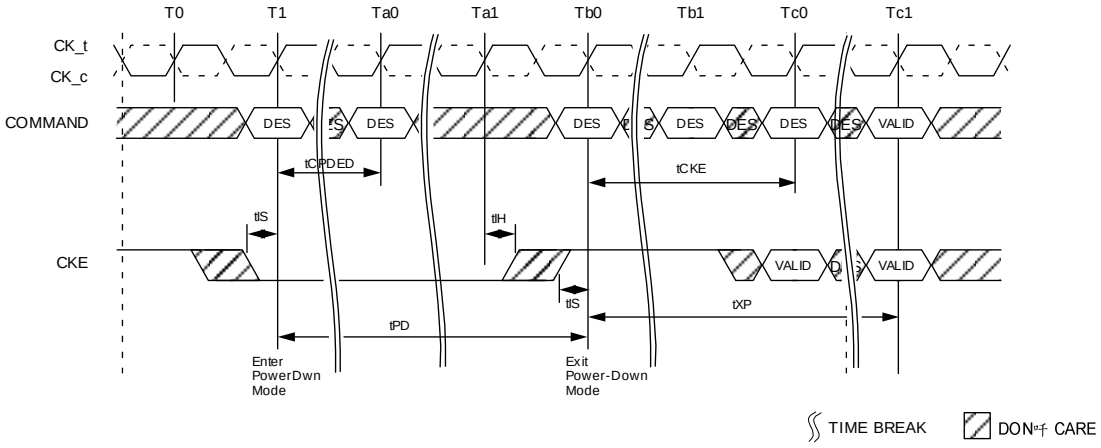


NOTE 1 tWR is programmed through MR0.

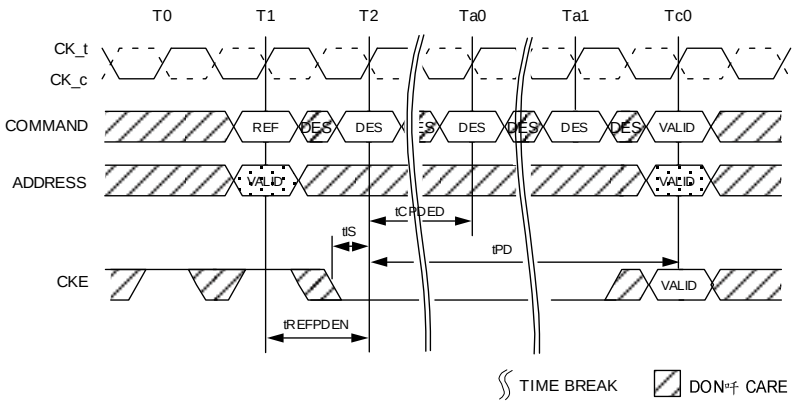
Power-Down Entry After Write



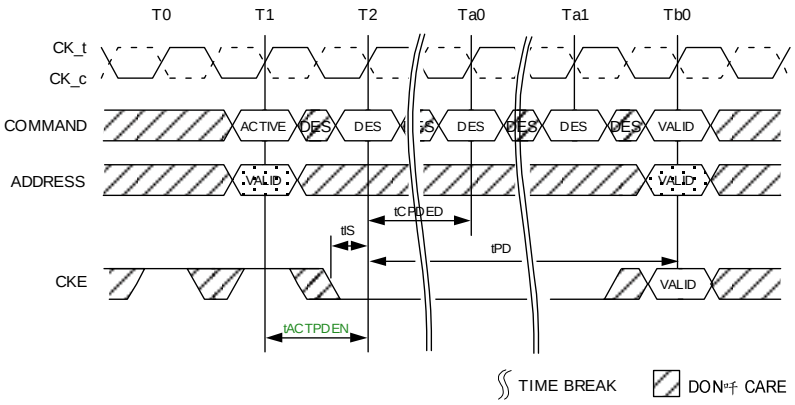
Precharge Power-Down Entry and Exit



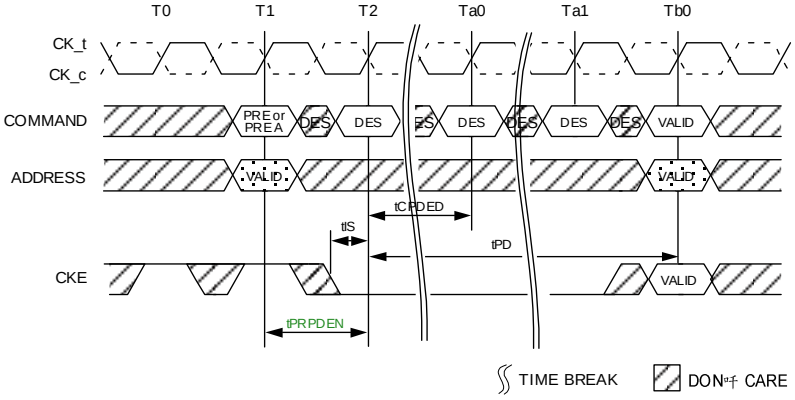
Refresh Command to Power-Down Entry



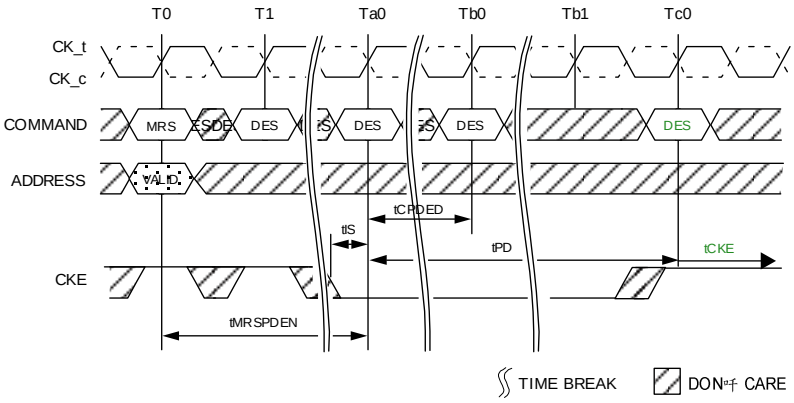
Active Command to Power-Down Entry



Precharge/Precharge All Command to Power-Down Entry



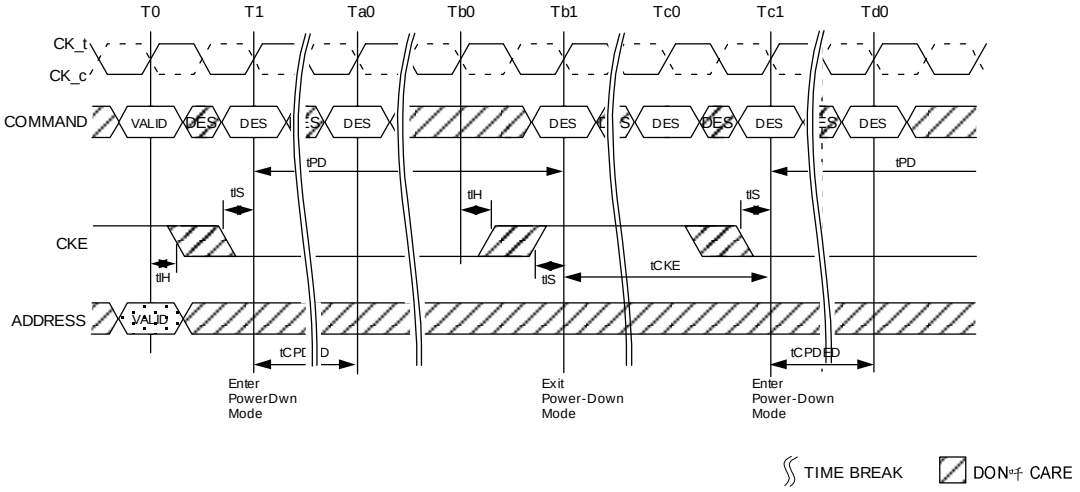
MRS Command to Power-Down Entry



Power-Down Clarifications

When CKE is registered LOW for power-down entry, tPD (MIN) must be satisfied before CKE can be registered HIGH for power-down exit. The minimum value of parameter tPD (MIN) is equal to the minimum value of parameter tCKE (MIN) as shown in the Timing Parameters by Speed Bin table. A detailed example of Case 1 is shown below.

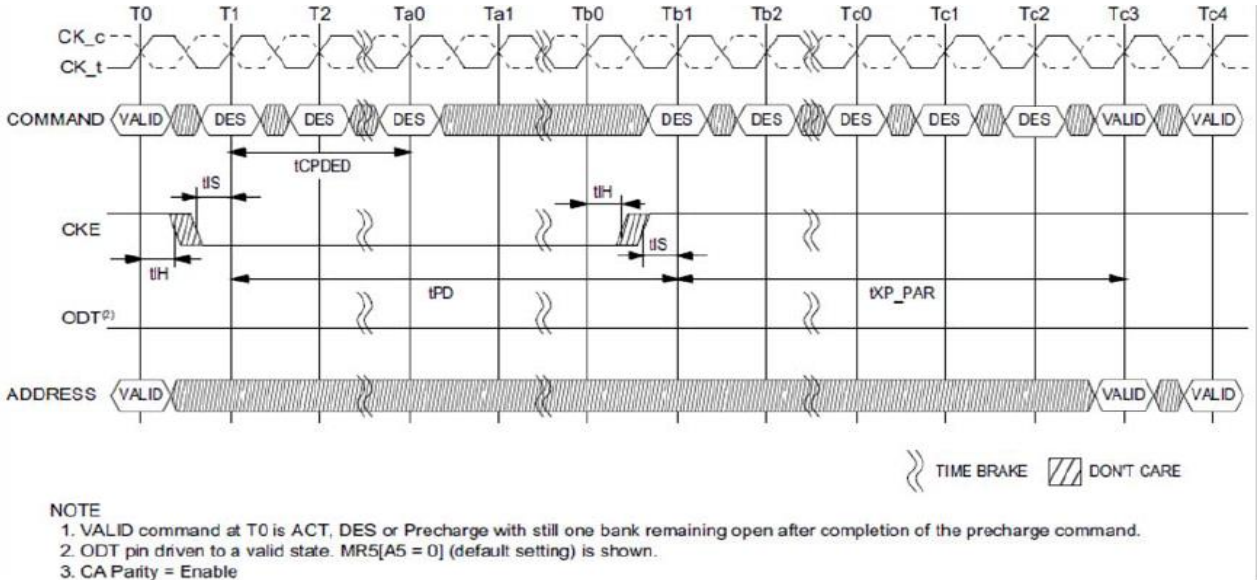
Power-Down Entry/Exit Clarification



Power Down Entry and Exit timing during Command/Address Parity Mode is Enable

Power Down entry and exit timing during Command/Address Parity mode is Enable are shown below.

Power Down Entry and Exit Timing with C/A Parity



NOTE
1. VALID command at T0 is ACT, DES or Precharge with still one bank remaining open after completion of the precharge command.
2. ODT pin driven to a valid state. MR5[A5 = 0] (default setting) is shown.
3. CA Parity = Enable

AC Timing Table

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL when CA Parity is enabled	tXP_PAR	max (4nCK,6ns) + PL	-	max (4nCK,6ns) + PL	-	max (4nCK,6ns) + PL	-	max (4nCK,6ns) + PL	-	

Maximum Power-Saving Mode (MPSM)

Maximum power saving mode

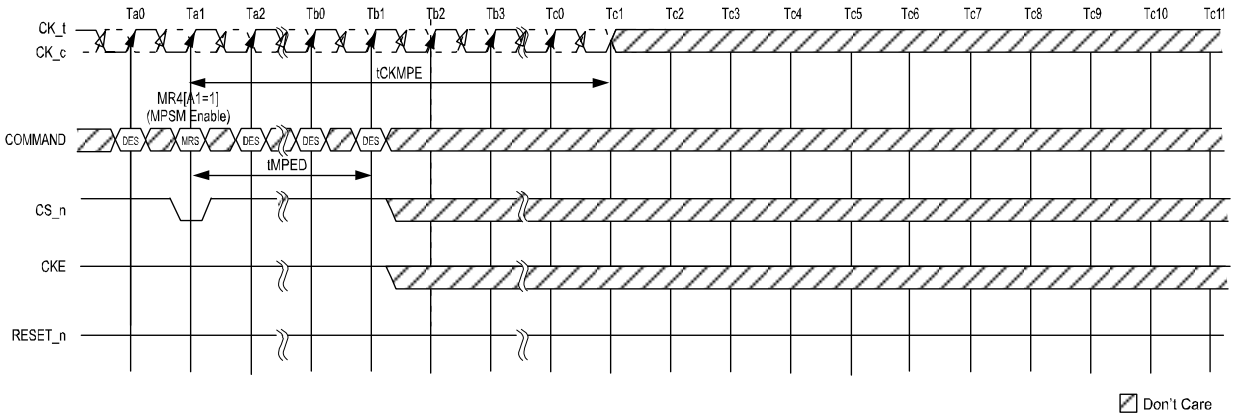
This mode provides lowest power consuming mode which could be similar to the Self-Refresh status with no internal refresh activity. When DDR4 SDRAM is in the maximum power saving mode, it does not need to guarantee data retention nor respond to any external command (except maximum power saving mode exit and asserting $\overline{\text{RESET}}$ signal LOW to minimize the power consumption.

Maximum Power-Saving Mode Entry

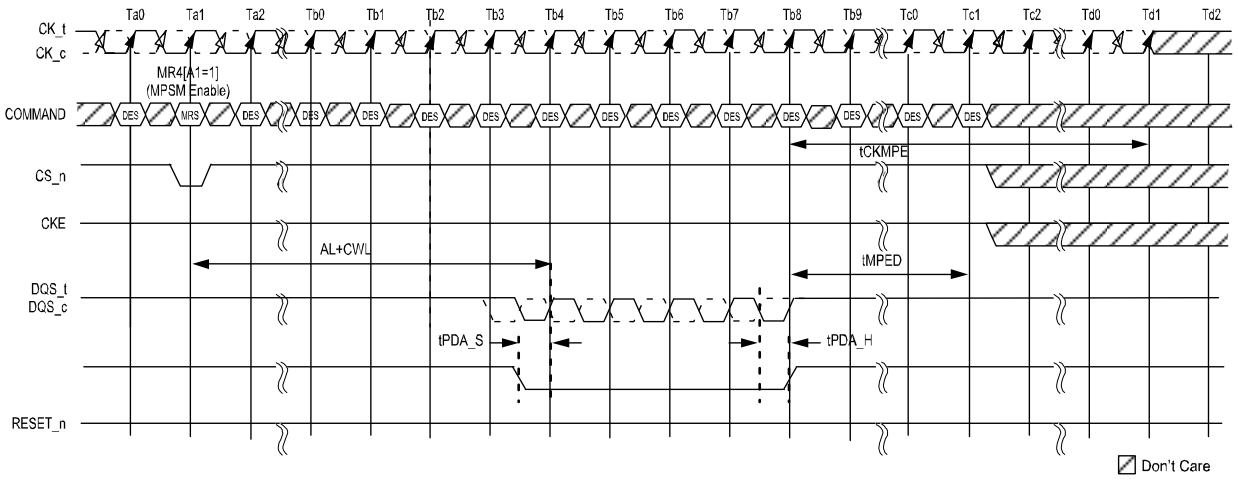
Max power saving mode is entered through an MRS command. For devices with shared control/address signals, a single DRAM device can be entered into the max power saving mode using the per DRAM Addressability MRS command. Note that large $\overline{\text{CS}}$ hold time to CKE upon the mode exit may cause DRAM malfunction, thus it is required that the CA parity, CAL and Gear Down modes are disabled prior to the max power saving mode entry MRS command.

When entering Maximum Power Saving mode, only DES commands are allowed until tMPED is satisfied. After tMPED period from the mode entry command, DRAM is not responsive to any input signals except $\overline{\text{CS}}$, CKE and $\overline{\text{RESET}}$ signals, and all other input signals can be High-Z. CLK should be valid for tCKMPE period and then can be High-Z.

Maximum Power Saving Mode Entry



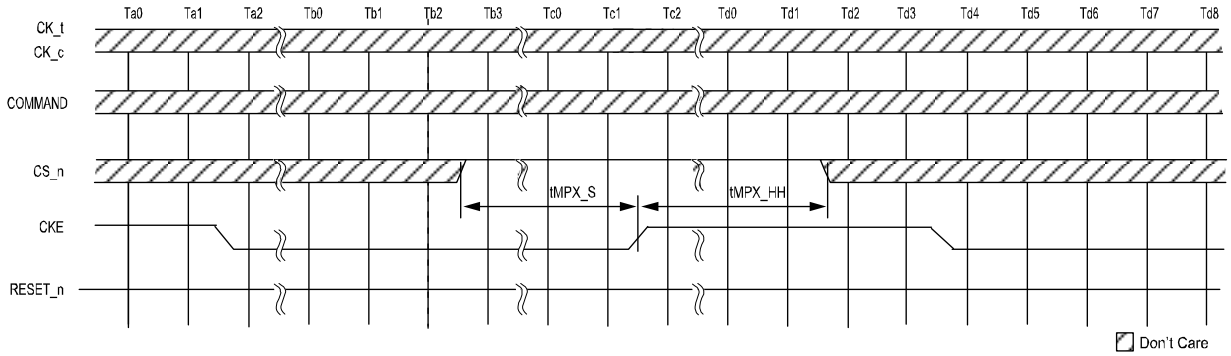
Maximum Power-Saving Mode Entry with PDA



CKE Transition during Maximum Power-Saving Mode

CKE toggle is allowed when DRAM is in the maximum power saving mode. To prevent the device from exiting the mode, $\overline{CS}$ should be issued 'High' at CKE 'L' to 'H' edge with appropriate setup tMPX_S and hold tMPX_HH timings.

CKE Transition Limitation to hold Maximum Power Saving Mode

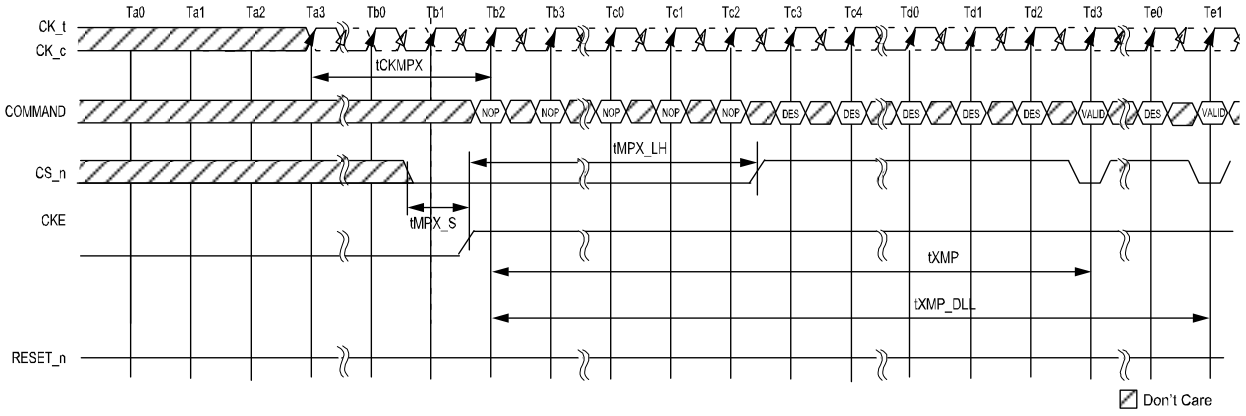


Maximum Power-Saving Mode Exit

DRAM monitors $\overline{CS}$ signal level and when it detects CKE 'L' to 'H' transition, and either exits from the power saving mode or stay in the mode depending on the $\overline{CS}$ signal level at the CKE transition. Because CK receivers are shut down during this mode, $\overline{CS}$ = 'L' is captured by rising edge of the CKE signal. If $\overline{CS}$ signal level is detected 'L', then the DRAM initiates internal exit procedure from the power saving mode. CK must be restarted and stable tCKMPX period before the device can exit the maximum power saving mode. During the exit time tXMP, any valid commands except DES command is not allowed to DDR4 SDRAM and also tXMP_DLL, any valid commands requiring a locked DLL is not allowed to DDR4 SDRAM.

When recovering from this mode, the DRAM clears the MRS bits of this mode. It means that the setting of MR4 A1 is move to '0' automatically.

Maximum Power-Saving Mode Exit



Timing parameter bin of Maximum Power Saving Mode

Description	symbol	DDR4-1600/1866/2133/2400/2666		Unit	Note
		Min	Max		
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-		
CS setup time to CKE	tMPX_S	tISmin + tIHmin	-		
$\overline{CS}$ High hold time to CKE rising edge	tMPX_HH	tXP(min)			
$\overline{CS}$ Low hold time to CKE rising edge	tMPX_LH	12	tXMP-10ns	ns	1

NOTE 1 tMPX_LH(max) is defined with respect to actual tXMP in system as opposed to tXMP(min).

Connectivity Test Mode (CT)

Introduction

The DDR4 memory device supports a connectivity test (CT) mode, which is designed to greatly speed up testing of electrical continuity of pin interconnection on the PC boards between the DDR4 memory devices and the memory controller on the SoC. Designed to work seamlessly with any boundary scan devices, the CT mode is required for all x16 width devices independent of density and optional for all x8 and x4 width devices with densities greater than or equal to 8Gb. Contrary to other conventional shift register based test mode, where test patterns are shifted in and out of the memory devices serially in each clock, DDR4's CT mode allows test patterns to be entered in parallel into the test input pins and the test results extracted in parallel from the test output pins of the DDR4 memory device at the same time, significantly enhancing the speed of the connectivity check. $\overline{\text{RESET}}$ is registered to High and VrefCA must be stable prior to entering CT mode. Once put in the CT mode, the DDR4 memory device effectively appears as an asynchronous device to the external controlling agent; after the input test pattern is applied, the connectivity check test results are available for extraction in parallel at the test output pins after a fixed propagation delay. During CT mode, any ODT is turned off.

A reset of the DDR4 memory device is required after exiting the CT mode.

Pin Mapping

Only digital pins can be tested via the CT mode. For the purposes of a connectivity check, all the pins used for digital logic in the DDR4 memory device are classified as one of the following 5 types:

Pin Classification of DDR4 Memory Device in Connectivity Test(CT) Mode

Types	CT Mode Pins		Pin Names during Normal Memory Operation
1	Test Enable		TEN
2	Chip Select		$\overline{\text{CS}}$
3	Test Input	A	BA[1:0], BG[1:0], A[9:0], A10/AP, A11, A12/$\overline{\text{BC}}$, A13, $\overline{\text{WE}}$/A14, $\overline{\text{CAS}}$/A15, $\overline{\text{RAS}}$/A16, CKE, $\overline{\text{ACT}}$, ODT, CK, $\overline{\text{CK}}$, PAR
		B	$\overline{\text{LDM}}$/LDBI, $\overline{\text{UDM}}$/UDBI, $\overline{\text{DM}}$/DBI
		C	$\overline{\text{ALERT}}$
4		D	$\overline{\text{RESET}}$
5	Test Output		DQ[15:0], DQSU, $\overline{\text{DQSU}}$, DQSL, $\overline{\text{DQSL}}$, DQS, $\overline{\text{DQS}}$

Signal Description

Symbol	Type	Function
TEN	Input	Connectivity Test Mode is active when TEN is HIGH and inactive when TEN is LOW. TEN must be LOW during normal operation TEN is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of VDD, i.e., 960mV for DC high and 240mV for DC low.

TEN Pin Weak Pull Down Strength Range

Symbol	Description	Min	Max	Unit
TEN	TEN pin should be internally pulled low to prevent DDR4 SDRAM from conducting Connectivity Test mode in case that TEN is not used.	0.05	10	uA

NOTE 1 The host controller should use good enough strength when activating Connectivity Test mode to avoid current fighting at TEN signal and inability of Connectivity Test mode.

Logic Equations

Min Term Equations

MTx is an internal signal to be used to generate the signal to drive the output signals.

x16 and x8 signals are internal signal indicating the density of the device.

MT0 = XOR (A1, A6, PAR)

MT1 = XOR (A8, $\overline{\text{ALERT}}$, A9)

MT2 = XOR (A2, A5, A13)

MT3 = XOR (A0 A7, A11)

MT4 = XOR ($\overline{\text{CK}}$, ODT, $\overline{\text{CAS}}$/A15)

MT5 = XOR (CKE, $\overline{\text{RAS}}$/A16, A10/AP)

MT6 = XOR ($\overline{\text{ACT}}$, A4, BA1)

MT7 = XOR (((x16 and $\overline{\text{UDM}}$ / $\overline{\text{UDBI}}$) or (!x16 and BG1)), ((x8 or x16) and $\overline{\text{LDM}}$ / $\overline{\text{LDBI}}$), CK))

MT8 = XOR ($\overline{\text{WE}}$ / A14, A12 / BC, BA0)

MT9 = XOR (BG0, A3, ($\overline{\text{RESET}}$ and TEN))

Output equations for x16 devices

DQ0 = MT0

DQ1 = MT1

DQ2 = MT2

DQ3 = MT3

DQ4 = MT4

DQ5 = MT5

DQ6 = MT6

DQ7 = MT7

DQ8 = !DQ0

DQ9 = !DQ1

DQ10 = !DQ2

DQ11 = !DQ3

DQ12 = !DQ4

DQ13 = !DQ5

DQ14 = !DQ6

DQ15 = !DQ7

DQSL = MT8

$\overline{\text{DQSL}}$ = MT9

DQSU = !DQSL

$\overline{\text{DQSU}}$ = !$\overline{\text{DQSL}}$

Output equations for x8 devices

DQ0 = MT0

DQ1 = MT1

DQ2 = MT2

DQ3 = MT3

DQ4 = MT4

DQ5 = MT5

DQ6 = MT6

DQ7 = MT7

DQS = MT8

$\overline{\text{DQS}}$ = MT9

Output equations for x4 devices

DQ0 = XOR (MT0, MT1)

DQ1 = XOR (MT2, MT3)

DQ2 = XOR (MT4, MT5

DQ3 = XOR (MT6, MT7)

DQS = MT8

$\overline{\text{DQS}}$ = MT9

Input level and Timing Requirement

During CT Mode, input levels are defined below.

1. TEN pin: CMOS rail-to-rail with DC high and low at 80% and 20% of VDD.
2. $\overline{CS}$: Pseudo differential signal referring to VrefCA
3. Test Input pin A: Pseudo differential signal referring to VrefCA
4. Test Input pin B: Pseudo differential signal referring to internal Vref 0.5*VDD
5. $\overline{RESET}$: CMOS DC high above 70 % VDD
6. $\overline{ALERT}$: Terminated to VDD. Swing level is TBD.

Prior to the assertion of the TEN pin, all voltage supplies must be valid and stable.

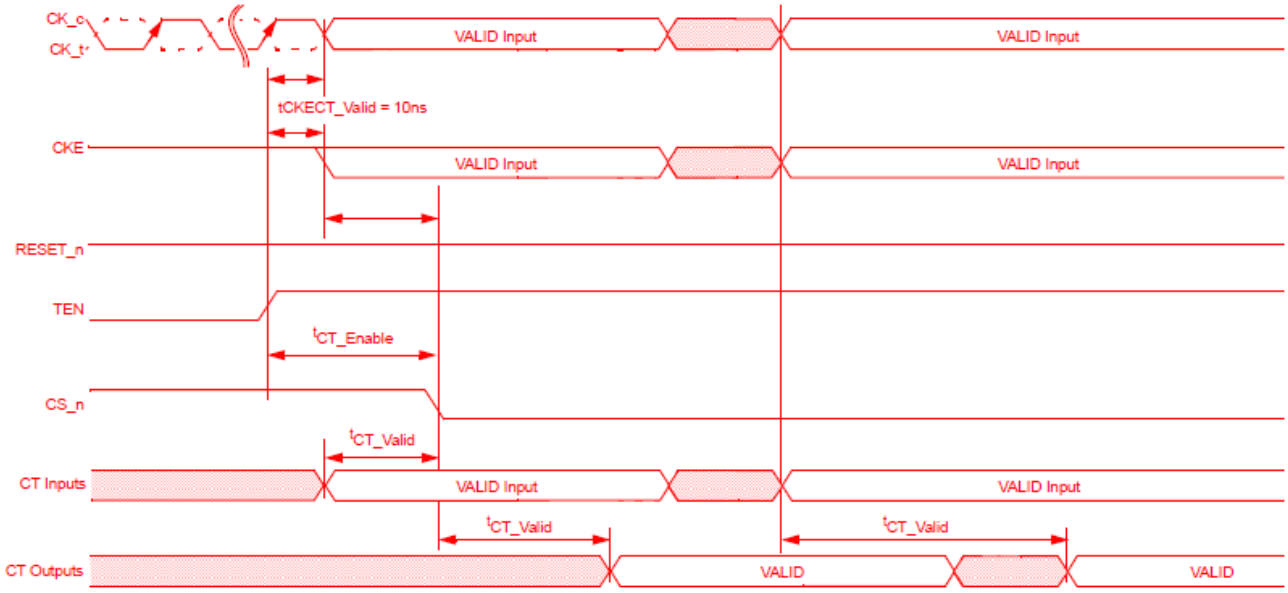
Upon the assertion of the TEN pin, the CK and $\overline{CK}$ signals will be ignored and the DDR4 memory device enter into the CT mode after tCT_Enable. In the CT mode, no refresh activities in the memory arrays, initiated either externally (i.e., auto-refresh) or internally (i.e., self-refresh), will be maintained.

The TEN pin may be asserted after the DRAM has completed power-on; once the DRAM is initialized and VREFDQ is calibrated, CT Mode may no longer be used.

The TEN pin may be de-asserted at any time in the CT mode. Upon exiting the CT mode, the states of the DDR4 memory device are unknown and the integrity of the original content of the memory array is not guaranteed and therefore the reset initialization sequence is required.

All output signals at the test output pins will be stable within tCT_valid after the test inputs have been applied to the test input pins with TEN input and input maintained High and Low respectively.

Timing Diagram for Connectivity Test(CT) Mode



AC parameters for Connectivity Test (CT) Mode

Symbol	Min	Max	Unit
tCT_IS	0	-	ns
tCT_Enable	200	-	ns
tCT_Valid	-	200	ns

Connectivity Test (CT) Mode Input Levels

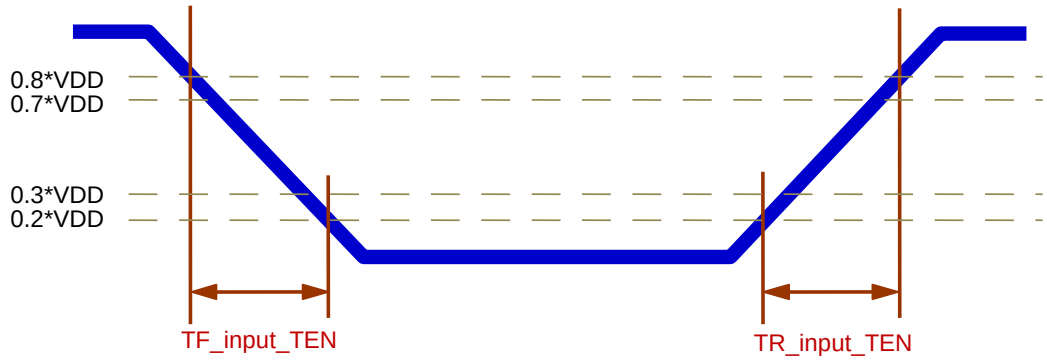
CMOS rail to rail Input Levels for TEN

Symbol	Parameter	Min	Max	Unit	NOTE
$VIH_{(AC)\_TEN}$	TEN AC Input High Voltage	0.8 x VDD	VDD	V	1
$VIH_{(DC)\_TEN}$	TEN DC Input High Voltage	0.7 x VDD	VDD	V	
$VIL_{(DC)\_TEN}$	TEN DC Input Low Voltage	VSS	0.3 x VDD	V	
$VIL_{(AC)\_TEN}$	TEN AC Input Low Voltage	VSS	0.2 x VDD	V	2
TF_{input_TEN}	TEN Input signal Falling time	–	10	ns	
TR_{input_TEN}	TEN Input signal Rising time	–	10	ns	

NOTE 1 Overshoot should not exceed the Vin Absolute Maximum Ratings.

NOTE 2 Undershoot should not exceed the Vin Absolute Maximum Ratings.

TEN Input Slew Rate Definition

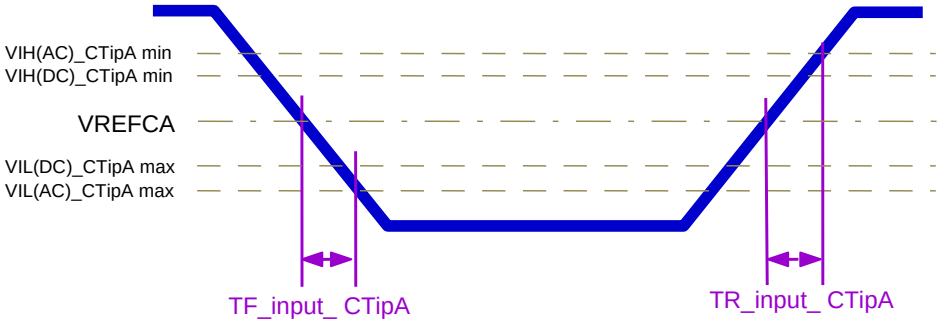


Single-Ended AC and DC Input levels for $\overline{CS}$, BA [1:0], BG [1:0], A [9:0], A10/AP, A12/$\overline{BC}$, A13, $\overline{WE}$/A14, $\overline{CAS}$/A15, $\overline{RAS}$/A16, CKE, $\overline{ACT}$, ODT, CK, $\overline{CK}$, and PAR

Parameter	Symbol	Min	Mix	Unit	Notes
CTipA AC Input High Voltage	VIH(AC)_CTipA	VREFCA + 0.2	Note 1	V	
CTipA DC Input High Voltage	VIH(DC)_CTipA	VREFCA + 0.15	VDD	V	
CTipA DC Input Low Voltage	VIL(DC)_CTipA	VSS	VREFCA - 0.15	V	
CTipA AC Input Low Voltage	VIL(AC)_CTipA	Note 1	VREFCA - 0.2	V	
CTipA Input signal Falling time	TF_input_CTipA	-	5	ns	
CTipA Input signal Rising time	TR_input_CTipA	-	5	ns	

NOTE 1 See “Overshoot and Undershoot Specifications”.

$\overline{CS}$ and Input a Slew Rate Definition

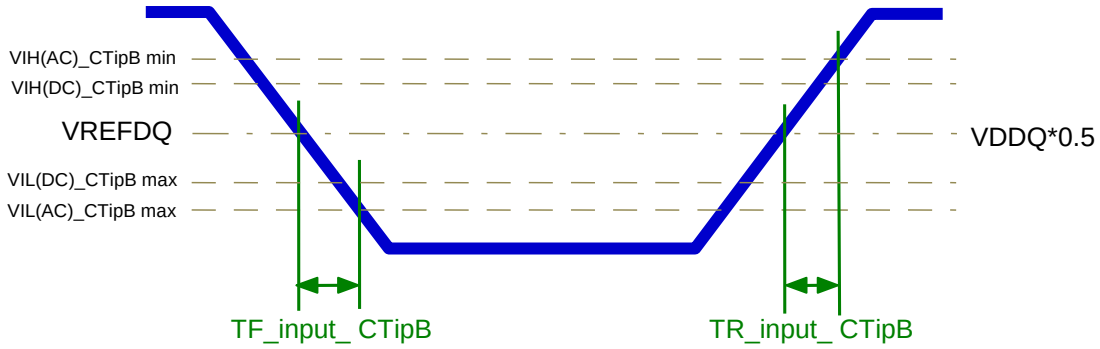


Single-Ended AC and DC Input levels for L$\overline{DM}$/L$\overline{DBI}$, U$\overline{DM}$/U$\overline{DBI}$ and $\overline{DM}$/$\overline{DBI}$

Parameter	Symbol	Min	Mix	Unit	Notes
CTipB AC Input High Voltage	VIH(AC)_CTipB	VREFDQ + 0.3	Note 2	V	1
CTipB DC Input High Voltage	VIH(DC)_CTipB	VREFDQ + 0.2	VDDQ	V	1
CTipB DC Input Low Voltage	VIL(DC)_CTipB	VSSQ	VREFDQ - 0.2	V	1
CTipB AC Input Low Voltage	VIL(AC)_CTipB	Note 2	VREFDQ - 0.3	V	1
CTipB Input signal Falling time	TF_input_CTipB	-	5	ns	
CTipB Input signal Rising time	TR_input_CTipB	-	5	ns	

NOTE 1 VREFDQ is VDDQ*0.5.
NOTE 2 See "Overshoot and Undershoot Specifications".

Input B Slew Rate Definition



Input Levels for $\overline{RESET}$

$\overline{RESET}$ input condition is the same as normal operation.

Input Levels for $\overline{ALERT}$

TBD

CLK to Read DQS timing parameters

DDR4 supports DLLOFF mode. Following parameters will be defined for CK to read DQS timings.

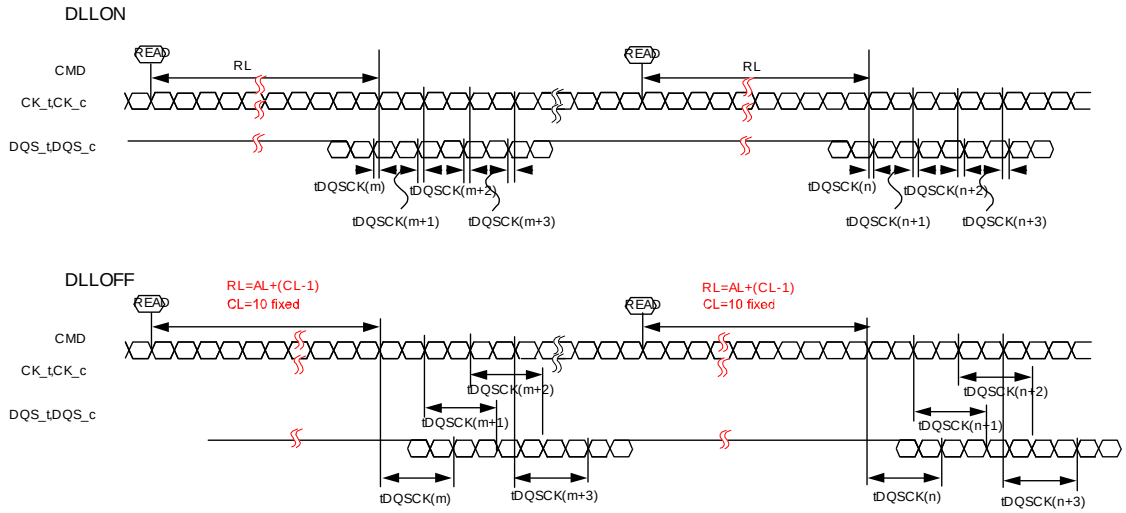
CLK to Read DQS Timing Parameters

Speed		DDR4-1600/1866/2133/2400/2666			
Parameter	**Symbol**	**Min**	**Max**	**Units**	**NOTE**
DQS, $\overline{DQS}$ rising edge output timing location from rising CK, $\overline{CK}$	tDQSCK (DLL On)	refer to AC parameter tables	refer to AC parameter tables	ps	1,3,7,8
	tDQSCK (DLL Off)	vendor specific	vendor specific	ps	2,3,7
DQS, $\overline{DQS}$ rising edge output variance window	tDQSCKi(DLL On)	-	refer to AC parameter tables	ps	1,5,6,7,8
	tDQSCKi(DLL Off)	-	vendor specific	ps	2,4,5,6,7
VDD sensitivity of tDQSCK (DLL Off)	dTDQSCKdV	-	vendor specific	ps/mV	2, 6
Temperature sensitivity of tDQSCK (DLL Off)	dTDQSCKdT	-	vendor specific	ps/°C	2, 6

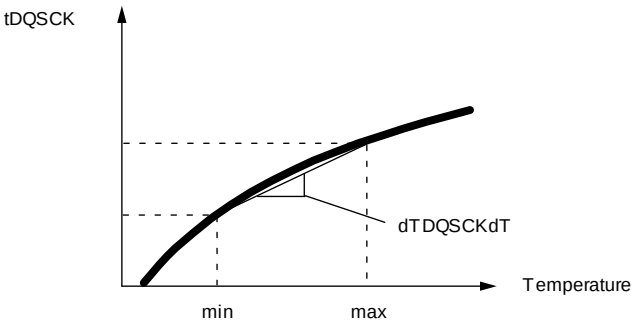
NOTE 1 These parameters are applied when DRAM is in DLLON mode.
NOTE 2 These parameters are applied when DRAM is in DLLOFF mode.
NOTE 3 Measured over full VDD and Temperature spec ranges.
NOTE 4 Measured at fixed and constant VDD and Temperature condition.
NOTE 5 Measured for a given DRAM part, and for each DQS/$\overline{DQS}$ pair in case of x16 (part variation is excluded).
NOTE 6 These parameters are verified by design and characterization, and may not be subject to production test.
NOTE 7 Assume no jitter on input clock signals to the DRAM.
NOTE 8 Refer to “READ Timing Definitions”.

tDQSCK (DLL On), Min limit = Earliest of {tDQSCKi (DLL On), at any valid VDD and Temperature, all DQS pairs and parts}
tDQSCK (DLL On), Max limit = Latest of {tDQSCKi (DLL On), at any valid VDD and Temperature, all DQS pairs and parts}
tDQSCK (DLL Off), Min limit = Earliest of {tDQSCKi (DLL Off), at any valid VDD and Temperature, all DQS pairs and parts}
tDQSCK (DLL Off), Max limit = Latest of {tDQSCKi (DLL Off), at any valid VDD and Temperature, all DQS pairs and parts}

tDQSCK Definition Difference between DLL ON and DLL OFF

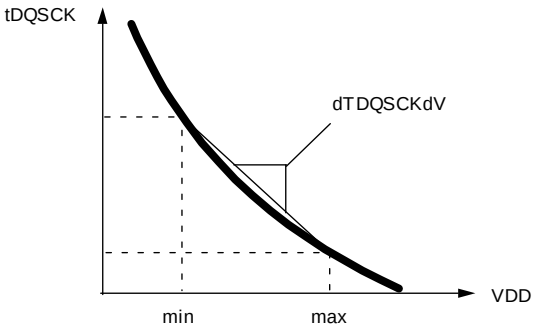


dTDQSCKTdT Definition



dTDQSCKdT = | tDQSCK(Toper,max) - tDQSCK(Toper,min)| / |Toper,max - Toper,min|

TDQSCKTdV Definition



dTDQSCKdV = | tDQSCK(VDD,max) - tDQSCK(VDD,min)| / |VDD,max - VDD,min|

Post Package Repair(hPPR)

DDR4 supports Fail Row address repair as optional feature for 4Gb and required for 8Gb and above. Supporting hPPR is identified via Datasheet and SPD in Module so should refer to DRAM manufacturer's Datasheet. PPR provides simple and easy repair method in the system and Fail Row address can be repaired by the electrical programming of Electrical-fuse scheme.

With hPPR, DDR4 can correct 1Row per Bank Group

Electrical-fuse cannot be switched back to un-fused states once it is programmed. The controller should prevent unintended hPPR

mode entry and repair. (i.e. Command/Address training period)

DDR4 defines two hard fail row address repair sequences and users can choose to use among those 2 command sequences. The first command sequence uses a WRA command and ensures data retention with Refresh operations except for the 2banks containing the rows being repaired, with BA [0] a don't care. Second command sequence is to use WR command and Refresh operation can't be performed in the sequence. So, the second command sequence doesn't ensure data retention for target DRAM.

When hard PPR Mode is supported, entry into hPPR Mode is to be is protected through a sequential MRS guard key to prevent unintentional hPPR programming. When soft PPR Mode, i.e. sPPR, is supported, entry into sPPR Mode is to be protected through a sequential MRS guard key to prevent unintentional sPPR programming. The sequential MRS guard key for hPPR mode and sPPR is the same Guard Key, i.e. hPPR/sPPR Guard Key.

The hPPR/sPPR Guard Key requires a sequence of four MR0 commands to be executed immediately after entering hPPR mode (setting MR4 bit 13 to a "1") or immediately after entering sPPR mode (setting MR4 bit 5 to a "1"). The hPPR/sPPR Guard Key's sequence must be entered in the specified order as stated and shown in the spec below. Any interruption of the hPPR/sPPR Guard Key sequence from other MR commands or non-MR commands such as ACT, WR, RD, PRE, REF, ZQ, NOP, RFU is not allowed.

Although interruption of the hPPR/sPPR Guard Key entry is not allowed, if the hPPR/sPPR Guard Key is not entering in the required order or is interrupted by other commands, the hPPR Mode or sPPR Mode will not execute and the offending command terminating hPPR/sPPR Mode may or may not execute correctly; however, the offending command will not cause the DRAM to "lock up". Additionally, when the hPPR or sPPR entry sequence is interrupted, subsequent ACT and WR commands will be conducted as normal DRAM commands. If a hPPR operation was prematurely terminated, the MR4 bit 13 must be re-set "0" prior to performing another hPPR or sPPR operation. If a sPPR operation was prematurely terminated, the MR4 bit 5 must be re-set to "0" prior to performing another sPPR or hPPR operation. The DRAM does not provide an error indication if an incorrect hPPR/sPPR Guard Key sequence is entered.

hPPR & sPPR MR0 Guard Key Sequences

Guard Keys	BG1:0[1]	BA1:0	A17:A12	A11	A10	A9	A8	A7	A6:A0
1st MR0	00	00	X	1	1	0	0	1	1111111
2nd MR0	00	00	X	0	1	1	1	1	1111111
3rd MR0	00	00	X	1	0	1	1	1	1111111
4th MR0	00	00	X	0	0	1	1	1	1111111

Note1 BG1 is 'Don't Care' in X16
Note2 A6:A0 can be either '1111111' or 'Don't Care'. And, it depends on vendor's implementation. '1111111' is allowed in all DDR4 density but 'Don't Care' in A6:A0 is only allowed in 4Gb & 8Gb die DDR4 product.
Note3 After completing hPPR & sPPR mode, MR0 must be re-programmed to pre-PPR mode state if the DRAM is to be accessed.

Hard Fail Row Address Repair (WRA Case)

The following is procedure of hPPR with WRA command.

1. Before entering 'hPPR' mode, all banks must be Precharged; DBI and CRC Modes must be disabled
2. Enable hPPR using MR4 bit "A13=1" and wait tMOD
3. Issue guard Key as four consecutive MR0 commands each with a unique address field A [17:0]. Each MR0 command should space by tMOD
4. Issue ACT command with Fail Row address
5. After tRCD, Issue WRA with VALID address. DRAM will consider Valid address with WRA command as 'Don't Care'
6. After WL(WL=CWL+AL+PL), All DQs of Target DRAM should be LOW for 4tCK. If HIGH is driven to All DQs of a DRAM consecutively for equal to or longer than 2tCK, then DRAM does not conduct hPPR and retains data if REF command is properly issued; if all DQs are neither LOW for 4tCK nor HIGH for equal to or longer than 2tCK, then hPPR mode execution is unknown.
7. Wait tPGM to allow DRAM repair target Row Address internally and issue PRE
8. Wait tPGM_Exit after PRE which allow DRAM to recognize repaired Row address
9. Exit hPPR with setting MR4 bit "A13=0"
10. DDR4 will accept any valid command after tPGMPST
11. In More than one fail address repair case, Repeat Step 2 to 9

In addition to that, hPPR mode allows REF commands from PL+WL+BL/2+tWR+tRP after WRA command during tPGM and tPGMPST for proper repair; provided multiple REF commands are issued at a rate of tREFI or tREFI/2, however back-to-back REF commands must be separated by at least tREFI/4 when the DRAM is in hPPR mode. Upon receiving REF command, DRAM performs normal Refresh operation and ensure data retention with Refresh operations except for the 2banks containing the rows being repaired, with BA A [0] don't care. Other command except REF during tPGM can cause incomplete repair so no other command except REF is allowed during tPGM.

Once hPPR mode is exited, to confirm if target row is repaired correctly, host can verify by writing data into the target row and reading

it back after hPPR exit with MR4 A13=0 and tPGMPST

Hard Fail Row Address Repair (WR Case)

The following is procedure of hPPR PPR with WR command.

1. Before entering hPPR mode, all banks must be precharged; DBI and CRC modes must be disabled.
2. Enable hPPR using MR4 bit “A13=1” and wait tMOD
3. Issue guard Key as four consecutive MR0 commands each with a unique address field A [17:0]. Each MR0 command should space by tMOD
4. Issue ACT command with row address
5. After tRCD, issue WR with valid address. DRAM consider the valid address with WR command as ‘Don’t Care’
6. After WL(WL=CWL+AL+PL), All DQs of target DRAM should be LOW for 4tCK. If HIGH is driven to All DQs of a DRAM consecutively for equal to or longer than first 2tCK, then DRAM does not conduct hPPR and retains data if REF command is properly issued; if all DQs are neither LOW for 4tCK nor HIGH for equal to or longer than first 2tCK, then hPPR mode execution is unknown.
7. Wait tPGM to allow DRAM repair target Row Address internally and issue PRE
8. Wait tPGM_Exit after PRE which allow DRAM to recognize repaired Row address
9. Exit hPPR with setting MR4 bit “A13=0”
10. DDR4 will accept any valid command after tPGMPST
11. In more than one fail address repair case, Repeat Step 2 to10

In this sequence, Refresh command is not allowed between hPPR MRS entry and exit.

Once hPPR mode is exited, to confirm if target row is repaired correctly, host can verify by writing data into the target row and reading it back after hPPR exit with MR4 A13=0 and tPGMPST.

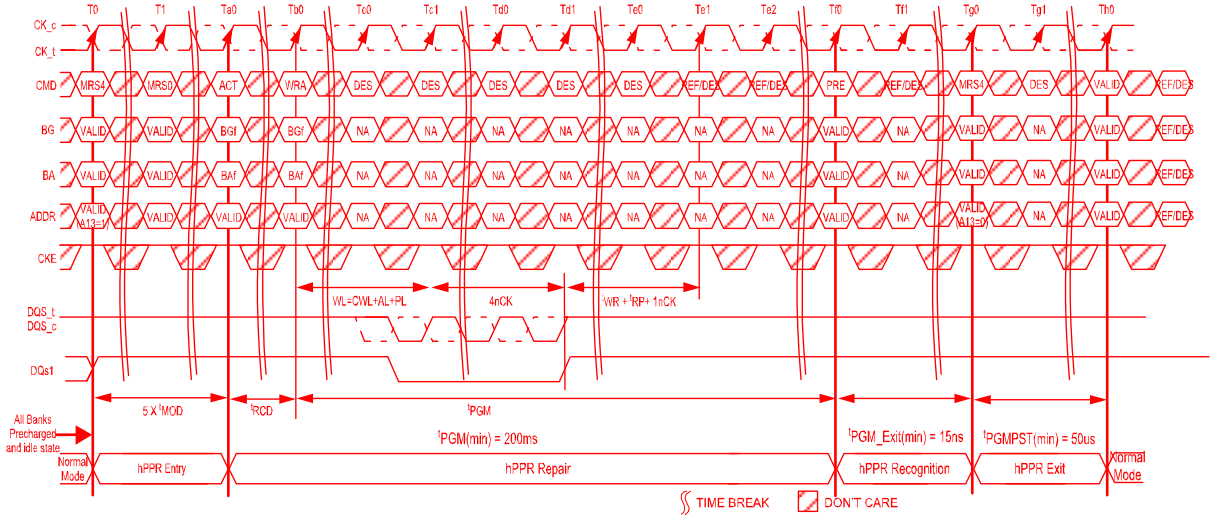
Hard Fail Row Address Repair MR bits and timing diagram

The following table and Timing diagram show hPPR related MR bits and its operation

hPPR Setting

MR4 [A13]	Description
0	hPPR Disabled
1	hPPR Enabled

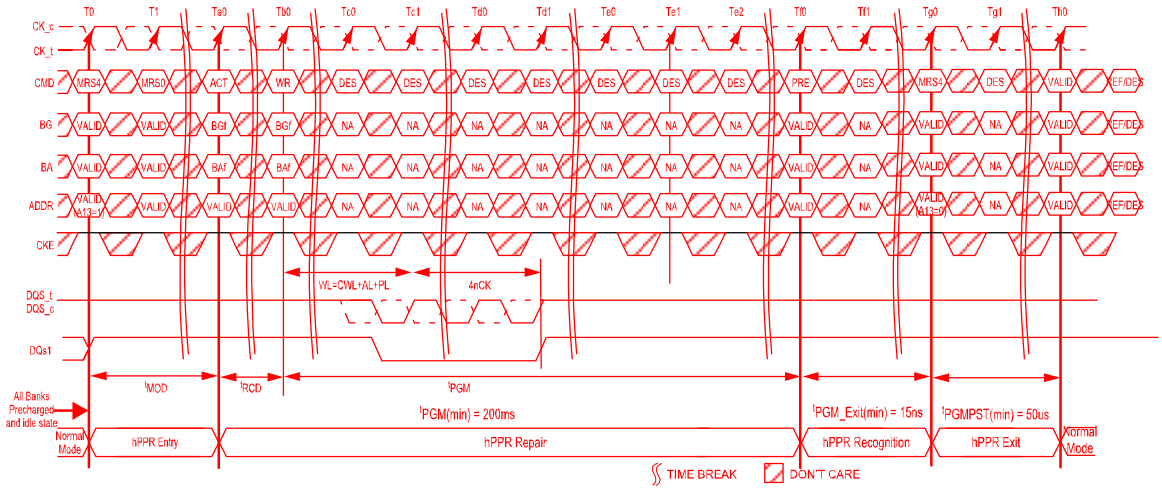
Hard Fail Row Repair (WRA Case)



Note1 Allow REF(1X) from PL+WL+BL/2+tWR+tRP after WR

Note2 Timing diagram shows possible commands but not all shown can be issued at same time; for example, if REF is issued at Te1, DES must be issued at Te2 as REF would be illegal at Te2. Likewise, DES must be issued tRFC prior to PRE at Tf0. All regular timings must still be satisfied.

Hard Fail Row Repair (WR Case)



Programming hPPR & sPPR support in MPR0 page2

hPPR & sPPR is optional feature of DDR4 4Gb so Host can recognize if DRAM is supporting hPPR & sPPR or not by reading out MPR0 Page2.

MPR page2;

hard PPR is supported: A7=1

hard PPR is not supported: A7=0

soft PPR is supported: A6=1

soft PPR is not supported: A6=0

Required Timing Parameters

Repair requires additional time period to repair Hard Fail Row Address into spare Row address and the followings are requirement timing parameters for hPPR

hPPR Timing Parameters

Speed		DDR4-1600/1866/2133/2400		DDR4-2666		Unit	Note
Parameter	Symbol	min	max	min	max		
hPPR Programming Time: x4/x8	tPGMa	1,000	-	1,000	-	ms	
hPPR Programming Time: x16	tPGMb	2,000	-	2,000	-	ms	
hPPR Exit Time	tPGM_Exit	15	-	15	-	ns	
New Address Setting time	tPGMPST	50	-	50	-	us	

Post Package Repair(sPPR)

Soft Post Package Repair (sPPR) is a way to quickly, but temporarily, repair a row element in a Bank Group on a DDR4 DRAM device, contrasted to hard Post Package Repair which takes longer but is permanent repair of a row element. There are some limitations and differences between sPPR and hPPR

Description and Comparison of hPPR & sPPR

Topic	Soft Repair	Hard Repair	Note
Persistence of Repair	Volatile – repair persists while power is within operating range	Non-Volatile – repair is permanent after the repair cycle.	sPPR cleared after power off or device reset
tPGM(hPPR & sPPR programming Time)	WL+ 4tCK+tWR	>1000ms(tPGMa) or 2000ms(tPGMb)	
# of Repair elements	1 per BG	1 per BG	Once hPPR is used within a BG,sPPR is no longer supported in that BG
Simultaneous use of soft and hard repair within a BG	Previous hPPR are allowed before soft repair to a different BG	Any outstanding sPPR must be cleared before a hard repair	Clearing sPPR occurs by either (a) or (b): (a) powerdown and power-up sequence (b) Reset and re-initialize.
Repair Sequence	1 method – WR cmd.	2 methods WRA and WR	
Bank[1] not having row repair retains array data	Yes	Yes, if WRA sequence; No, if WR sequence	WRA sequence requires use of REF commands
Bank[1] having row repair retain array data	Yes, except for seed and associated rows	No	sPPR must be performed outside of REF window (tRFC)

Note1 If a BA pin is defined to be an “sPPR associated row” to the seed row, both states of the BA address input are affected. For example, if BA0 is selected as an “sPPR associated row” to the seed row, addresses in both BA0 = 0 and BA0 = 1 are equally affected.

sPPR mode is entered in a similar fashion as hPPR, sPPR uses MR4 bit A5 while hPPR uses MR4 bit A13; sPPR requires the same guard key sequence as hPPR to qualify the MR4 PPR entry. Prior to sPPR entry, either an hPPR exit command or an sPPR exit command should be performed, which ever was the last PPR entry. After sPPR entry, an ACT command will capture the target bank

and target row, herein seed row, where the row repair will be made. After tRCD time, a WR command is used to select the individual DRAM, through the DQ bits, to transfer the repair address into an internal register in the DRAM. After a write recovery time and PRE command, the sPPR mode can be exited and normal operation can resume. The DRAM will retain the sPPR change as long as VDD remains within the operating region. If the DRAM power is removed or the DRAM is RESET, all sPPR changes will revert to the unrepaired state. sPPR changes must be cleared by either a power-up sequence or re-initialization by RESET signal before hPPR mode is enabled.

DDR4 sPPR can repair one row per Bank Group, however when the hPPR resources for a bank group have been used, sPPR resources are no longer available for that bank group. If an sPPR or hPPR repair sequence is issued to a bank group with PPR resource un-available, the DRAM will ignore the programming sequence. sPPR mode is optional for 4Gb & 8Gb density DDR4 devices and required for densities which are larger than 8Gb.

The bank receiving sPPR change is expected to retain array data in all other rows except for the seed row and its associated row addresses on all densities larger than 8Gb; and is optional for 8Gb devices and smaller. If the user does not require the data in the array in the bank under sPPR repair to be retained, then the handling of the seed row's associated row addresses is not of interest and can be ignored. If the user requires the data in the array to be retained in the bank under sPPR mode, then prior to executing the sPPR mode, the seed row and its associated row addresses should be backed up and restored after sPPR has been completed. sPPR associated seed row addresses are specified in below.

sPPR associated row address

sPPR Associated Row Addresses							
BA0	A17	A16	A15	A14	A13	A1	A0

Soft Repair of a Fail Row Address

The following is the procedure of sPPR with WR command. Note that during the soft repair sequence, no refresh is allowed.

1. Before entering 'sPPR' mode, all banks must be Precharged; DBI and CRC Modes must be disabled
2. Enable sPPR using MR4 bit "A5=1" and wait tMOD
3. Issue Guard Key as four consecutive MR0 commands each with a unique address field A[17:0]. Each MR0 command should space by tMOD. MR0 Guard Key sequence is same as hPPR in hPPR.

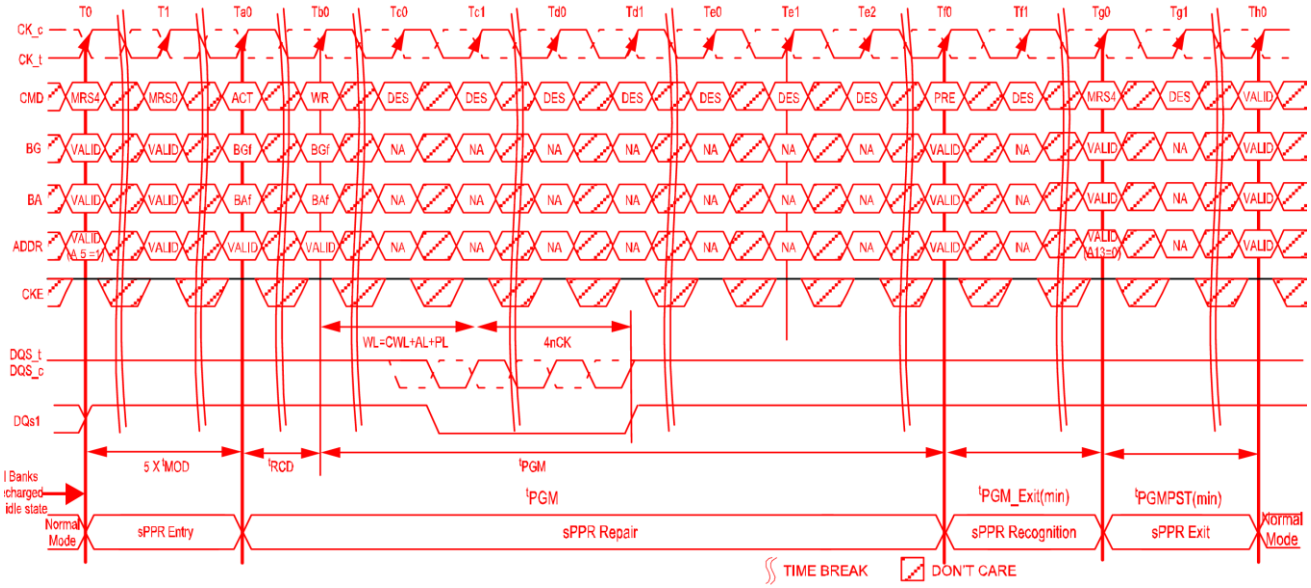
Guard Keys	BG1:0[1]	BA1:0	A17:A12	A11	A10	A9	A8	A7	A6:A0
1st MR0	00	00	X	1	1	0	0	1	1111111
2nd MR0	00	00	X	0	1	1	1	1	1111111
3rd MR0	00	00	X	1	0	1	1	1	1111111
4th MR0	00	00	X	0	0	1	1	1	1111111

4. Issue ACT command with the Bank and Row Fail address, Write data is used to select the individual DRAM in the Rank for repair.
5. A WR command is issued after tRCD, with VALID column address. The DRAM will ignore the column address given with the WR command.
6. After WL(WL=CWL+AL+PL), All DQs of Target DRAM should be LOW for 4tCK. If HIGH is driven to All DQs of a DRAM consecutively for equal to or longer than first 2tCK, then DRAM does not conduct sPPR. If all DQs are neither LOW for 4tCK nor HIGH for equal to or longer than first 2tCK, then sPPR mode execution is unknown.
7. Wait tWR for the internal repair register to be written and then issue PRE to the Bank.
8. Wait 20ns after PRE which allow DRAM to recognize repaired Row address
9. Exit PPR with setting MR4 bit "A5=0" and wait tMOD
10. One soft repair address per Bank Group is allowed before a hard repair is required. When more than one sPPR request is made to the same BG, the most recently issued sPPR address would replace the early issued one. In the case of

conducting soft repair address in a different Bank Group, Repeat Step 2 to 9. During a soft Repair, Refresh command is not allowed between sPPR MRS entry and exit.

Once sPPR mode is exited, to confirm if target row is repaired correctly, the host can verify the repair by writing data into the target row and reading it back after sPPR exit with MR4 A5=0.

Fail Row Soft PPR (WR Case)

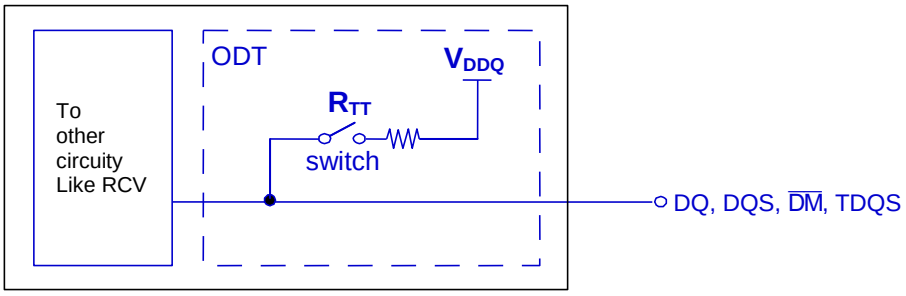


On-Die Termination

On-die termination (ODT) is a feature of the DDR4 SDRAM that enables the DRAM to change termination resistance for each DQ, DQS, $\overline{DQS}$, and $\overline{DM}$ for x4 and x8 configuration (and DQS, $\overline{TDQS}$, for x8 configuration, when enabled via A11 = 1 in MR1) via the ODT control pin or WRITE command or default parking value with MR setting. For x16 configuration, ODT is applied to each DQ, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$, $\overline{UDM}$ and $\overline{LDM}$ signal. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently change termination resistance for any or all DRAM devices.

The ODT feature is turned off and not supported in self refresh mode. A simple functional representation of the DRAM ODT feature is shown below.

Functional Representation of ODT



The switch is enabled by the internal ODT control logic, which uses the external ODT pin and Mode Register Setting and other control information. The value of RTT is determined by the settings of mode register bits (see Mode Register). The ODT pin will be ignored if the mode register MR1 is programmed to disable RTT_NOM (MR1 A [10:8] = 000) and in self refresh mode.

ODT Mode Register and ODT State Table

The ODT mode of the DDR4 device has 4 states: data termination disable, RTT_WR, RTT_NOM and RTT_PARK. The ODT mode is enabled if any of RTT_NOM: MR1 A [10:8], RTT_WR: MR2[11:9] or RTT_PARK: MR5[8:6] are non-zero. When enabled, the value of RTT is determined by the settings of these bits.
After entering Self-Refresh mode, DRAM automatically disables ODT termination and set Hi-Z as termination state regardless of these setting.

Controller can control each RTT condition with WR/RD command and ODT pin

- RTT_WR: The rank that is being written to provide termination regardless of ODT pin status (either HIGH or LOW).
- RTT_NOM: DRAM turns ON RTT_NOM if it sees ODT asserted (except when ODT is disabled by MR1).
- RTT_PARK: Default parked value set via MR5 to be enabled and ODT pin is driven LOW.
- Data Termination Disable: DRAM driving data upon receiving READ command disables the termination after RL-X and stays off for a duration of BL/2 + X clock cycles. (X is 2 for 1tCK and 3 for 2tCK preamble mode.)

The RTT values have the following priority:
if there is WRITE command along with ODT pin HIGH, then DRAM turns on RTT_WR not RTT_NOM, and also if there is

READ command, then DRAM disables data termination regardless of ODT pin and goes into Driving mode.

• Data termination disable

• RTT_WR

• RTT_NOM

• RTT_PARK

Termination State Table

RTT_PARK MR5[8:6]	RTT_NOM MR1[10:8]	ODT pin	DRAM termination state	Note
Enabled	Enabled	HIGH	RTT_NOM	1,2
		LOW	RTT_PARK	1,2
	Disabled	Don't care[3]	RTT_PARK	1,2,3
Disabled	Enabled	HIGH	RTT_NOM	1,2
		LOW	Hi-Z	1,2
	Disabled	Don't care[3]	Hi-Z	1,2,3

NOTE 1 When a READ command is executed, DRAM termination state will be High-Z for defined period independent of ODT pin and MR setting of RTT_PARK/RTT_NOM. This is described in the ODT During Read section.

NOTE 2 If RTT_WR is enabled, RTT_WR will be activated by WRITE command for defined period time independent of ODT pin and MR setting of RTT_PARK /RTT_NOM. This is described in the Dynamic ODT section.

NOTE 3 If RTT_NOM MR is disabled, ODT receiver power will be turned off to save power.

On-die termination effective resistances are defined and can be selected by any or all of the following options:

• MR1[10:8] (RTT_NOM) - Disable, 240Ω, 120Ω, 80Ω, 60Ω, 48Ω, 40Ω, and 34Ω.

• MR2[11:9] (RTT_WR) - Disable, 240Ω,120Ω, and 80Ω.

• MR5[8:6] (RTT_PARK) - Disable, 240Ω, 120Ω, 80Ω, 60Ω, 48Ω, 40Ω, and 34Ω.

ODT is applied to the following inputs:

• X4: DQs, $\overline{DM}$, DQS, and DQS inputs.

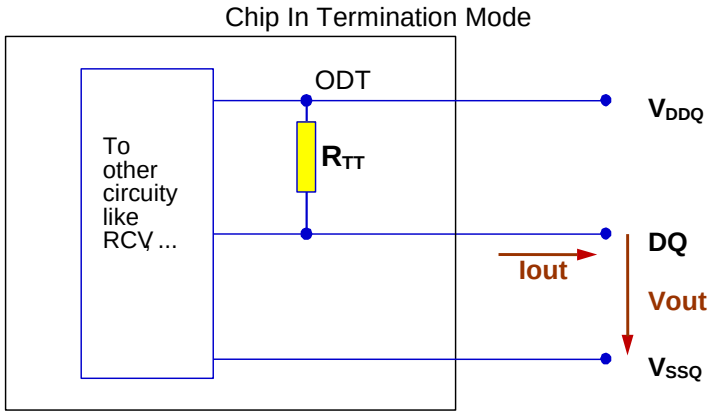
• X8: DQs, $\overline{DM}$, DQS, $\overline{DQS}$, TDQS, and $\overline{TDQS}$ inputs.

• X16: DQs, $\overline{LDM}$, $\overline{UDM}$, LDQS, $\overline{DQS}$, UDQS, and $\overline{DQSU}$ inputs.

ODT Definition of Voltages and Currents

On die termination effective Rtt values supported are 240, 120, 80, 60, 48, 40, 34 ohms.

$$RTT = \frac{VDDQ - Vout}{|\ Iout\ |}$$



ODT Electrical Characteristics RZQ=240Ω +/-1% entire temperature operation range after ZQ calibration

RTT	Vout	Min	Nom	Max	Unit	NOTE
240Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ	1,2,3
120Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/2	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/2	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/2	1,2,3
80Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/3	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/3	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/3	1,2,3
60Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/4	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/4	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/4	1,2,3
48Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/5	1,2,3
40Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/6	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/6	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/6	1,2,3
34Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/7	1,2,3
DQ-DQ Mismatch within byte	VOMdc = 0.8* VDDQ	0	-	10	%	1,2,4,5,6

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

NOTE 2 Pull-up ODT resistors are recommended to be calibrated at 0.8*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5*VDDQ and 1.1*VDDQ.

NOTE 3 The tolerance limits are specified under the condition that VDDQ=VDD and VSSQ=VSS

NOTE 4 DQ to DQ mismatch within byte variation for a given component including DQS and $\overline{DQS}$(characterized)

NOTE 5 RTT variance range ratio to RTT Nominal value in a given component, including DQS and $\overline{DQS}$.

$$\text{DQ-DQ Mismatch in a device} = \frac{RTTmax - RTTmin}{RTTNOM} * 100$$

NOTE 6 This parameter of x16 device is specified for Upper byte and Lower byte.

Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes are:

- Any bank active with CKE HIGH
- Refresh with CKE HIGH
- Idle mode with CKE HIGH
- Active power-down mode (regardless of MR1 bit A10)
- Precharge power-down mode

In synchronous ODT mode, RTT_NOM will be turned on DODTLon clock cycles after ODT is sampled HIGH by a rising clock edge and turned off DODTLoff clock cycles after ODT is registered LOW by a rising clock edge. The ODT latency is tied to the Write Latency (WL = CWL + AL + PL) by: DODTLon = WL - 2; DODTLoff = WL - 2. When operating in 2tCK Preamble Mode, The ODT latency must be 1 clock smaller than in 1tCK Preamble Mode; DODTLon =WL - 3; DODTLoff = WL - 3."(WL = CWL+AL+PL)

ODT Latency and Posted ODT

In Synchronous ODT Mode, the Additive Latency (AL) and the Parity Latency (PL) programmed into the Mode Register MR1 applies to ODT Latencies as shown below:

ODT Latency

Symbol	Parameter	1 tCK Preamble	2 tCK Preamble	Unit
DODTLon	Direct ODT turn on Latency	CWL + AL + PL – 2	CWL + AL + PL – 3	tCK
DODTLoff	Direct ODT turn off Latency	CWL + AL + PL – 2	CWL + AL + PL – 3	
RODTLoff	Read command to internal ODT turn off Latency	CWL + AL + PL – 2	CWL + AL + PL – 3	
RODTLon4	Read command to RTT_PARK turn on Latency in BC4	RODTLoff + 4	RODTLoff + 5	
RODTLon8	Read command to RTT_PARK turn on Latency in BC8/BL8	RODTLoff + 6	RODTLoff + 7	
ODTH4		4	5	
ODTH8		6	7	

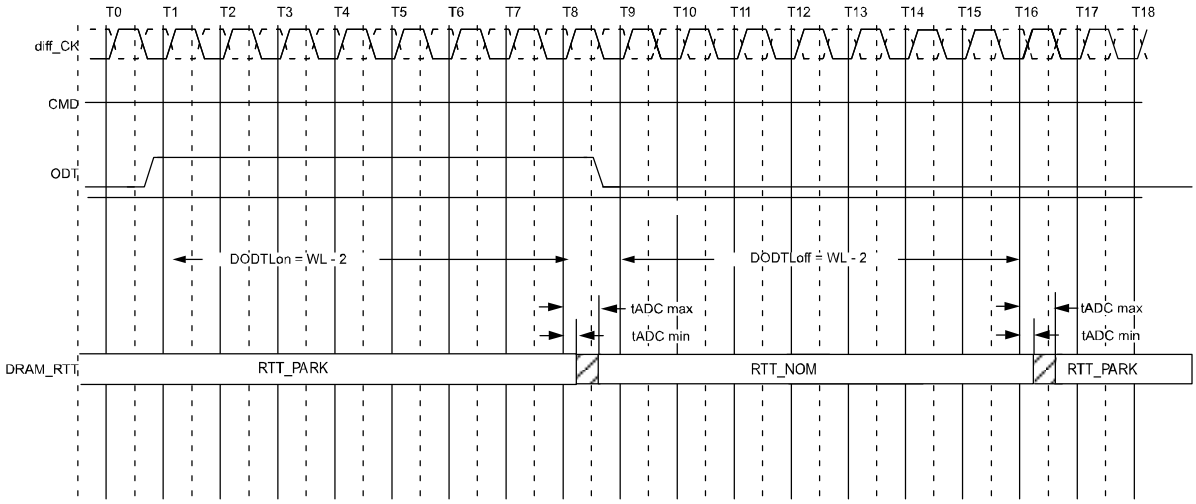
Timing Parameters

In synchronous ODT mode, the following parameters apply:

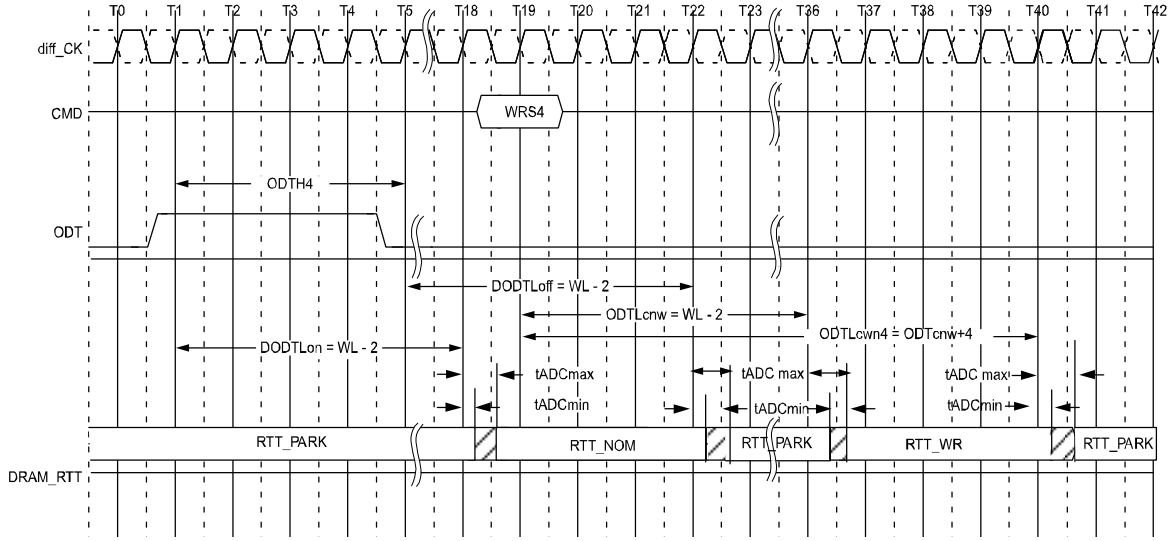
- DODTLon, DODTLoff, RODTLoff, RODTLon4, RODTLon8, tADC (MIN) (MAX).
- tADC (MIN) and tADC (MAX) are minimum and maximum RTT change timing skew between different termination values. These timing parameters apply to both the synchronous ODT mode and the data termination disable mode.

When ODT is asserted, it must remain HIGH until minimum ODTH4 (BL = 4) or ODTH8 (BL = 8) is satisfied. Additionally, depending on CRC or 2tCK preamble setting in MRS, ODTH should be adjusted.

Synchronous ODT Timing Example for CWL=9, AL=0, PL=0; DODTLon=WL-2=7; DODTLoff=WL-2=7



Synchronous ODT example with BL=4, CWL=9, AL=10, PL=0; DODTLon/off=WL-2=17, ODTcnw=WL-2=17

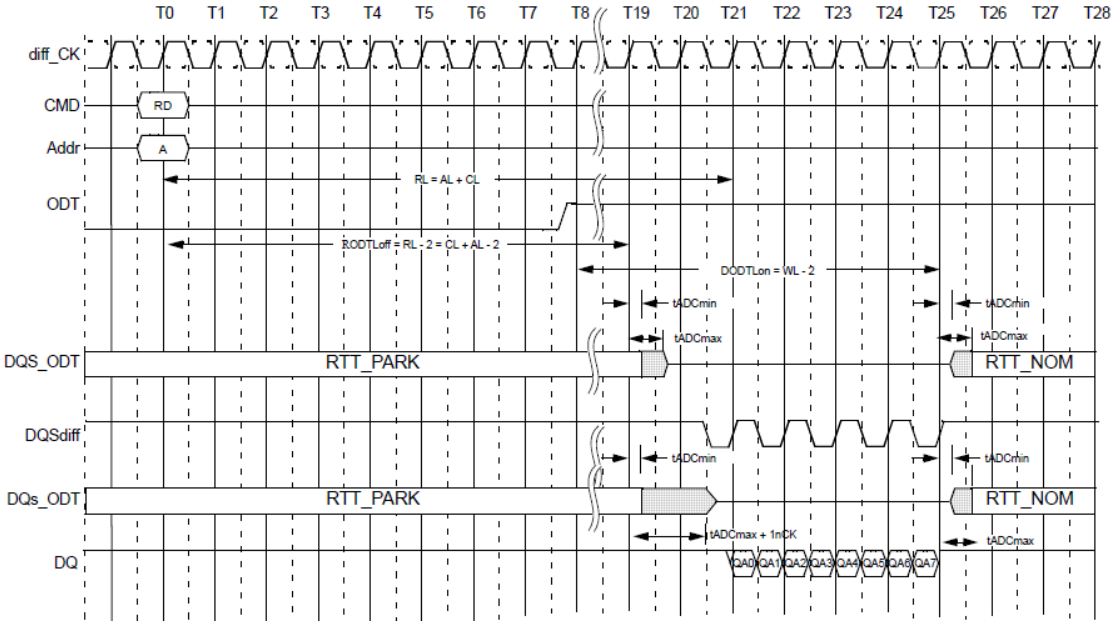


ODT must be held HIGH for at least ODTH4 after assertion (T1). ODTH is measured from ODT first registered HIGH to ODT first registered LOW, or from registration of Write command. Note that ODTH4 should be adjusted depending on CRC or 2tCK preamble setting

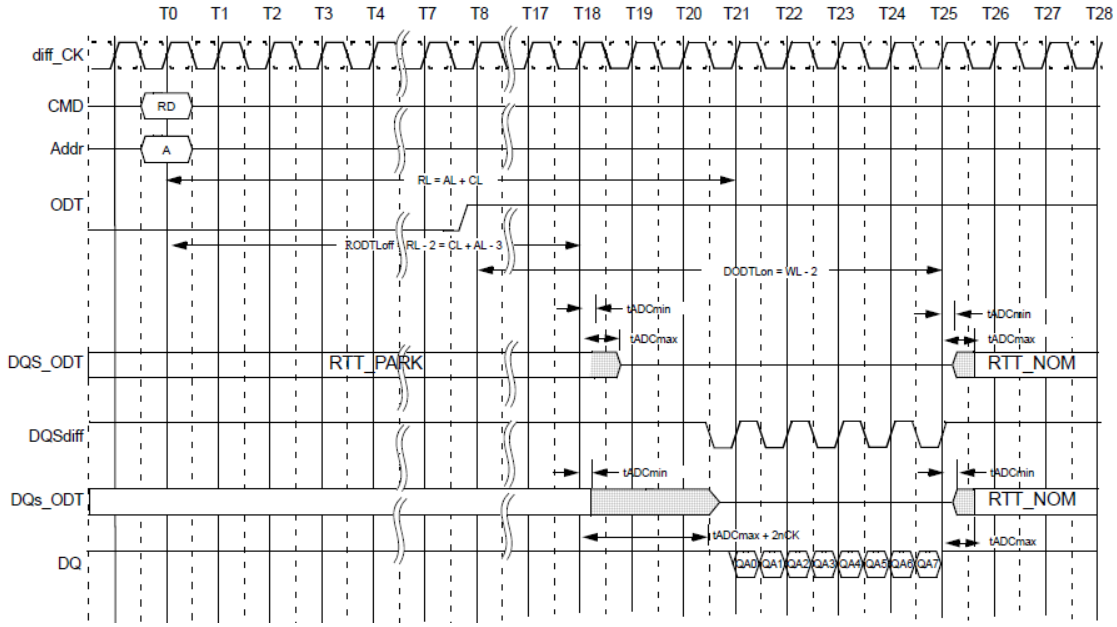
ODT During Reads

Because the DRAM cannot terminate with RTT and drive with RON at the same time; RTT may nominally not be enabled until the end of the postamble as shown in the example below. At cycle T25, the device turns on the termination when it stops driving, which is determined by tHZ. If the DRAM stops driving early (that is, tHZ is early), then tADC (MIN) timing may apply. If the DRAM stops driving late (that is, tHZ is late), then the DRAM complies with tADC (MAX) timing.

Example: CL=11, PL=0; AL=CL-1=10; RL=AL+PL+CL=21; CWL=9; DODTLon=AL+CWL-2=17; DODTLoff=AL+CWL-2=17;1tCK preamble)



Example: CL=11, PL=0; AL=CL-1=10; RL=AL+PL+CL=21; CWL=9; DODTLon= AL+CWL-2=17; DODTLoff=AL+CWL-2=17;2tCK preamble)



Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the device can be changed without issuing an MRS command. This requirement is supported by the dynamic ODT feature, described below.

Functional Description

The dynamic ODT mode is enabled if bit A9 or A10 of MR2 is set to 1.

• Three RTT values are available: RTT_NOM, RTT_WR, and RTT_PARK.

– The value for RTT_NOM is preselected via bits MR1[10:8].

– The value for RTT_WR is preselected via bits MR2[11:9].

– The value for RTT_PARK is preselected via bits MR5[8:6].

• During operation without WRITE commands, the termination is controlled as follows:

- Nominal termination strength RTT_NOM or RTT_PARK is selected.
- RTT_NOM on/off timing is controlled via ODT pin and latencies DODTLon and DODTLoff; and RTT_PARK is on when ODT is LOW.

• When a WRITE command (WR, WRA, WRS4, WRS8, WRAS4, WRAS8) is registered, and if Dynamic ODT is enabled, the termination is controlled as follows:

- Latency ODTLcnw after the WRITE command, termination strength RTT_WR is selected.
- Latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the WRITE command, termination strength RTT_WR is deselected. One or two clocks will be added into or subtracted from ODTLcwn8 and ODTLcwn4, depending on Write CRC Mode and/or 2 tCK preamble enablement.

The following table shows latencies and timing parameters which are relevant for the on-die termination control in dynamic ODT mode. The dynamic ODT feature is not supported in DLL-off mode. MRS command must be used to set RTT_WR, MR2[11:9] = 000, to disable dynamic ODT externally.

Latencies and timing parameters relevant for Dynamic ODT with 1tCK preamble mode and CRC disabled

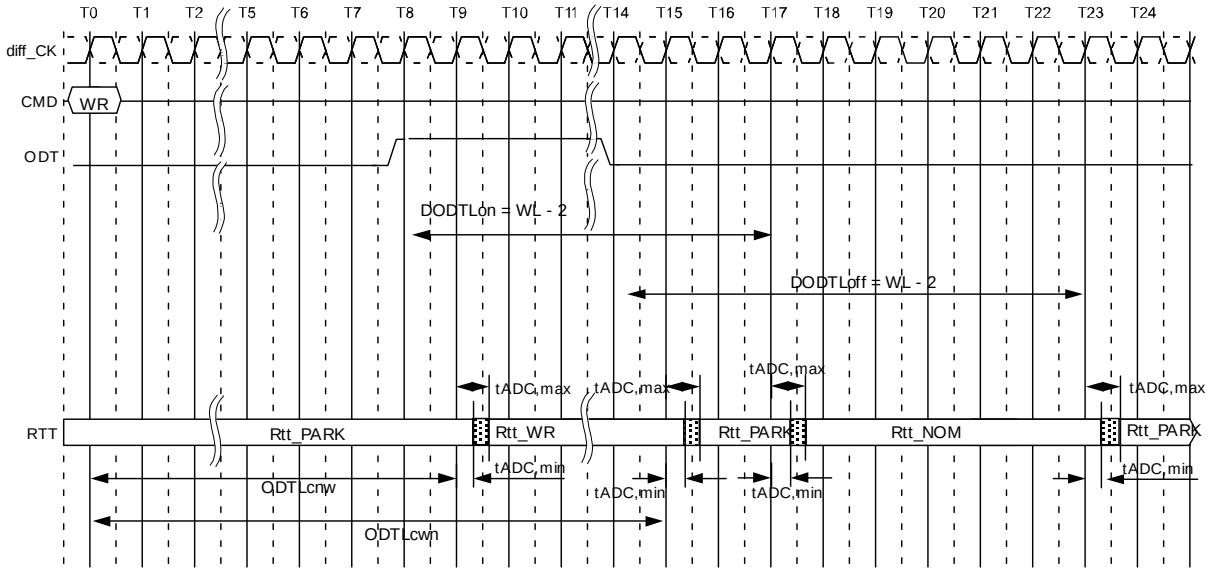
Name and Description	Abbr.	Defined from	Define to	1600/1866 /2133/2400	2666	Unit
ODT Latency for changing from RTT_PARK/RTT_NOM to RTT_WR	**ODTLcnw**	Registering external write command	Change RTT strength from RTT_PARK/RTT_NOM to RTT_WR	ODTLcnw = WL - 2		tCK
ODT Latency for change from RTT_WR to RTT_PARK/RTT_NOM (BL = 4)	**ODTLcwn4**	Registering external write command	Change RTT strength from RTT_WR to RTT_PARK/RTT_NOM	ODTLcwn4 = 4 + ODTLcnw		tCK
ODT Latency for change from RTT_WR to RTT_PARK/RTT_NOM (BL = 8)	**ODTLcwn8**	Registering external write command	Change RTT strength from RTT_WR to RTT_PARK/RTT_NOM	ODTLcwn8 = 6 + ODTLcnw		tCK(avg)
RTT change skew	**tADC**	ODTLcnw ODTLcwn	RTT valid	tADC(min) = 0.3 tADC(max) = 0.7	tADC(min) = 0.28 tADC(max) = 0.72	tCK(avg)

Latencies and timing parameters relevant for Dynamic ODT with 1 and 2tCK preamble mode and CRC en/disabled

Symbol	1tck Preamble		2tck Preamble		Unit
	CRC off	CRC on	CRC off	CRC on	
ODTLcnw	WL - 2	WL - 2	WL - 3	WL - 3	tCK
ODTLcwn4	ODTLcnw +4	ODTLcnw +7	ODTLcnw +5	ODTLcnw +8	
ODTLcwn8	ODTLcnw +6	ODTLcnw +7	ODTLcnw +7	ODTLcnw +8	

ODT Timing Diagrams

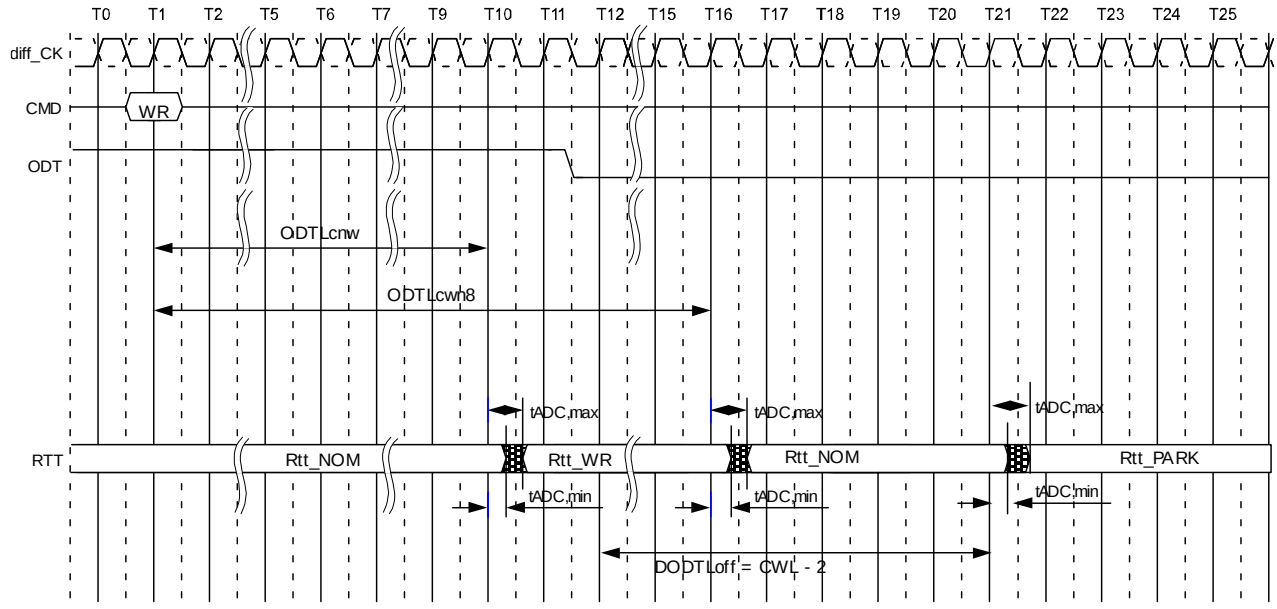
Dynamic ODT (1t CK Preamble; CL = 14, CWL = 11, BL = 8, AL = 0, CRC Disabled)



NOTE 1 ODTLcnw = WL - 2 (1 tCK preamble) or WL - 3 (2 tCK preamble).

NOTE 2 If BC4 then ODTLcwn = WL+4 if CRC disabled or WL+5 if CRC enabled; If BL8 then ODTLcwn = WL+6 if CRC disabled or WL+7 if CRC enabled.

Dynamic ODT Overlapped with RTT_NOM (CL=14, CWL=11, BL=8, AL=0, CRC Disabled)



NOTE 1 Behavior with WR command issued while ODT is being registered HIGH.

Asynchronous ODT Mode

Asynchronous ODT mode is selected when DLL is disabled by MR1 bit A0='0'b.

In asynchronous ODT timing mode, internal ODT command is not delayed by either the Additive latency (AL) or relative to the external ODT signal (RTT_NOM). In asynchronous ODT mode, the following timing parameters apply tAONAS,min, max, tAOFAS,min,max.

Minimum RTT_NOM turn-on time (tAONASmin) is the point in time when the device termination circuit leaves RTT_PARK and ODT resistance begins to change. Maximum RTT_NOM turn on time(tAONASmax) is the point in time when the ODT resistance is reached RTT_NOM.

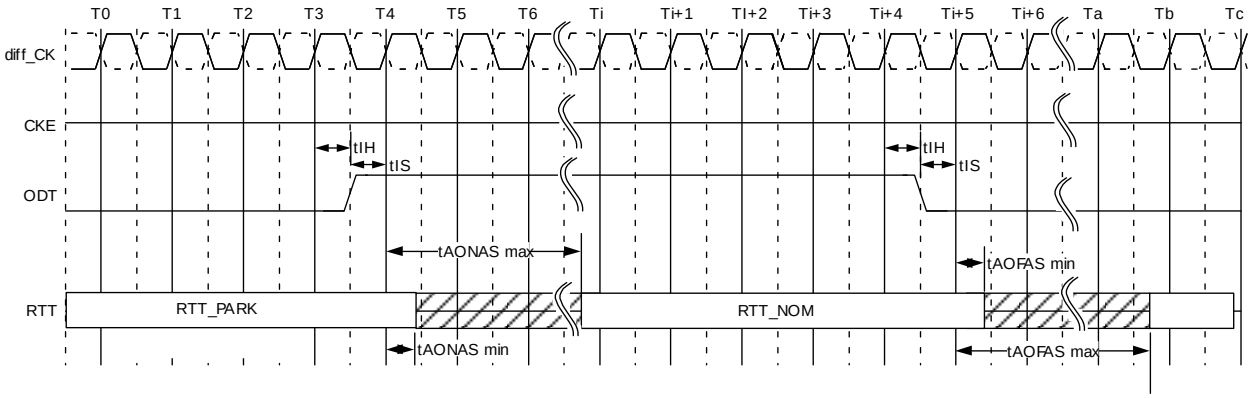
tAONASmin and tAONASmax are measured from ODT being sampled high.

Minimum RTT_NOM turn-off time (tAOFASmin) is the point in time when the devices termination circuit starts to leave RTT_NOM.

Maximum RTT_NOM turn-off time (tAOFASmax) is the point in time when the on-die termination has reached RTT_PARK.

tAOFASmin and tAOFASmax are measured from ODT being sampled low.

Asynchronous ODT Timings with DLL Off



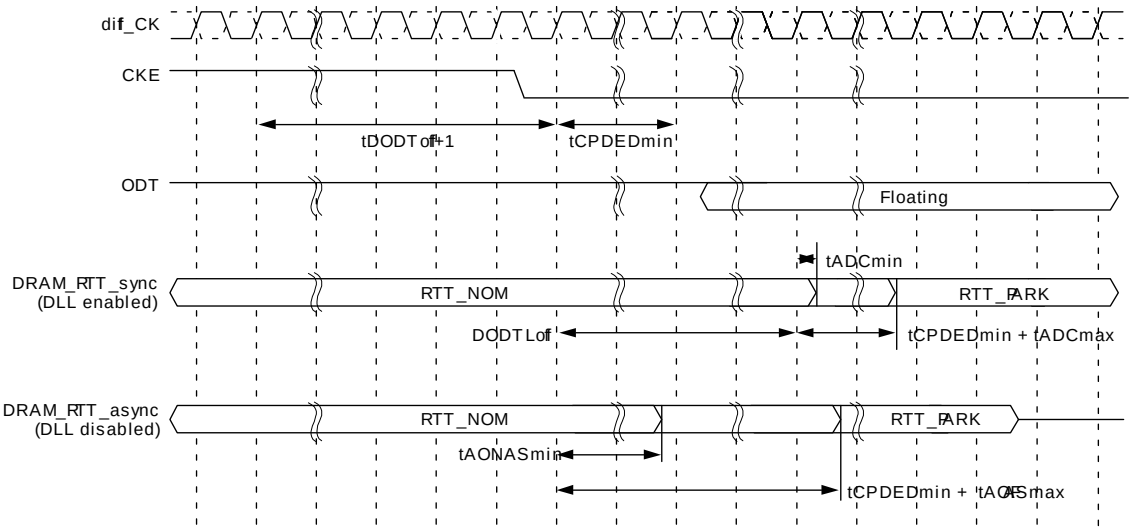
Asynchronous ODT Timing Parameters for all Speed Bins

Description	Symbol	Min.	Max.	Unit
Asynchronous RTT turn-on delay	tAONAS	1.0	9.0	ns
Asynchronous RTT turn-off delay	tAOFAS	1.0	9.0	ns

ODT buffer disabled mode for Power down

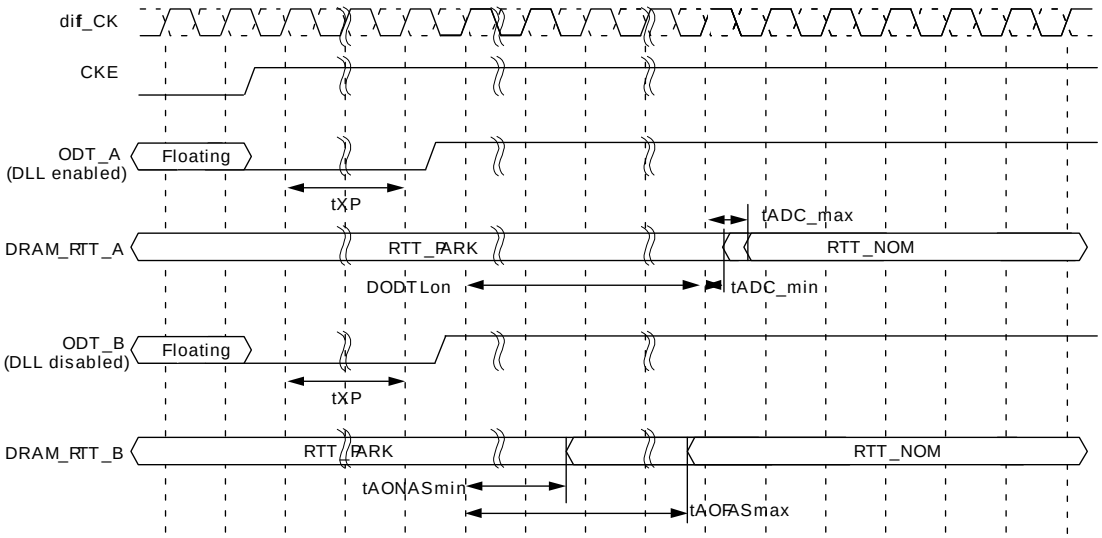
DRAM does not provide Rtt_NOM termination during power down when ODT input buffer deactivation mode is enabled in MR5 bit A5. To account for DRAM internal delay on CKE line to disable the ODT buffer and block the sampled output, the host controller must continuously drive ODT to either low or high when entering power down. The ODT signal may be floating after tCPDEDmin has expired. In this mode, RTT_NOM termination corresponding to sampled ODT at the input after CKE is first registered low (and tANPD before that) may not be provided. tANPD is equal to (WL-1) and is counted backwards from PDE.

ODT timing for power down entry with ODT buffer disable mode



When exit from power down, along with CKE being registered high, ODT input signal must be re-driven and maintained low until tXP is met.

ODT timing for power down exit with ODT buffer disable mode

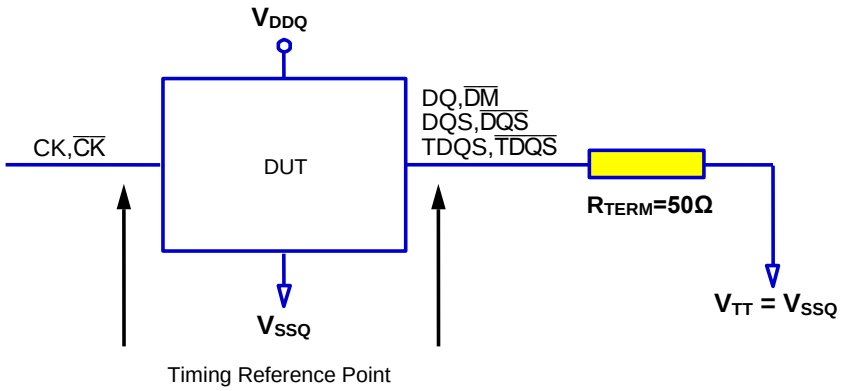


ODT Timing Definitions

Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined below

ODT Timing Reference Load



ODT Timing Definitions

Definitions for tADC, tAONAS and tAOFAS are provided in the Table and measurement reference settings are provided in the subsequent. The tADC for the Dynamic ODT case and Read Disable ODT cases are represented by tADC of Direct ODT Control case.

ODT Timing Definitions

Symbol	Begin Point Definition	End Point Definition
tADC	Rising edge of CK, CK defined by the end point of **DODTLoff**	Extrapolated point at V_{RTT_NOM}
	Rising edge of CK, CK defined by the end point of **DODTLon**	Extrapolated point at V_{SSQ}
	Rising edge of CK - CK defined by the end point of **ODTLcnw**	Extrapolated point at V_{RTT_NOM}
	Rising edge of CK - CK defined by the end point of **ODTLcwn4** or **ODTLcwn8**	Extrapolated point at V_{SSQ}
tAONAS	Rising edge of CK, CK with ODT being first registered high	Extrapolated point at V_{SSQ}
tAOFAS	Rising edge of CK, CK with ODT being first registered low	Extrapolated point at V_{RTT_NOM}

Reference Settings for ODT Timing Measurements

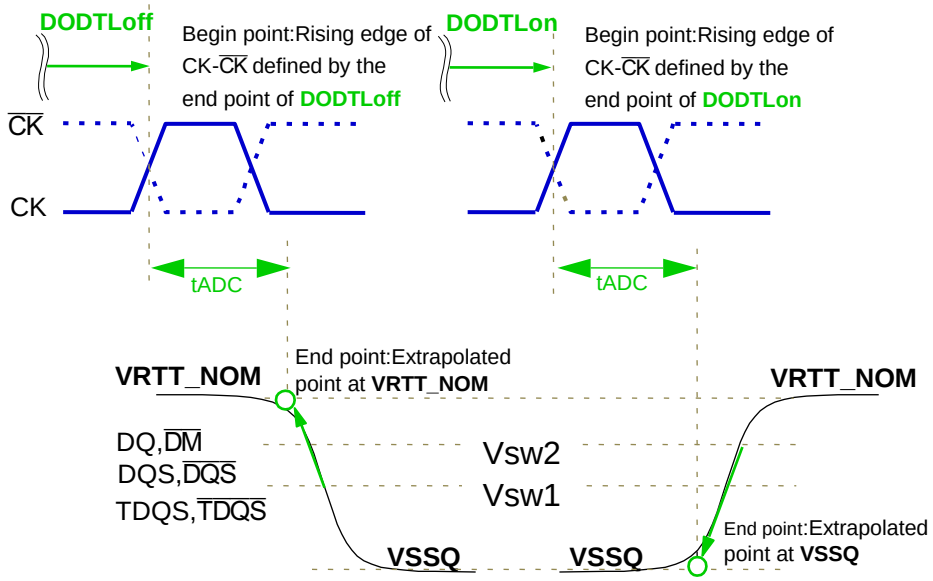
Measured Parameter	RTT_PARK	RTT_NOM	RTT_WR	Vsw1	Vsw2	Note
tADC	Disable	RZQ/7	–	0.20V	0.40V	1,2
	–	RZQ/7	Hi-Z	0.20V	0.40V	1,3
tAONAS	Disable	RZQ/7	–	0.20V	0.40V	1,2
tAOFAS	Disable	RZQ/7	–	0.20V	0.40V	

NOTE 1 MR setting is as follows.
- MR1 A10=1, A9=1, A8=1 (RTT_NOM_Setting)
- MR5 A8=0, A7=0, A6=0 (RTT_PARK Setting)
- MR2 A11=0, A10=1, A9=1 (RTT_WR Setting)

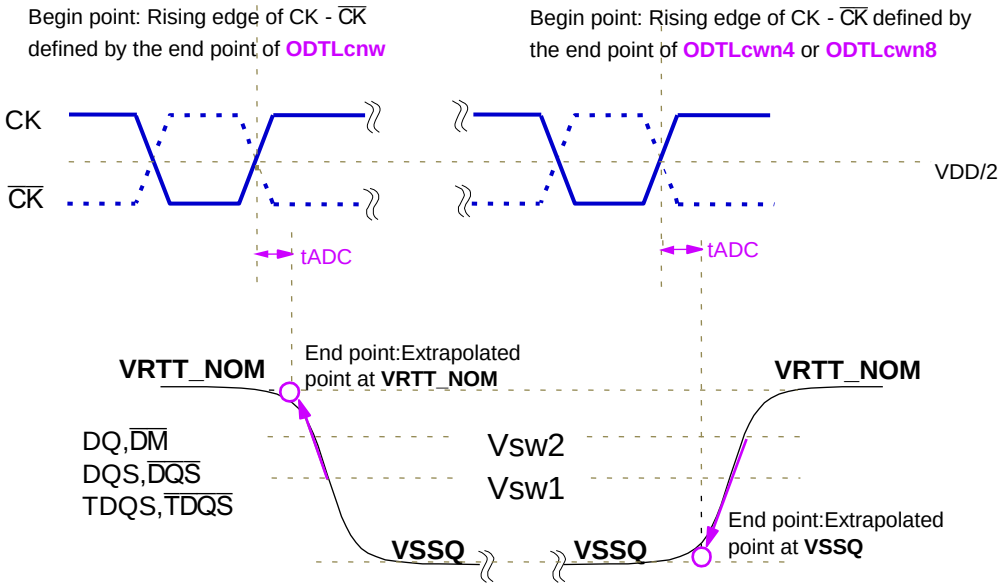
NOTE 2 ODT state change is controlled by ODT pin.

NOTE 3 ODT state change is controlled by Write Command.

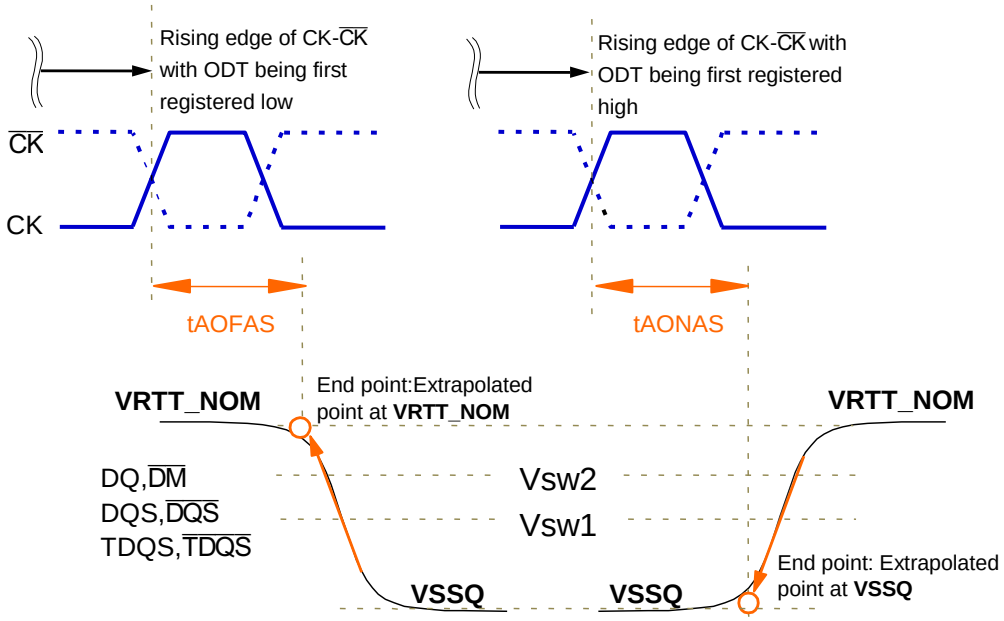
Definition of tADC at Direct ODT Control



Definition of tADC at Dynamic ODT Control



Definition of tAOFAS and tAONAS



Absolute Maximum DC Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Min	Max	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3	1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3	1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3	3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA relative to Vss	-0.3	1.5	V	1,3,5
T_{STG}	Storage Temperature	-55	100	°C	1,2

NOTE 1 Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

NOTE 2 Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51- 2 standard.

NOTE 3 VDD and VDDQ must be within 300 mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV

NOTE 4 VPP must be equal or greater than VDD/VDDQ at all times.

NOTE 5 Refer to overshoot area above 1.5 V is specified in Overshoot and Undershoot specifications section.

Absolute Maximum Ratings

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP		2.375	2.5	2.75	V	3

NOTE 1 Under all conditions VDDQ must be less than or equal to VDD.

NOTE 2 VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

NOTE 3 The DC bandwidth is limited to 20MHz

AC and DC Input Measurement Levels

AC & DC Logic input levels for single-ended signal

Single-ended AC & DC input levels for Command and Address

Symbol	Parameter	DDR4-1600/1866/2133/2400		DDR4-2666		Unit	NOTE
		Min.	Max.	Min.	Max.		
VIH.CA(DC75)	DC input logic high	V_{REFCA}+ 0.075	V_{DD}	-	-	V	
VIL.CA(DC75)	DC input logic low	V_{SS}	V_{REFCA} -0.075	-	-	V	
VIH.CA(DC65)	DC input logic high	-	-	V_{REFCA} + 0.065	V_{DD}	V	
VIL.CA(DC65)	DC input logic low	-	-	V_{SS}	V_{REFCA} - 0.065	V	
VIH.CA(AC100)	AC input logic high	V_{REF} + 0.1	Note 2	-	-	V	1
VIL.CA(AC100)	AC input logic low	Note 2	V_{REF} - 0.1	-	-	V	1
VIH.CA(AC90)	AC input logic high	-	-	V_{REF} + 0.09	Note 2	V	1
VIL.CA(AC90)	AC input logic low	-	-	Note 2	V_{REF} - 0.09	V	1
VREFCA(DC)	Reference Voltage for ADD, CMD inputs	0.49*V_{DD}	0.51*V_{DD}	0.49*V_{DD}	0.51*V_{DD}	V	2, 3

NOTE 1 See “Overshoot and Undershoot Specifications”.

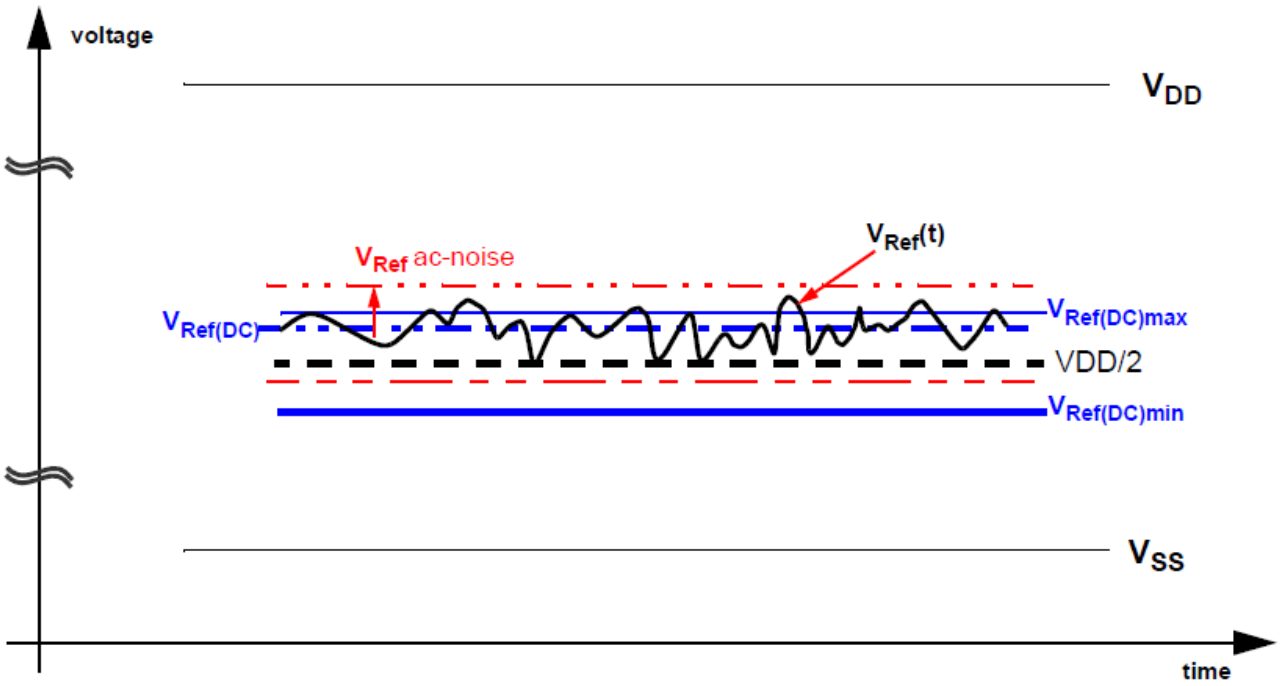
NOTE 2 The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1% VDD (for reference: approx. ± 12mV).

NOTE 3 For reference: approx. VDD/2 ± 12mV.

AC and DC Input Measurement Levels: V_{REF} Tolerances

The DC-tolerance limits and ac-noise limits for the reference voltages VREFCA is illustrated in Illustration of VREF(DC) tolerance and VREF AC-noise limits. It shows a valid reference voltage VREF(t) as a function of time. (VREF stands for VREFCA).

VREF(DC) is the linear average of VREF(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Single-ended AC & DC input levels for Command and Address. Furthermore, VREF(t) may temporarily deviate from VREF(DC) by no more than ± 1% VDD.



The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VREF. "VREF" shall be understood as VREF(DC), as defined in Illustration of V.

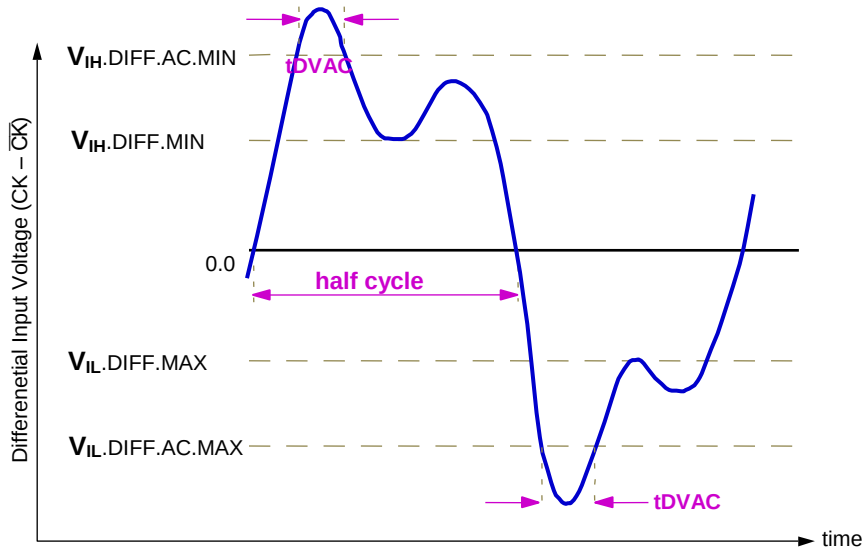
This clarifies, that DC-variations of VREF affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for VREF(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with VREF AC-noise. Timing and voltage effects due to AC-noise on VREF up to the specified limit (+/-1% of VDD) are included in DRAM timings and their associated deratings.

AC and DC Logic Input Levels for Differential Signals

Differential signal definition

Definition of differential ac-swing and "time above ac-level" tDVAC



NOTE 1 Differential signal rising edge from VIL_DIFF(MAX) to VIH_DIFF_AC(MIN) must be monotonic slope.

NOTE 2 Differential signal falling edge from VIH_DIFF(MIN) to VIL_DIFF_AC(MAX) must be monotonic slope.

Differential Input Swing Requirements for CK - $\overline{CK}$

Differential AC and DC Input Levels

Symbol	Parameter	DDR4 -1600/1866/2133		DDR4 -2400/2666		Unit	NOTE
		Min	Max	Min	Max		
VIH_{diff}	differential input high	150	NOTE 3	135	NOTE 3	mV	1
VIL_{diff}	differential input low	NOTE 3	-150	NOTE 3	-135	mV	1
$VIH_{diff(AC)}$	differential input high ac	2 x (VIH(AC) - VREF)	NOTE 3	2 x (VIH(AC) - VREF)	NOTE 3	V	2
$VIL_{diff(AC)}$	differential input low ac	NOTE 3	2 x (VIL(AC) - VREF)	NOTE 3	2 x (VIL(AC) - VREF)	V	2

NOTE 1 Used to define a differential signal slew-rate.

NOTE 2 For CK - $\overline{CK}$ use $VIH._{CA}$(AC) and $VIL._{CA}$ (AC) of ADD/CMD and VREFCA.

NOTE 3 These values are not defined; however, the differential signals (CK, $\overline{CK}$) need to be within the respective limits, $VIH._{CA}$ (DC) max and $VIL._{CA}$ (DC) min for single-ended signals as well as the limitations for overshoot and undershoot.

Allowed time before ringback (tDVAC) for CK - $\overline{CK}$

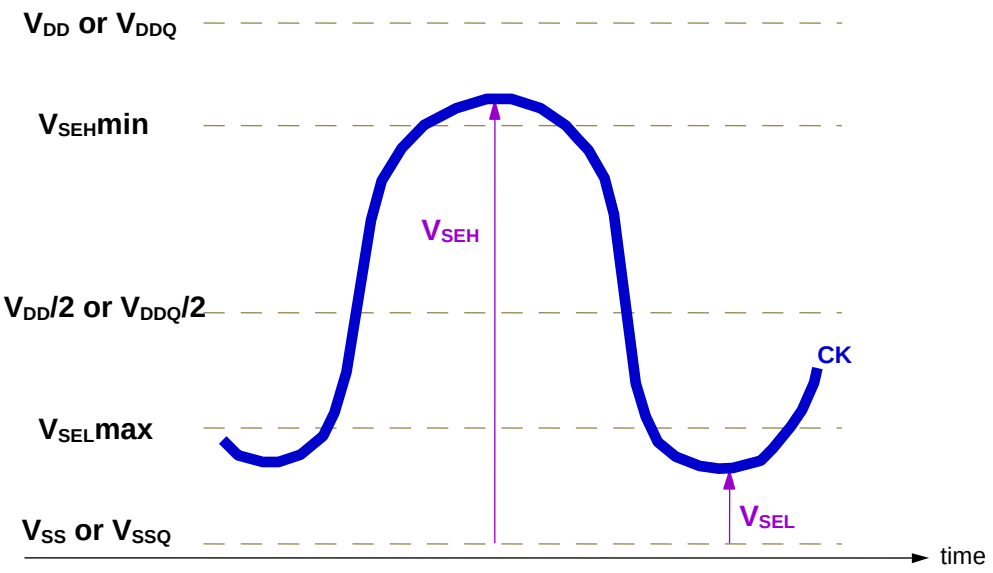
Slew Rate [V/ns]	tDVAC [ps] @ |VIH/Ldiff(AC)| = 200mV		tDVAC [ps] @ |VIH/Ldiff(AC)| = TBD mV	
	Min	Max	Min	Max
> 4.0	120	–	TBD	–
4.0	115	–	TBD	–
3.0	110	–	TBD	–
2.0	105	–	TBD	–
1.8	100	–	TBD	–
1.6	95	–	TBD	–
1.4	90	–	TBD	–
1.2	85	–	TBD	–
1.0	80	–	TBD	–
< 1.0	80	–	TBD	–

Single-ended requirements for CK differential signals

Each individual component of a differential signal (CK, $\overline{CK}$) has also to comply with certain requirements for single-ended signals. CK and $\overline{CK}$ have to reach approximately VSEHmin / VSELmax (approximately equal to the ac-levels V IH.CA (AC) and VIL.CA (AC) for ADD/CMD signals in every half-cycle. The applicable ac-levels for ADD/CMD might be different per speed-bin etc. e.g., if a value other than 100mV is used for ADD/CMD VIH.CA (AC) and VIL.CA (AC) signals, then these ac-levels apply also for the single-ended signals CK and $\overline{CK}$.

While ADD/CMD signal requirements are with respect to V_{REFCA}, the single-ended components of differential signals have a requirement with respect to V_{DD} / 2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Single-ended requirement for CK



Single-Ended levels for CK,$\overline{CK}$

Symbol	Parameter	DDR4-2133		DDR4-2400/2666		Unit	NOTE
		Min	Max	Min	Max		
V_{SEH}	Single-ended high-level for CK , $\overline{CK}$	(V_{DD}/2)+0.100	NOTE 3	(V_{DD}/2)+0.095	NOTE 3	V	1,2
V_{SEL}	Single-ended low-level for CK , $\overline{CK}$	NOTE 3	(VDD/2)-0.100	NOTE 3	(V_{DD}/2)-0.095	V	1,2

NOTE 1 For CK - $\overline{CK}$ use V IH.CA (AC) and VIL.CA (AC) of ADD/CMD.

NOTE 2 ADDR/CMD V IH.CA (AC) and VIL.CA (AC) based on VREFCA.

NOTE 3 These values are not defined; however, the differential signals (CK, $\overline{CK}$) need to be within the respective limits, V IH.CA (DC) max and VIL.CA (AC) min for single-ended signals as well as the limitations for overshoot and undershoot.

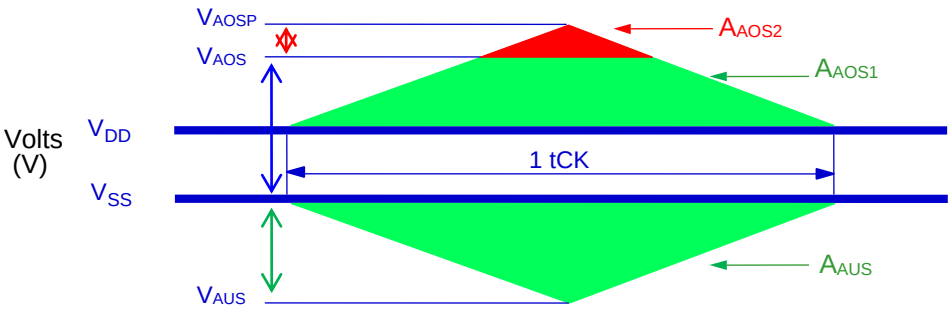
Address, Command, and Control Overshoot and Undershoot Specifications

AC overshoot/undershoot specification for Address, Command and Control pins

Symbol	Parameter	DDR4 Specification					Unit	Note
		1600/1866/2133/2400				2666		
V_{AOSP}	Maximum peak amplitude above VDD Absolute Max allowed for overshoot area	0.06				TBD	V	
V_{AOS}	Delta value between VDD Absolute Max and VDD Max allowed for overshoot area	VDD + 0.24				TBD	V	1
V_{AUS}	Maximum peak amplitude allowed for undershoot area	0.3				TBD	V	
A_{AOS2}	Maximum overshoot area per 1tCK Above Absolute Max	0.0083	0.0071	0.0062	0.0055	TBD	V/ns	
A_{AOS1}	Maximum overshoot area per 1tCK Between Absolute Max and VDD Max	0.2550	0.2185	0.1914	0.1699	TBD	V/ns	
A_{AUS}	Maximum undershoot area per 1tCK Below VSS	0.2644	0.2265	0.1984	0.1762	TBD	V/ns	
Address and control pins (A0-A13,A17,BG[1:0],BA[1:0],$\overline{ACT}$,$\overline{RAS}$/A16,$\overline{CAS}$/A15,$\overline{WE}$/A14,$\overline{CS}$,CKE,ODT)								

NOTE 1 The value of VAOS matches VDD absolute max as defined in “Absolute Maximum DC Ratings”. Absolute Maximum DC Ratings if VDD equals VDD max as defined in "ADDR, CMD, CNTL Overshoot and Undershoot Definition”. If VDD is above the recommended operating conditions, VAOS remains at VDD absolute max as defined in “Absolute Maximum DC Ratings”

Address, Command and Control Overshoot and Undershoot Definition



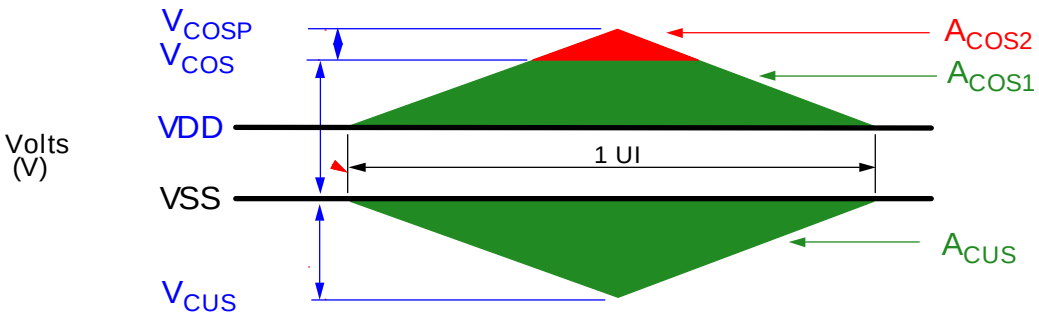
Clock Overshoot and Undershoot Specifications

AC overshoot/undershoot specification for Clock

Symbol	Parameter	DDR4 Specification					Unit	Note
		1600/1866/2133/2400				2666		
V_{COSP}	Maximum peak amplitude	0.06				TBD	V	
V_{COS}	above VCOS	VDD + 0.24				TBD	V	1
V_{CUS}	Upper boundary of overshoot area ADOS1	0.3				TBD	V	
A_{COS2}	Maximum peak amplitude allowed for undershoot	0.0038	0.0032	0.0028	0.0025	TBD	V/ns	
A_{COS1}	Maximum overshoot area	0.1125	0.0964	0.0844	0.0750	TBD	V/ns	
A_{CUS}	per 1 UI above VCOS	0.1144	0.0980	0.0858	0.0762	TBD	V/ns	
CK,$\overline{CK}$								

NOTE 1 The value of VCOS matches VDD absolute max as defined in Absolute Maximum DC Ratings Absolute Maximum DC Ratings if VDD equals VDD max as defined in Recommended DC Operating Conditions. If VDD is above the recommended operating conditions, VCOS remains at VDD absolute max as defined in Absolute Maximum DC Ratings.

CK Overshoot and Undershoot Definition



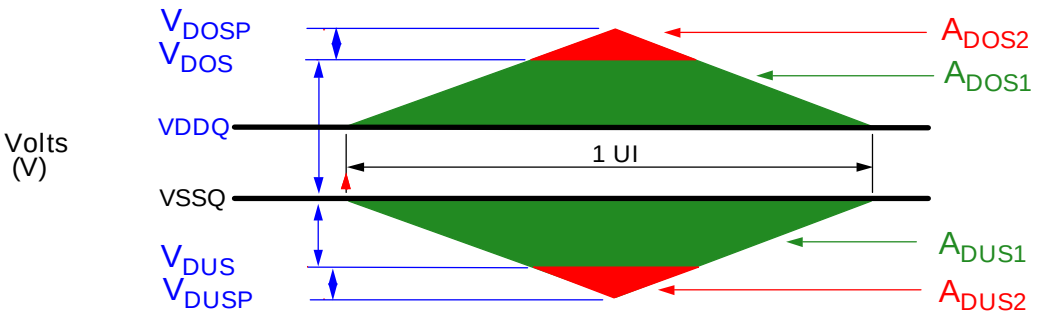
Data, Strobe, and Mask Overshoot and Undershoot Specifications

AC overshoot/undershoot specification for Data, Strobe and Mask

Symbol	Parameter	DDR4 1600	DDR4 1866	DDR4 2133	DDR4 2400	DDR4 2666	Unit	Note
V_{DOSP}	Maximum peak amplitude above VDOS	0.16				TBD	V	
V_{DOS}	Upper boundary of overshoot area ADOS1	VDD + 0.24				TBD	V	1
V_{DUS}	Lower boundary of undershoot area ADUS1	0.30				TBD	V	2
V_{DUSP}	Maximum peak amplitude below VDUS	0.10				TBD	V	
A_{DOS2}	Maximum overshoot area	0.0150	0.0129	0.0113	0.0100	TBD	V/ns	
A_{DOS1}	per 1 UI above VDOS	0.1050	0.0900	0.0788	0.0700	TBD	V/ns	
A_{DUS1}	Maximum overshoot area per	0.1050	0.0900	0.0788	0.0700	TBD	V/ns	
A_{DUS2}	1 UI between VDDQ and VDOS	0.0150	0.0129	0.0113	0.0100	TBD	V/ns	
	Data, Strobe and Mask (DQ, DQS, $\overline{DQS}$, $\overline{DM}$, $\overline{DBI}$, TDQS, $\overline{TDQS}$)							

NOTE 1 The value of VDOS matches (VIN, VOUT) max as defined in Absolute Maximum DC Ratings Absolute Maximum DC Ratings if VDDQ equals VDDQ max as defined in

Data, Strobe, and Mask Overshoot and Undershoot Definition



Slew Rate Definitions

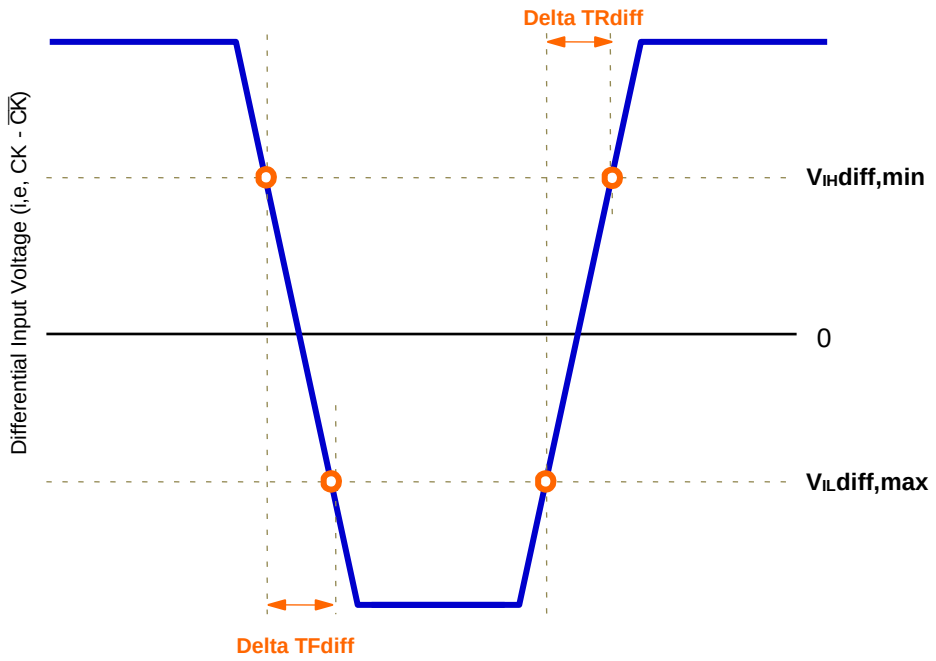
Slew Rate Definitions for CK Differential Input Signals

CK Differential Input Slew Rate Definition

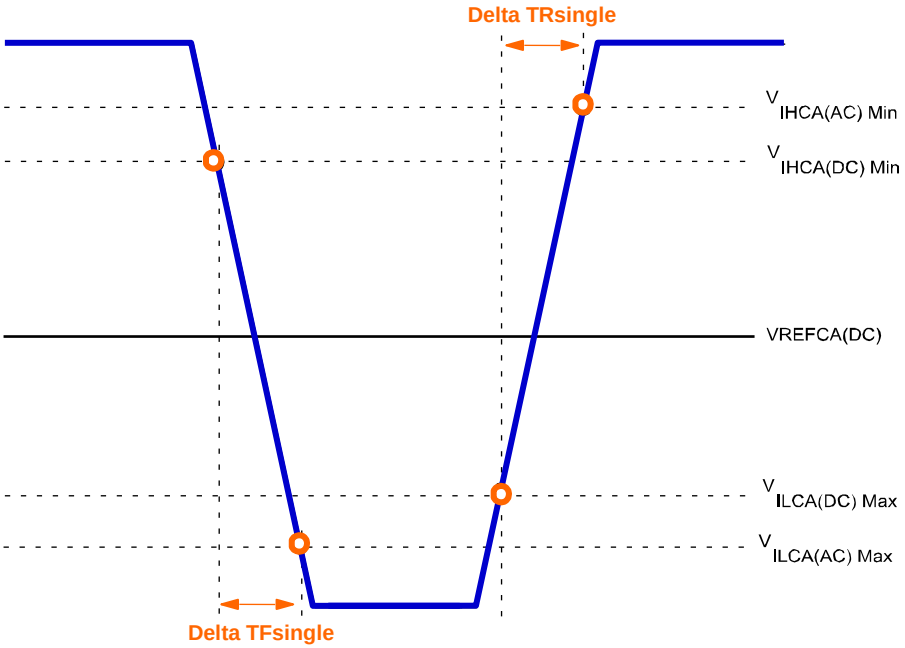
Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge(CK - $\overline{CK}$)	**$V_{IL,diff,max}$**	**$V_{IH,diff,min}$**	[$V_{IH,diff,min} - V_{IL,diff,max}$] /ΔTRdiff
Differential input slew rate for falling edge(CK - $\overline{CK}$)	**$V_{IH,diff,min}$**	**$V_{IL,diff,max}$**	[$V_{IH,diff,min} - V_{IL,diff,max}$] /ΔTFdiff

NOTE 1 The differential signal CK - $\overline{CK}$ must be monotonic between these thresholds.

Differential Input Slew Rate Definition for CK, $\overline{CK}$



Slew Rate Definition for Single-ended Input Signals (CMD/ADD)



NOTE1 Single-ended input slew rate for rising edge = {VIHCA(AC)Min - VILCA(DC)Max} / Delta TR single

NOTE2 Single-ended input slew rate for falling edge = {VIHCA(DC)Min - VILCA(AC)Max} / Delta TF single

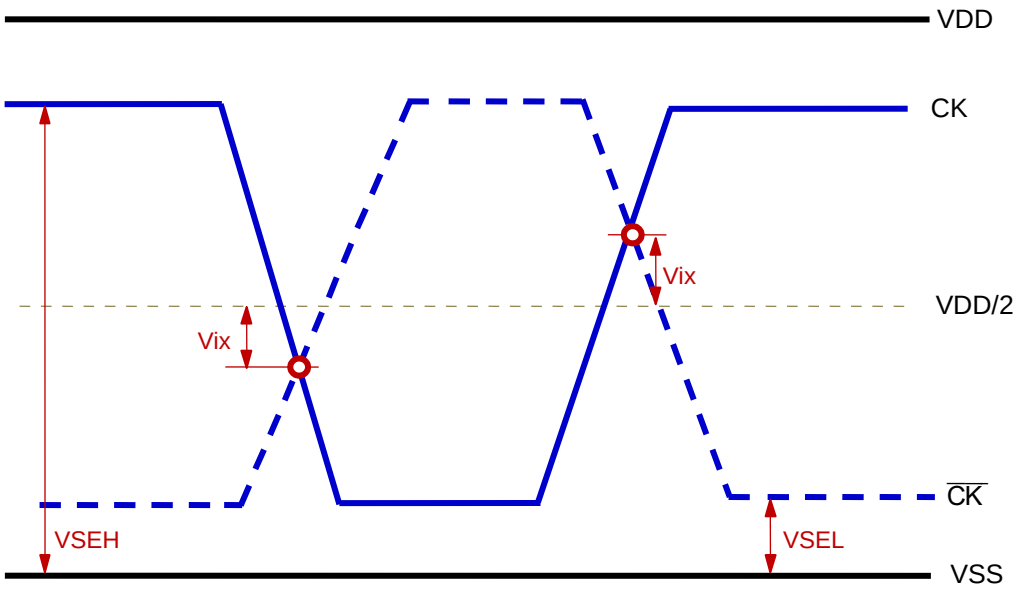
NOTE3 Single-ended signal rising edge from VILCA(DC)Max to VIHCA(DC)Min must be monotonic slope.

NOTE4 Single-ended signal falling edge from VIHCA(DC)Min to VILCA(DC)Max must be monotonic slope.

Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signal CK, $\overline{CK}$ must meet the requirements in Cross point voltage for differential input signals (CK) shown below. The differential input cross point voltage $V_{IX(CK)}$ is measured from the actual cross point of true and complement signals to the midlevel between V_{DD} and V_{SS}.

VIX(CK) Definition



Cross Point Voltage for CK Differential Input Signals

Symbol	Parameter	DDR4-1600/1866/2133/2400			
		Min		Max	
–	Area of VSEH, VSEL	VSEL< VDD/2 - 145 mV	VDD/2 - 145 mV ≦VSEL≦ VDD/2 - 100 mV	VDD/2 + 100 mV ≦VSEH≦ VDD/2 + 145 mV	VDD/2 + 145 mV <VSEH
$V_{IX(CK)}$	Differential Input Cross Point Voltage relative to VDD/2 for CK, $\overline{CK}$	-120 mV	- (VDD/2 - VSEL) + 25 mV	(VSEH - VDD/2) - 25 mV	120 mV

Symbol	Parameter	DDR4-2666			
		Min		Max	
–	Area of VSEH, VSEL	VSEL< VDD/2 - 145 mV	VDD/2 - 145 mV ≦VSEL≦ VDD/2 - 100 mV	VDD/2 + 100 mV ≦VSEH≦ VDD/2 + 145 mV	VDD/2 + 145 mV <VSEH
$V_{IX(CK)}$	Differential Input Cross Point Voltage relative to VDD/2 for CK, $\overline{CK}$	-110 mV	- (VDD/2 - VSEL) + 30 mV	(VSEH - VDD/2) - 30 mV	110 mV

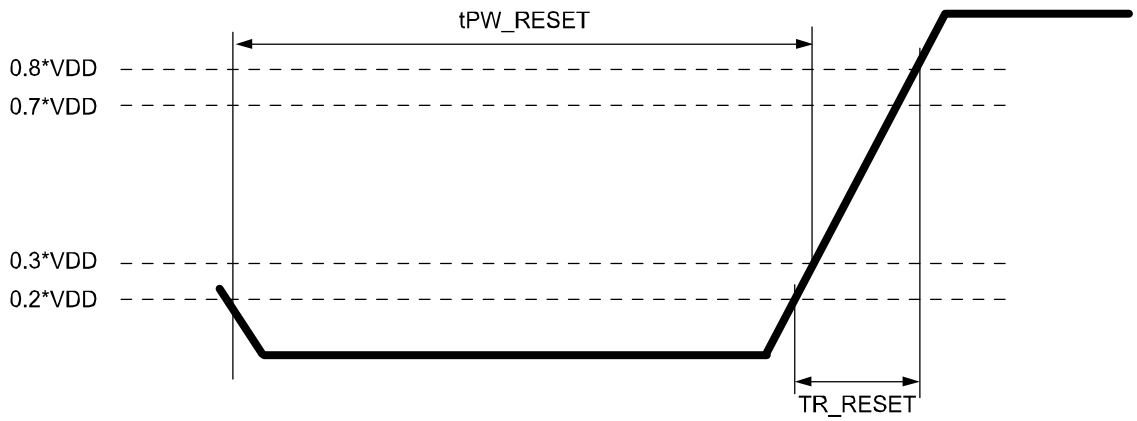
CMOS rail to rail Input Levels

CMOS rail to rail Input Levels for $\overline{\text{RESET}}$

Symbol	Parameter	Min	Max	Unit	NOTE
VIH(AC)_RESET	AC Input High Voltage	0.8*VDD	VDD	V	6
VIH(DC)_RESET	DC Input High Voltage	0.7*VDD	VDD	V	2
VIL(DC)_RESET	DC Input Low Voltage	VSS	0.3*VDD	V	1
VIL(AC)_RESET	AC Input Low Voltage	VSS	0.2*VDD	V	7
TR_RESET	Rising time	-	1.0	us	4
tPW_RESET	RESET pulse width	1.0	-	us	3,5

NOTE1 After $\overline{\text{RESET}}$ is registered LOW, $\overline{\text{RESET}}$ level shall be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, SDRAM may not be reset.
NOTE2 Once RESET is registered HIGH, RESET level must be maintained above VIH(DC)_RESET, otherwise, SDRAM operation will not be guaranteed until it is reset asserting $\overline{\text{RESET}}$ signal LOW.
NOTE3 RESET is destructive to data contents.
NOTE4 No slope reversal(ringback) requirement during its level transition from Low to High.
NOTE5 This definition is applied only “Reset Procedure at Power Stable”.
NOTE6 Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
NOTE7 Undershoot might occur. It should be limited by Absolute Maximum DC Ratings

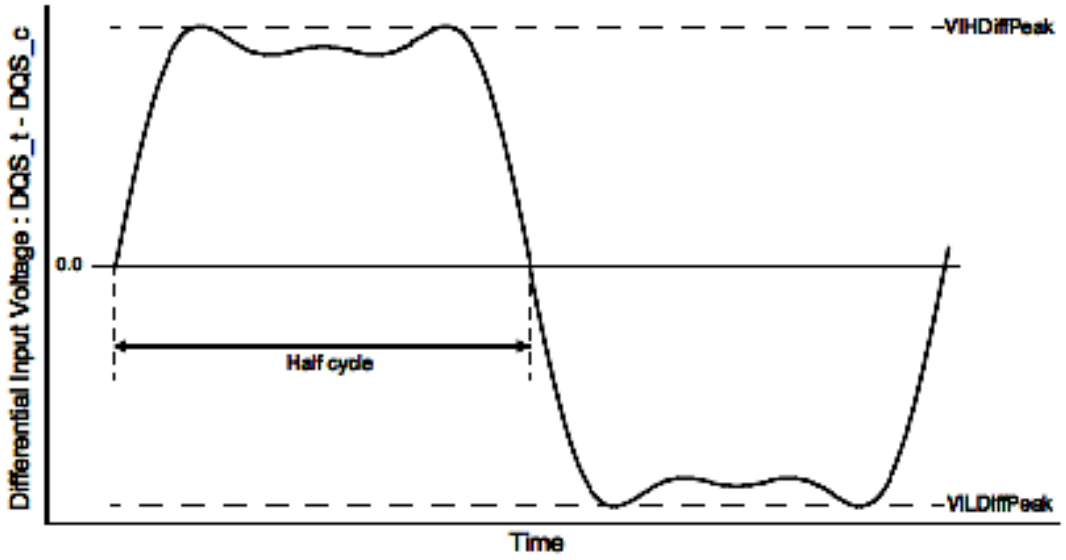
$\overline{\text{RESET}}$ Input Slew Rate Definition



AC and DC Logic Input Levels for DQS Signals

Differential signal definition

Definition of differential DQS Signal AC-swing Level



Differential swing requirements for DQS (DQS - $\overline{DQS}$)

Differential AC and DC Input Levels for DQS

Symbol	Parameter	DDR4-1600, 1866, 2133		DDR4-2400		DDR4-2666		Unit	Note
		Min	Max	Min	Max	Min	Max		
VIHDiffPeak	VIH.DIFF.Peak Voltage	186	Note2	160	Note2	150	Note2	mV	1
VILDiffPeak	VIL.DIFF.Peak Voltage	Note2	-186	Note2	-160	Note2	150	mV	1

NOTE1 Used to define a differential signal slew-rate.
NOTE2 These values are not defined; however, the differential signals DQS - $\overline{DQS}$, need to be within the respective limits Overshoot, Undershoot Specification for single-ended signals.

Peak voltage calculation method

The peak voltage of Differential DQS signals are calculated in a following equation.

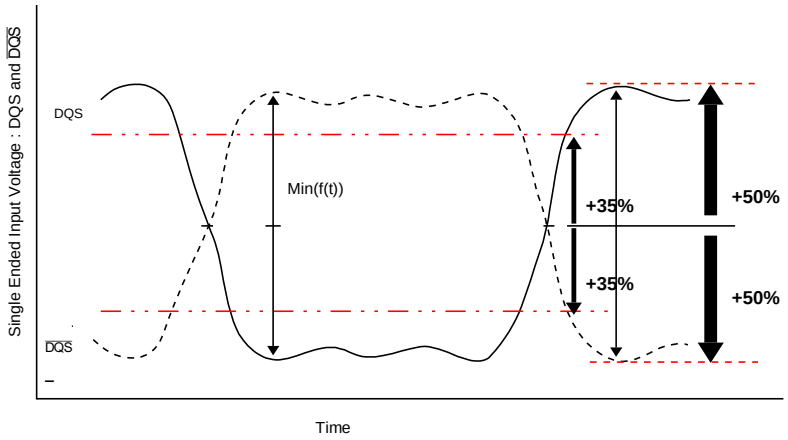
VIH.DIFF.Peak Voltage = Max(f(t))

VIL.DIFF.Peak Voltage = Min(f(t))

f(t) = VDQS - $\overline{VDQS}$

The Max(f(t)) or Min(f(t)) used to determine the midpoint which to reference the +/-35% window of the exempt non-monotonic signaling shall be the smallest peak voltage observed in all ui's.

Definition of differential DQS Peak Voltage and rage of exempt non-monotonic signaling



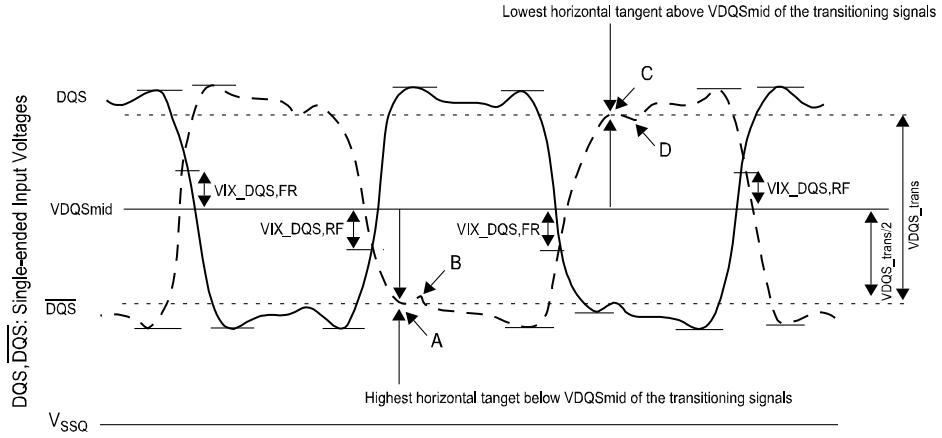
Differential Input Cross Point Voltage

To achieve tight RxMask input requirements as well as output skew parameters with respect to strobe, the cross point voltage of differential input signals (DQS, $\overline{DQS}$) must meet the requirements in Cross point voltage for DQS differential input signals. The differential input cross point voltage VIX_DQS (VIX_DQS_FR and VIX_DQS_RF) is measured from the actual cross point of DQS, $\overline{DQS}$ relative to the VDQSmid of the DQS and $\overline{DQS}$ signals.

VDQSmid is the midpoint of the minimum levels achieved by the transitioning DQS and $\overline{DQS}$ signals, and noted by VDQSrans. VDQSrans is the difference between the lowest horizontal tangent above VDQSmid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.

A non-monotonic transitioning signal's ledge is exempt or not used in determination of a horizontal tangent provided the said ledge occurs within +/- 35% of the midpoint of either VIH.DIFF.Peak Voltage (DQS rising) or VIL.DIFF.Peak Voltage ($\overline{DQS}$ rising), refer to Definition of differential DQS Peak Voltage and rage of exempt non-monotonic signal. A secondary horizontal tangent resulting from a ring-back transition is also exempt in determination of a horizontal tangent. That is, a falling transition's horizontal tangent is derived from its negative slope to zero slope transition (point A in Vix Definition (DQS)) and a ring-back's horizontal tangent derived from its positive slope to zero slope transition (point B in Vix Definition (DQS)) is not a valid horizontal tangent; and a rising transition's horizontal tangent is derived from its positive slope to zero slope transition (point C in Vix Definition (DQS)) and a ring-back's horizontal tangent derived from its negative slope to zero slope transition (point D in Vix Definition (DQS)) is not a valid horizontal tangent.

VIX(DQS) Definition



Cross Point Voltage for Differential Input Signals DQS

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2666		Unit	NOTE
		Min.	Max.	Min.	Max.		
Vix_DQS_ratio	DQS Differential input cross point voltage ratio	–	25	–	25	%	1,2
VDQSmid_to_Vcent	VDQSmid offset relative to Vcent_DQ(midpoint)	-	min(VIHdiff,50)	-	min(VIHdiff,50)	mV	3, 4, 5

NOTE 1 Vix_DQS_Ratio is DQS VIX crossing (Vix_DQS_FR or Vix_DQS_RF) divided by VDQSrans. VDQSrans is the difference between the lowest horizontal tangent above VDQSmid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.

NOTE 2 VDQSmid will be similar to the VREFDQ internal setting value obtained during Vref Training if the DQS and DQs drivers and paths are matched.

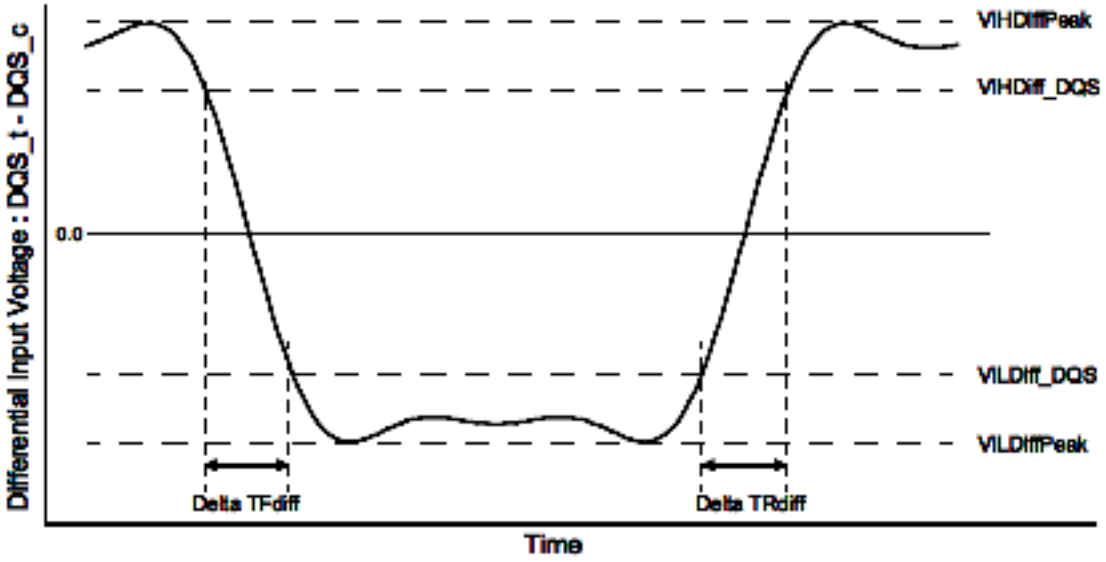
NOTE 3 The maximum limit shall not exceed the smaller of VIHdiff minimum limit or 50mV.

NOTE 4 VIX measurements are only applicable for transitioning DQS and $\overline{DQS}$ signals when toggling data, preamble and high-z states are not applicable conditions.

NOTE 5 The parameter VDQSmid is defined for simulation and ATE testing purposes, it is not expected to be tested in a system.

Differential Input Slew Rate Definition

Differential Input Slew Rate and Input Level Definition for DQS - $\overline{DQS}$



NOTE 1 Differential signal rising edge from VILDiff_DQS to VIHDiff_DQS must be monotonic slope.
NOTE 2 Differential signal falling edge from VIHDiff_DQS to VILDiff_DQS must be monotonic slope.

Differential Input Slew Rate Definition for DQS,$\overline{DQS}$

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge(DQS - $\overline{DQS}$)	VIL_{Diff_DQS}	VIH_{Diff_DQS}	$\lvert VIL_{Diff\_DQS} - VIH_{Diff\_DQS} \rvert$ / ΔTRdiff
Differential input slew rate for falling edge(DQS - $\overline{DQS}$)	VIH_{Diff_DQS}	VIL_{Diff_DQS}	$\lvert VIL_{Diff\_DQS} - VIH_{Diff\_DQS} \rvert$ / ΔTFdiff

NOTE 1 The differential signal DQS - $\overline{DQS}$ must be monotonic between these thresholds.

Differential Input Slew Rate and Input Levels for DQS - $\overline{DQS}$

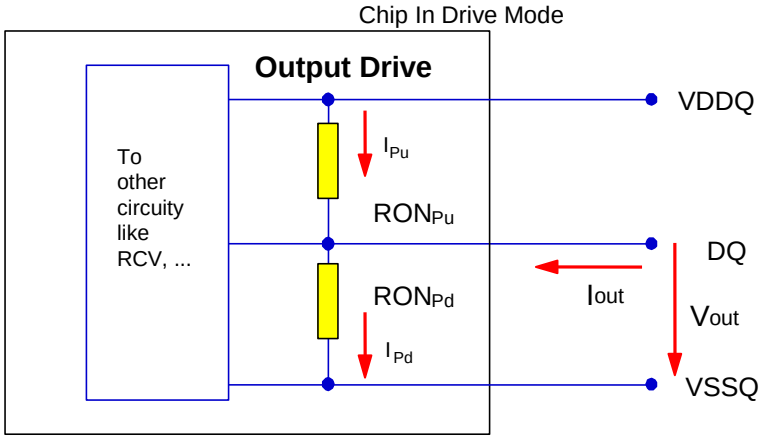
Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400		DDR4-2666		Unit
		Min	Max	Min	Max	Min	Max	
VIH_{Diff_DQS}	Differential Input High	136	-	130	-	130	-	mV
VIL_{Diff_DQS}	Differential Input Low	-	-136	-	-130	-	-130	mV
SR_{Idiff}	Differential Input Slew Rate	3	18	3	18	2.5	18	V/ns

AC and DC Output Measuremnt Levels

Output Driver DC Electrical Characteristics

The DDR4 driver supports two different Ron values. These Ron values are referred as strong (low Ron) and weak mode (high Ron). A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

Output driver



The individual pull-up and pull-down resistors (RONPu and RONPd) are defined as follows:

$$RON_{Pu} = \frac{VDDQ - Vout}{|\,Iout\,|}$$ under the condition that RON_{Pd} is off

$$RON_{Pd} = \frac{Vout}{|\,Iout\,|}$$ under the condition that RON_{Pu} is off

Output Driver DC Electrical Characteristics, assuming RZQ = 240ohm; entire operating temperature range; after proper ZQ calibration

RTT_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	NOTE
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.73	1	1.1	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.83	1	1.1	RZQ/7	1,2
		VOHdc= 1.1* VDDQ	0.83	1	1.25	RZQ/7	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/7	1,2
48	RON48Pd	VOLdc= 0.5*VDDQ	0.73	1	1.1	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.83	1	1.1	RZQ/5	1,2
		VOHdc= 1.1* VDDQ	0.83	1	1.25	RZQ/5	1,2
	RON48Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/5	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc = 0.8* VDDQ	-10	-	17	%	1,2,3,4
Mismatch DQ-DQ within byte variation pull-up, MMPudd		VOMdc= 0.8* VDDQ	-	-	10	%	1,2,4
Mismatch DQ-DQ within byte variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ	-	-	10	%	1,2,4

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity(TBD).

NOTE 2 Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 1.1 * VDDQ.

NOTE3 Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately; Ronnom is the nominal Ron value

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} * 100$$

NOTE 4 RON variance range ratio to RON Nominal value in a given component, including DQS and DQS.

$$MMPudd = \frac{RONPuMax - RONPuMin}{RONNOM} * 100$$

$$MMPddd = \frac{RONPdMax - RONPdMin}{RONNOM} * 100$$

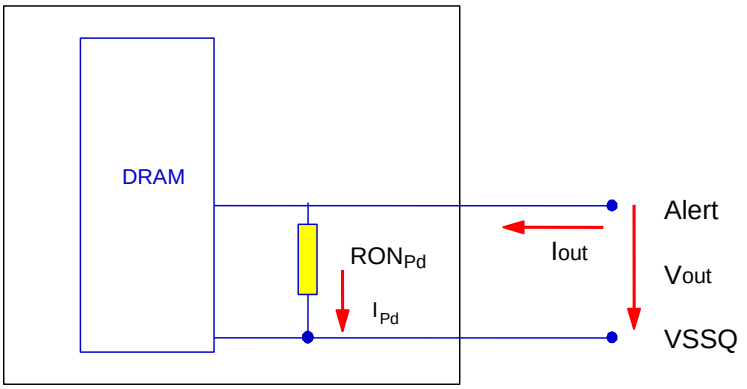
NOTE 5 This parameter of x16 device is specified for Upper byte and Lower byte.

$\overline{\text{ALERT}}$ Output Drive Characteristic

Output driver impedance RON is defined as follows:

$$RON_{Pd} = \frac{Vout}{|\ Iout\ |} \quad \text{under the condition that } RON_{Pu} \text{ is off}$$

Alert Driver



Resistor	Vout	Min	Max	Unit	NOTE
RONPd	VOLdc= 0.1* VDDQ	0.3	1.2	34Ω	1
	VOMdc = 0.8* VDDQ	0.4	1.2	34Ω	1
	VOHdc = 1.1* VDDQ	0.4	1.4	34Ω	1

NOTE 1 VDDQ voltage is at VDDQ DC. VDDQ DC definition is TBD.

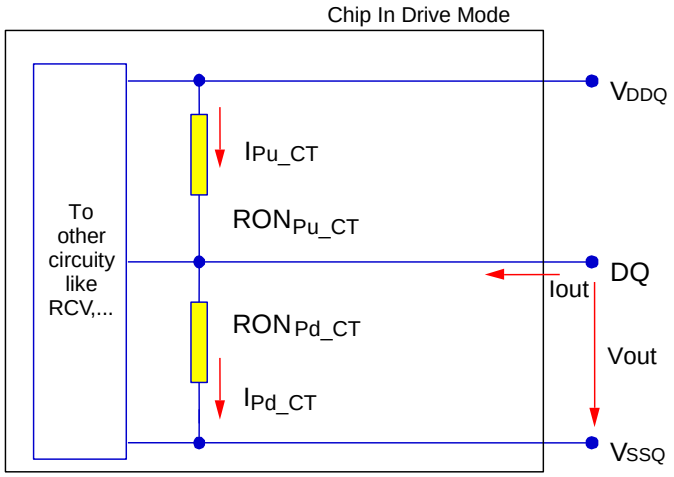
Output Driver Characteristic of Connectivity Test (CT) Mode

Following Output driver impedance RON will be applied Test Output Pin during Connectivity Test (CT) Mode.

The individual pull-up and pull-down resistors (RONPu_CT and RONPd_CT) are defined as follows:

$$RON_{Pu\_CT} = \frac{V_{DDQ} - V_{OUT}}{|I_{out}|} \qquad RON_{Pd\_CT} = \frac{V_{OUT}}{|I_{out}|}$$

Output Driver



RON$_{NOM_CT}$	Resistor	Vout	Max	Units	NOTE
34Ω	RON$_{Pd_CT}$	VOB$_{dc}$ = 0.2 x V$_{DDQ}$	1.9	34Ω	1
		VOL$_{dc}$ = 0.5 x V$_{DDQ}$	2.0	34Ω	1
		VOM$_{dc}$ = 0.8 x V$_{DDQ}$	2.2	34Ω	1
		VOH$_{dc}$ = 1.1 x V$_{DDQ}$	2.5	34Ω	1
	RON$_{Pu_CT}$	VOB$_{dc}$ = 0.2 x V$_{DDQ}$	2.5	34Ω	1
		VOL$_{dc}$ = 0.5 x V$_{DDQ}$	2.2	34Ω	1
		VOM$_{dc}$ = 0.8 x V$_{DDQ}$	2.0	34Ω	1
		VOH$_{dc}$ = 1.1 x V$_{DDQ}$	1.9	34Ω	1

NOTE 1 Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined.

Single-Ended AC & DC Output Levels

Single-ended AC & DC output levels

Symbol	Parameter		DDR4-1600/1866/2133/2400/2666	Units	NOTE
$V_{OH(DC)}$	DC output high measurement level	For IV curve linearity	1.1 x VDDQ	V	
$V_{OM(DC)}$	DC output mid measurement level		0.8 x VDDQ	V	
$V_{OL(DC)}$	DC output low measurement level		0.5 x VDDQ	V	
$V_{OH(AC)}$	AC output high measurement level	For output SR	(0.7 + 0.15) x VDDQ	V	1
$V_{OL(AC)}$	AC output low measurement level		(0.7 - 0.15) x VDDQ	V	1

NOTE 1 The swing of ± 0.15 × VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7 and an effective test load of 50Ω to VTT = VDDQ.

Differential AC & DC Output Levels

Differential AC & DC output levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666	Units	NOTE
VOHdiff(AC)	AC differential output high measurement level (for output SR)	+0.3 x VDDQ	V	1
VOLdiff(AC)	AC differential output low measurement level (for output SR)	-0.3 x VDDQ	V	1

NOTE 1 The swing of ± 0.3 × VDDQ is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to VTT = VDDQ at each of the differential outputs.

Single-ended Output Slew Rate

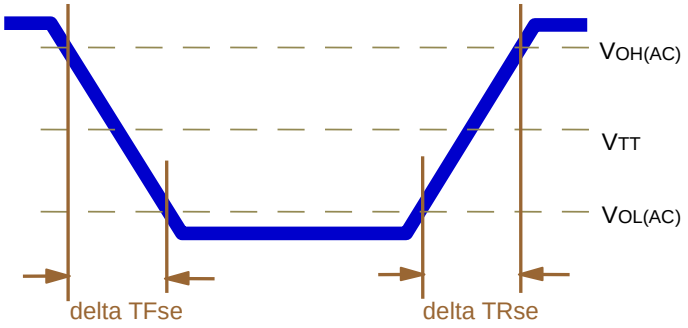
Using the same reference load used for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals.

Single-Ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single ended output slew rate for rising edge	**$V_{OL(AC)}$**	**$V_{OH(AC)}$**	[$V_{OH(AC)}$-$V_{OL(AC)}$] / ΔTRse
Single ended output slew rate for falling edge	**$V_{OH(AC)}$**	**$V_{OL(AC)}$**	[$V_{OH(AC)}$-$V_{OL(AC)}$] / ΔTFse

NOTE 1 Output slew rate is verified by design and characterization, and may not be subject to production test.

Single-ended Output Slew Rate Definition



Single-Ended Output Slew Rate

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666		Unit
		Min	Max	
SRQse	Single ended output slew rate	4	9	V/ns

For RON = RZQ/7
SR = slew rate; Q = query output; se = single-ended signals
NOTE 1 In two cases a maximum slew rate of 12V/ns applies for a single DQ signal within a byte lane.

- Case 1 is defined for a single DQ signal within a byte lane that is switching into a certain direction (either from high-to-low or low-to-high) while all remaining DQ signals in the same byte lane are static (they stay at either high or low).
- Case 2 is defined for a single DQ signal within a byte lane that is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies.

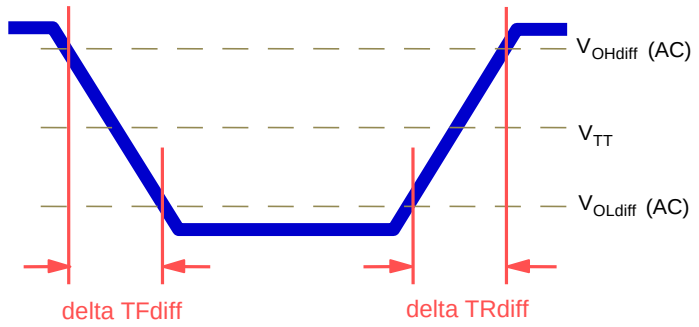
Differential Output Slew Rate

Differential output slew rate definition

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	**$VOL_{diff(AC)}$**	**$VOH_{diff(AC)}$**	$[VOH_{,diff(AC)}-VOL_{,diff(AC)}] / \Delta TRdiff$
Differential output slew rate for falling edge	**$VOH_{diff(AC)}$**	**$VOL_{diff(AC)}$**	$[VOH_{,diff(AC)}-VOL_{,diff(AC)}] / \Delta TFdiff$

NOTE 1 Output slew rate is verified by design and characterization, and may not be subject to production test.

Differential Output Slew Rate Definition



Differential Output Slew Rate

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666		Unit
		Min	Max	
SRQdiff	Differential output slew rate	8	18	V/ns

For RON = RZQ/7

SR = slew rate; Q = query output; diff: Differential Signals

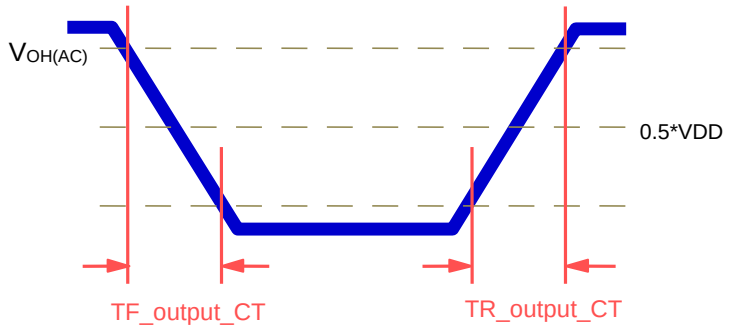
Single-ended AC & DC output levels of Connectivity Test Mode

Single-ended AC & DC output levels of Connectivity Test Mode

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	1.1 x VDDQ	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.8 x VDDQ	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.5 x VDDQ	V	
$V_{OB(DC)}$	DC output below measurement level (for IV curve linearity)	0.2 x VDDQ	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	VTT + (0.1 x VDDQ)	V	1
$V_{OL(AC)}$	AC output below measurement level (for output SR)	VTT - (0.1 x VDDQ)	V	1

NOTE 1 The effective test load is 50Ω terminated by VTT = 0.5 * VDDQ.

Output Slew Rate Definition of Connectivity Test Mode

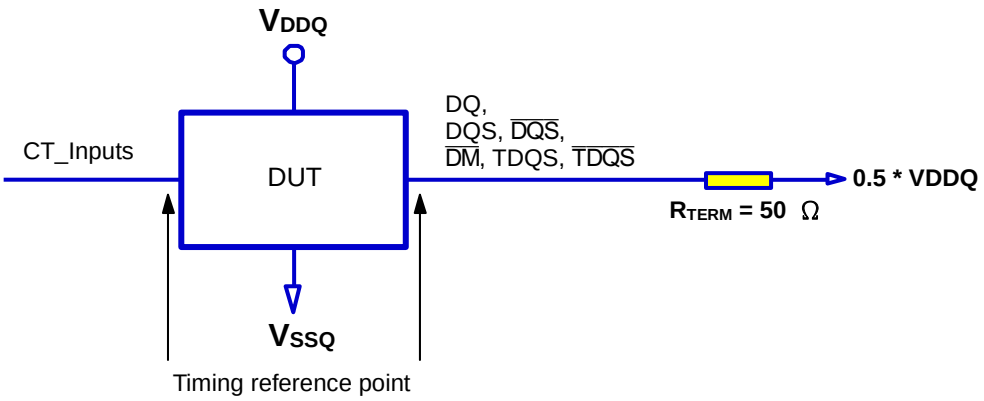


Single-ended output slew rate of Connectivity Test Mode

Symbol	Parameter	DDR4-1600/1866/2133/ 2400/2666		Unit
		Min	Max	
TF_output_CT	Output signal Falling time	-	10	ns/V
TR_output_CT	Output signal Rising time	-	10	ns/V

Test Load for Connectivity Test Mode Timing

Connectivity Test Mode Timing Reference Load



Speed Bin

DDR4-2666 Speed Bin

Speed Bin				DDR4-2666		Unit	Notes
CL-nRCD-nRP				19			
Parameter			Symbol	Min	Max		
Internal read command to first data			tAA	14.25[14]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	12
ACT to internal read or write delay time			tRCD	14.25	-	ns	12
PRE command period			tRP	14.25	-	ns	12
ACT to PRE command period			tRAS	32	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	46.25	-	ns	12
	Normal	Read DBI					
CWL= 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	4
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,11
CWL= 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,9
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,9
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,9
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,9
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,9
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,9
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	4
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,9
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	4
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3
Supported CL Settings				10, 11, 12,13,14,15,16,17,18,19,20		nCK	16
Supported CL Settings with read DBI				12,13, 14,15,17,18,19,20,21,22,23		nCK	16
Supported CWL Settings				9,10,11,12,14, 16,18		nCK	16

Speed Bin Table Note

Absolute Specification

- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-1600,1866,2133 and 2400 Speed Bin Tables are valid only when Geardown Mode is disabled.

NOTE 1 The CL setting and CWL setting result in tCK(avg). MIN and tCK(avg). MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.

NOTE 2 tCK(avg). MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from tAA following rounding algorithm defined in Section 13.5.

NOTE 3 tCK(avg). MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.937 ns or 0.833 ns). This result is tCK(avg). MAX corresponding to CL SELECTED.

NOTE 4 'Reserved' settings are not allowed. User must program a different value.

NOTE 5 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.

NOTE 6 Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but has been verified.

NOTE 7 Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but has been verified.

NOTE 8 Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but has been verified.

NOTE 9 Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but has been verified.

NOTE 10 Any DDR4-3200 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but has been verified.

NOTE 11 DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.

NOTE 12 Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.

NOTE 13 CL number in parentheses, it means that these numbers are optional.

NOTE 14 DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).

NOTE 15 Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.

NOTE 16 Supporting CL setting herewith is a reference base on JEDEC's. Precise CL & tCK setting needs to follow where defined on speed compatible table in section "Operating frequency", exceptional setting please confirm with NTC.CWL setting follow CL value in above table in section "Speed Bin"

IDD and IDDQ Specification Parameters and Test conditions

I_{DD}, I_{PP} and I_{DDQ} Measurement Conditions

In this chapter, I_{DD}, I_{PP} and I_{DDQ} measurement conditions such as test load and patterns are defined and setup and test load for I_{DD}, I_{PP} and I_{DDQ} measurements are also described here.

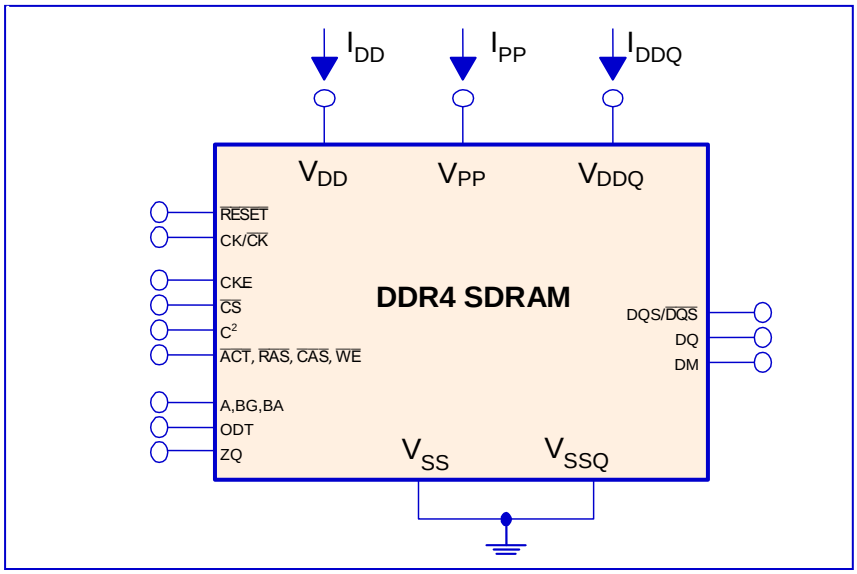
- I_{DD} currents (such as I_{DD0}, I_{DD0A}, $I_{DD}1$, I_{DD1A}, I_{DD2N}, I_{DD2NA}, I_{DD2NL}, I_{DD2NT}, I_{DD2P}, I_{DD2Q}, I_{DD3N}, I_{DD3NA}, I_{DD3P}, I_{DD4R}, I_{DD4RA}, I_{DD4W}, I_{DD4WA}, I_{DD5B}, I_{DD5F2}, I_{DD5F4}, I_{DD6N}, I_{DD6E}, I_{DD6R}, I_{DD6A}, I_{DD7} and I_{DD8}) are measured as time-averaged currents with all V_{DD} balls of the DDR4 SDRAM under test tied together. Any I_{PP} or I_{DDQ} current is not included in I_{DD} currents.
- I_{PP} currents have the same definition as I_{DD} except that the current on the V_{PP} supply is measured.
- I_{DDQ} currents (such as I_{DDQ2NT} and I_{DDQ4R}) are measured as time-averaged currents with all V_{DDQ} balls of the DDR4 SDRAM under test tied together. Any I_{DD} current is not included in I_{DDQ} currents.

  Attention: I_{DDQ} values cannot be directly used to calculate IO power of the DDR4 SDRAM. They can be used to support correlation of simulated IO power to actual IO power. In DRAM module application, I_{DDQ} cannot be measured separately since V_{DD} and V_{DDQ} are using one merged-power layer in Module PCB.

For I_{DD}, I_{PP} and I_{DDQ} measurements, the following definitions apply:

- "0" and "LOW" is defined as $V_{IN} <= V_{ILAC(max)}$.
- "1" and "HIGH" is defined as $V_{IN} >= V_{IHAC(min)}$.
- "MID-LEVEL" is defined as inputs are $V_{REF} = V_{DD} / 2$.
- Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns are described Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns.
- Basic I_{DD}, I_{PP} and I_{DDQ} Measurement Conditions are described in: Basic IDD, IPP and IDDQ Measurement Conditions.
- Detailed I_{DD}, I_{PP} and I_{DDQ} are described in table: IDD0, IDD0A and IPP0 Measurement-Loop Pattern through IDD7 Measurement-Loop Pattern.
- IDD Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting
  - $R_{ON} = R_{ZQ}/7$ (34 Ω in MR1);
  - $R_{TT\_NOM} = R_{ZQ/6}$ (40 Ω in MR1);
  - $R_{TT\_WR} = R_{ZQ/2}$ (120 Ω in MR2);
  - R_{TT_PARK} = Disable;
  - Qoff = 0B (Output Buffer enabled) in MR1;
  - TDQS disabled in MR1;
  - CRC disabled in MR2;
  - CA parity feature disabled in MR5;
  - Gear down mode disabled in MR3;
  - Read/Write DBI disabled in MR5;
  - DM disabled in MR5
- Attention: The I_{DD}, I_{PP} and I_{DDQ} Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {$\overline{CS}$, $\overline{ACT}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}: = {HIGH, LOW, LOW, LOW, LOW} apply BG/BA changes when directed.
- Define D# = {$\overline{CS}$, $\overline{ACT}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}: = {HIGH, HIGH, HIGH, HIGH, HIGH} apply invert of BG/BA changes when directed above.

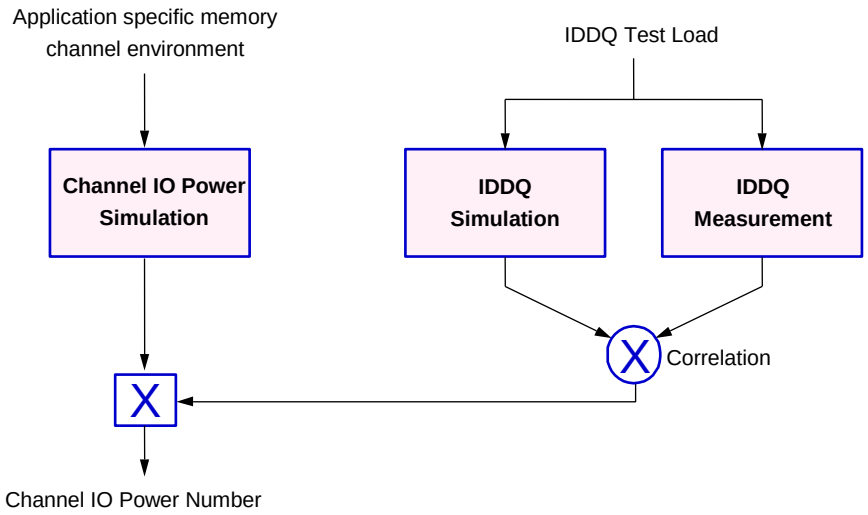
Measurement Setup and Test Load for I_{DD}, I_{PP} and I_{DDQ}



NOTE 1 DIMM level Output test load condition may be different from above.

NOTE 2 For information only.

Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement



IDD, IDDQ and IPP Specification

Timings used for I_{DD}, I_{PP} and I_{DDQ} Measurement-Loop Patterns

Symbol		DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	Unit
		11	13	15	17	19	
tCK		1.25	1.071	0.937	0.833	0.75	ns
CL		11	13	15	17	19	nCK
CWL		11	12	14	16	18	nCK
nRCD		11	13	15	17	19	nCK
nRC		39	45	51	55	62	nCK
nRAS		28	32	36	39	43	nCK
nRP		11	13	15	17	19	nCK
nFAW	x4	16	16	16	16	16	nCK
	x8	20	22	23	28	28	nCK
	x16	28	28	32	40	40	nCK
nRRDS	x4	4	4	4	4	4	nCK
	x8	4	4	4	4	4	nCK
	x16	5	5	6	8	8	nCK
nRRDL	x4	5	5	6	7	7	nCK
	x8	5	5	6	7	7	nCK
	x16	6	6	7	9	9	nCK
tCCD_S		4	4	4	4	4	nCK
tCCD_L		5	5	6	6	7	nCK
tWTR_S		2	3	3	3	4	nCK
tWTR_L		6	7	8	9	10	nCK
nRFC 4Gb		208	243	278	313	347	nCK

Basic IDD, IPP, and IDDQ Measurement Conditions

Symbol	Description
I_{DD0}	**Operating One Bank Active-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns **BL:** 8[1]; **AL:** 0; $\overline{CS}$**:** High between ACT and PRE; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to table (IDD0, IDD0A and IPP0 Measurement-Loop Pattern) **Data IO:** VDDQ; $\overline{DM}$**:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2, 2, (see: IDD0, IDD0A and IPP0 Measurement-Loop Pattern); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD0, IDD0A and IPP0 Measurement-Loop Pattern
I_{DD0A}	**Operating One Bank Active-Precharge Current (AL=CL-1)** **AL = CL-1,** **Other conditions:** see IDD0
I_{PP0}	**Operating One Bank Active-Precharge IPP Current** **Same condition with IDD0**
I_{DD1}	**Operating One Bank Active-Read-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns; **BL:** 8[1]; **AL:** 0; $\overline{CS}$: High between ACT, RD and PRE; **Command, Address, Bank Group Address, Bank Address Inputs, Data IO:** partially toggling according to table (IDD1, IDD1A and IPP1 Measurement-Loop Pattern); $\overline{DM}$**:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2, 2, (see: IDD0, IDD0A and IPP0 Measurement-Loop Pattern); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD1, IDD1A and IPP1 Measurement-Loop Pattern
I_{DD1A}	**Operating One Bank Active-Read-Precharge Current (AL=CL-1)** **AL = CL-1,** **Other conditions:** see IDD1
I_{PP1}	**Operating One Bank Active-Read-Precharge IPP Current** **Same condition with IDD1**
I_{DD2N}	**Precharge Standby Current (AL=0)** **CKE**: High; **External clock:** On; **tCK, CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns; **BL:** 8[1]; **AL:** 0; $\overline{CS}$: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to table (IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2, IDD3N, IDD3NA and IDD3P Measurement-Loop Pattern) **Data IO:** VDDQ; $\overline{DM}$**:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2, IDD3N, IDD3NA and IDD3P Measurement-Loop Pattern

Symbol	Description
I_{DD2NA}	**Precharge Standby Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD2N
I_{PP2N}	**Precharge Standby IPP Current** **Same condition with IDD2N**
I_{DD2NT}	**Precharge Standby ODT Current** **CKE**: High; **External clock:** On; **tCK, CL:** see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns; **BL:** 8[1]; **AL:** 0; $\overline{CS}$: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to see Timings used for IDD2NT and IDDQ2NT Measurement-Loop Pattern; **Data IO:** VSSQ; $\overline{DM}$: stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** toggling according to IDD2NT and IDDQ2NT Measurement-Loop Pattern **Pattern Details:** see IDD2NT and IDDQ2NT Measurement-Loop Pattern
I_{DDQ2NT} (Optional)	**Precharge Standby ODT IDDQ Current** Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
I_{DD2NL}	**Precharge Standby Current with CAL enabled** Same definition like for IDD2N, CAL enabled[3]
I_{DD2NG}	**Precharge Standby Current with Gear Down mode enabled** Same definition like for IDD2N, Gear Down mode enabled[3,5]
I_{DD2ND}	**Precharge Standby Current with DLL disabled** Same definition like for IDD2N, DLL disabled[3]
I_{DD2N_par}	**Precharge Standby Current with CA parity enabled** Same definition like for IDD2N, CA parity enabled[3]
I_{DD2P}	**Precharge Power-Down Current** **CKE:** Low; **External clock:** On; **tCK, CL:** see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns; **BL:** 8[1]; **AL:** 0; $\overline{CS}$: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; $\overline{DM}$: stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
I_{PP2P}	**Precharge Power-Down IPP Current** **Same condition with IDD2P**
I_{DD2Q}	**Precharge Quiet Standby Current** **CKE**: High; **External clock:** On; **tCK, CL:** see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns; **BL:** 8[1]; **AL:** 0; $\overline{CS}$: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; $\overline{DM}$: stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0

Symbol	Description
I_{DD3N}	**Active Standby Current** **CKE**: High; **External clock:** On; **tCK, CL:** see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns; **BL:** 8[1]; **AL:** 0; $\overline{CS}$: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to table(IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2, IDD3N, IDD3NA and IDD3P Measurement-Loop Pattern) **Data IO:** VDDQ; $\overline{DM}$: stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2, IDD3N, IDD3NA and IDD3P Measurement-Loop Pattern
I_{DD3NA}	**Active Standby Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD3N
I_{PP3N}	**Active Standby IPP Current** **Same condition with IDD3N**
I_{DD3P}	**Active Power-Down Current** **CKE:** Low; **External clock:** On; **tCK, CL:** see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns; **BL:** 8[1]; **AL:** 0; $\overline{CS}$: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; $\overline{DM}$: stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
I_{PP3P}	**Active Power-Down IPP Current** **Same condition with IDD3P**
I_{DD4R}	**Operating Burst Read Current** **CKE:** High; **External clock:** On; **tCK, CL:** see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns; **BL:** 8[2]; **AL:** 0; $\overline{CS}$: High between RD; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD4R, IDD4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern **Data IO:** seamless read data burst with different data between one burst and the next one according to IDD4R, IDD4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern $\overline{DM}$: stable at 1; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2, 2, (see IDD4R, IDD4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD4R, IDD4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern;
I_{DD4RA}	**Operating Burst Read Current (AL=CL-1)** **AL = CL-1,** **Other conditions:** see IDD4R
Symbol	**Description**

I_{DD4RB}	**Operating Burst Read Current with Read DBI** **Read DBI enabled[3],** **Other conditions:** see IDD4R
I_{PP4R}	**Operating Burst Read IPP Current** **Same condition with IDD4R**
I_{DDQ4R} (Optional)	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
I_{DDQ4RB} (Optional)	**Operating Burst Read IDDQ Current with Read DBI** Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current
I_{DD4W}	**Operating Burst Write Current** **CKE:** High; **External clock:** On; **tCK, CL:** see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns; **BL:** 8[1]; **AL:** 0; $\overline{CS}$: High between WR; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD0, IDD0A and IPP0 Measurement-Loop Pattern **Data IO:** seamless write data burst with different data between one burst and the next one according to table (IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern) $\overline{DM}$: stable at 1; **Bank Activity:** all banks open, WR commands cycling through banks: 0,0,1,1,2, 2, (see IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at HIGH; **Pattern Details:** see IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern
I_{DD4WA}	**Operating Burst Write Current (AL=CL-1)** **AL = CL-1,** **Other conditions:** see IDD4W
I_{DD4WB}	**Operating Burst Write Current with Write DBI** **Write DBI enabled[3],** **Other conditions:** see IDD4W
I_{DD4WC}	**Operating Burst Write Current with Write CRC** **Write CRC enabled[3],** **Other conditions:** see IDD4W
I_{DD4W_par}	**Operating Burst Write Current with CA Parity** **CA Parity enabled[3],** **Other conditions:** see IDD4W
I_{PP4W}	**Operating Burst Write IPP Current** **Same condition with IDD4W**
I_{DD5B}	**Burst Refresh Current (1X REF)** **CKE:** High; **External clock:** On; **tCK, CL, nRFC**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns; **BL:** 8[1]; **AL:** 0; $\overline{CS}$: High between REF; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to table(IDD5B Measurement-Loop Pattern) **Data IO:** VDDQ; $\overline{DM}$: stable at 1; **Bank Activity:** REF command every nRFC (see IDD5B Measurement-Loop Pattern); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD5B Measurement-Loop Pattern
I_{PP5B}	**Burst Refresh Write IPP Current (1X REF)** **Same condition with IDD5B**
Symbol	**Description**

I_{DD5F2}	**Burst Refresh Current (2X REF)** **tRFC=tRFC_x2, Other conditions:** see IDD5B
I_{PP5F2}	**Burst Refresh Write IPP Current (2X REF)** **Same condition with IDD5F2**
I_{DD5F4}	**Burst Refresh Current (4X REF)** **tRFC=tRFC_x4, Other conditions:** see IDD5B
I_{PP5F4}	**Burst Refresh Write IPP Current (4X REF)** **Same condition with IDD5F4**
I_{DD6N}	**Self Refresh Current: Normal Temperature Range** ***T*CASE:** 0 - 85°C; **Low Power Array Self Refresh (LP ASR):** Normal[4]; **CKE:** Low; **External clock:** Off; CK and $\overline{CK}$: LOW; **CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **$\overline{DM}$:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
I_{PP6N}	**Self Refresh IPP Current: Normal Temperature Range** **Same condition with IDD6N**
I_{DD6E}	**Self-Refresh Current: Extended Temperature Range** ***T*CASE:** 0 - 95°C; **Low Power Array Self Refresh (LP ASR):** Extended[4]; **CKE:** Low; **External clock:** Off; CK and $\overline{CK}$: LOW; **CL**: Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **$\overline{DM}$**: stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
I_{PP6E}	**Self Refresh IPP Current: Extended Temperature Range Same condition with IDD6E**
I_{DD6R}	**Self-Refresh Current: Reduced Temperature Range** ***T*CASE:** 0 - 45°C; **Low Power Array Self Refresh (LP ASR):** Reduced[4]; **CKE:** Low; **External clock:** Off; CK and $\overline{CK}$: LOW; **CL**: Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **$\overline{DM}$**: stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
I_{PP6R}	**Self Refresh IPP Current: Reduced Temperature Range** **Same condition with IDD6R**
I_{DD6A}	**Auto Self-Refresh Current** ***T*CASE:** 0 - 95°C; **Low Power Array Self Refresh (LP ASR):** Auto[4]; **CKE:** Low; **External clock:** Off; CK and $\overline{CK}$: LOW; **CL**: Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$, Command, Address, Bank Group Address, Bank Address, Data IO:** High;

	$\overline{DM}$: stable at 1; **Bank Activity:** Auto Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
I_{PP6A}	**Auto Self-Refresh IPP Current** **Same condition with IDD6A**
I_{DD7}	**Operating Bank Interleave Read Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns; **BL:** 8[1]; **AL:** CL-1; $\overline{CS}$: High between ACT and RDA; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Timings used for see table(IDD7 Measurement-Loop Pattern) **Data IO:** read data bursts with different data between one burst and the next one according to IDD7 Measurement-Loop Pattern $\overline{DM}$: stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing, see IDD7 Measurement-Loop Pattern **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD7 Measurement-Loop Pattern
I_{PP7}	**Operating Bank Interleave Read IPP Current** **Same condition with IDD7**
I_{DD8}	**Maximum Power Down Current**
I_{PP8}	**Maximum Power Down IPP Current** **Same condition with IDD8**

NOTE 1 Burst Length: BL8 fixed by MRS: set MR0 A [1:0] =00.

NOTE 2 Output Buffer Enable:
- set MR1 A12 = 0: Qoff = Output buffer enabled
- set MR1 A [2:1] = 00: Output Driver Impedance Control = RZQ/7
RTT_NOM enable:
- set MR1 A [10:8] = 011: RTT_NOM = RZQ/6
RTT_WR enable:
- set MR2 A [10:9] = 01: RTT_WR = RZQ/2
RTT_PARK disable:
- set MR5 A [8:6] = 000

NOTE 3 CAL enabled :
- set MR4 A[8:6]=001 : 1600 MT/s
- set MR4 A [8:6] =010: 1866,2133 MT/s
- set MR4 A [8:6] =011: 2400MT/s
Gear Down mode enabled:
- set MR3 A3 = 1: 1/4 Rate
DLL disabled:
- set MR1 A0 = 0
CA parity enabled:
- set MR5 A [2:0] = 001: 1600,1866,2133MT/s
- set MR5 A [2:0] = 010: 2400MT/s
Read DBI enabled:
- set MR5 A12 = 1
Write DBI enabled:
- set: MR5 A11 = 1

NOTE 4 Low Power Array Self Refresh (LP ASR):
- set MR2 A [7:6] = 00: Normal
- set MR2 A [7:6] = 01: Reduced Temperature range
- set MR2 A [7:6] = 10: Extended Temperature range
- set MR2 A [7:6] = 11: Auto Self Refresh

NOTE 5 IDD2NG should be measured after sync pulse(NOP) input.

NOTE 6 The IDD values must be derated (increased) when operated outside of the range 0°C ≤TC≤ 85°C

I_{DD0}, I_{DD0A} and I_{PP0} Measurement-Loop Pattern

CK / $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ / A16	$\overline{CAS}$ / A15	$\overline{WE}$ / A14	ODT	BG[1:0][2]	BA[1:0]	A12/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	**ACT**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			3,4	D_#, D_#	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	–
			…	repeat pattern 1...4 until nRAS - 1, truncate if necessary															
			nRAS	**PRE**	0	1	0	1	0	0	0	0	0	0	0	0	0	0	–
			…	repeat pattern 1...4 until nRC - 1, truncate if necessary															
		1	1*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 1 instead															
		2	2*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead															
		3	3*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 3 instead															
		4	4*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead															
		5	5*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 2 instead															
		6	6*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead															
		7	7*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 0 instead															
		8	8*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead															For x4 and x8 only
		9	9*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 1 instead															
		10	10*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead															
		11	11*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 3 instead															
		12	12*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead															
		13	13*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 2 instead															
		14	14*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead															
		15	15*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 0 instead															

NOTE 1 DQS, $\overline{DQS}$ are VDDQ.

NOTE 2 DBG1 is a don't care for x16 devices.

NOTE 3 DQ signals are VDDQ.

I_{DD1}, I_{DD1A} and I_{PP1} Measurement-Loop Pattern

CK / $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ / A16	$\overline{CAS}$ / A15	$\overline{WE}$ / A14	ODT	BG[1:0][2]	BA[1:0]	A12/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	**ACT**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			3,4	D_#, D_#	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	–
			…	repeat pattern 1...4 until nRCD - AL - 1, truncate if necessary															
			nRCD -AL	**RD**	0	1	1	0	1	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
				repeat pattern 1...4 until nRAS - 1, truncate if necessary															
			nRAS	**PRE**	0	1	0	1	0	0	0	0	0	0	0	0	0	0	–
			…	repeat pattern 1...4 until nRC - 1, truncate if necessary															
		1	1*nRC + 0	**ACT**	0	0	0	1	1	0	1	1	0	0	0	0	0	0	
			1*nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
			1*nRC + 3, 4	D#, D#	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	
			…	repeat pattern nRC + 1...4 until 1*nRC + nRAS - 1, truncate if necessary															
			1*nRC + nRCD - AL	**RD**	0	1	1	0	1	0	1	1	0	0	0	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			…	repeat pattern 1...4 until nRAS - 1, truncate if necessary															
			1*nRC + nRAS	**PRE**	0	1	0	1	0	0	1	1	0	0	0	0	0	0	
			…	repeat nRC + 1...4 until 2*nRC - 1, truncate if necessary															
		2	2*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead															
		3	3*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead															
		4	4*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead															
		5	5*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2 instead															
		6	6*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead															
		7	7*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead															
		9	9*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead															For x4 and x8 only
		10	10*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 2, BA[1:0] = 0 instead															
		11	11*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 1 instead															
		12	12*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 2, BA[1:0] = 2 instead															
		13	13*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 3 instead															
		14	14*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 2, BA[1:0] = 1 instead															
		15	15*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 2 instead															

NOTE 1 DQS, $\overline{DQS}$ are used according to RD Commands, otherwise VDDQ.

NOTE 2 BG1 is don't care for x16 device.

NOTE 3 Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

I_{DD2N}, I_{DD2NA}, I_{DD2NL}, I_{DD2NG}, I_{DD2ND}, I_{DD2N_par}, I_{PP2}, I_{DD3N}, I_{DD3NA} and I_{DD3P} Measurement-Loop Pattern

CK / $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ / A16	$\overline{CAS}$ / A15	$\overline{WE}$ / A14	ODT	BG[1:0][2]	BA[1:0]	A12/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			2	D#, D#	1	1	1	1	1	0	3^2	3	0	0	0	7	F	0	0
			3	D#, D#	1	1	1	1	1	0	3^2	3	0	0	0	7	F	0	0
		1	4-7	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 1 instead														
		2	8-11	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead														
		3	12-15	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 3 instead														
		4	16-19	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead														
		5	20-23	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 2 instead														
		6	24-27	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead														
		7	28-31	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 0 instead														
		8	32-35	`repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead														
		9	36-39	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 1 instead														
		10	40-43	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead														
		11	44-47	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 3 instead														
		12	48-51	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead														
		13	52-55	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 2 instead														
		14	56-59	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead														
		15	60-63	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 0 instead														

NOTE 1 DQS, $\overline{DQS}$ are VDDQ.

NOTE 2 BG1 is don't care for x16 device.

NOTE 3 DQ signals are VDDQ.

I_{DD2NT} and I_{DDQ2NT} Measurement-Loop Pattern

CK / $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ / A16	$\overline{CAS}$ / A15	$\overline{WE}$ / A14	ODT	BG[1:0][2]	BA[1:0]	A12/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			2	D#, D#	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	–
			3	D#, D#	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	–
		1	4-7	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]2 = 1, BA[1:0] = 1 instead															
		2	8-11	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]2 = 0, BA[1:0] = 2 instead															
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]2 = 1, BA[1:0] = 3 instead															
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]2 = 0, BA[1:0] = 1 instead															
		5	20-23	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]2 = 1, BA[1:0] = 2 instead															
		6	24-27	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]2 = 0, BA[1:0] = 3 instead															
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]2 = 1, BA[1:0] = 0 instead															
		8	32-35	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]2 = 2, BA[1:0] = 0 instead															For x4 and x8 only
		9	36-39	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]2 = 3, BA[1:0] = 1 instead															
		10	40-43	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]2 = 2, BA[1:0] = 2 instead															
		11	44-47	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]2 = 3, BA[1:0] = 3 instead															
		12	48-51	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]2 = 2, BA[1:0] = 1 instead															
		13	52-55	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]2 = 3, BA[1:0] = 2 instead															
		14	56-59	repeat Sub-Loop 0, but ODT = 0 and BG[1:0]2 = 2, BA[1:0] = 3 instead															
		15	60-63	repeat Sub-Loop 0, but ODT = 1 and BG[1:0]2 = 3, BA[1:0] = 0 instead															

NOTE 1 DQS, $\overline{DQS}$ are VDDQ.

NOTE 2 BG1 is don't care for x16 device

NOTE 3 DQ signals are VDDQ.

I_{DD4R}, I_{DD4RA}, I_{DD4RB} and I_{DDQ4R} Measurement-Loop Pattern

CK / $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ / A16	$\overline{CAS}$ / A15	$\overline{WE}$ / A14	ODT	BG[1:0][2]	BA[1:0]	A12/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	**RD**	0	1	1	0	1	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			2,3	D#, D#	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	–
		1	4	**RD**	0	1	1	0	1	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			6,7	D#, D#	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	–
		2	8-11	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead														
		3	12-15	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead														
		4	16-19	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead														
		5	20-23	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2 instead														
		6	24-27	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead														
		7	28-31	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead														
		8	32-35	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead														For x4 and x8 only
		9	36-39	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 1 instead														
		10	40-43	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead														
		11	44-47	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 3 instead														
		12	48-51	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead														
		13	52-55	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 2 instead														
		14	56-59	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead														
		15	60-63	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 0 instead														

NOTE 1 DQS, $\overline{DQS}$ are used according to RD Commands, otherwise VDDQ.

NOTE 2 BG1 is don't care for x16 device

NOTE 3 Burst Sequence driven on each DQ signal by Read Command.

I_{DD4W}, I_{DD4WA}, I_{DD4WB} and I_{DD4W_par} Measurement-Loop Pattern

CK / $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ / A16	$\overline{CAS}$ / A15	$\overline{WE}$ / A14	ODT	BG[1:0][2]	BA[1:0]	A12/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			1	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	–
			2,3	D#, D#	1	1	1	1	1	1	3[2]	3	0	0	0	7	F	0	–
		1	4	WR	0	1	1	0	0	1	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			5	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	–
			6,7	D#, D#	1	1	1	1	1	1	3[2]	3	0	0	0	7	F	0	–
		2	8-11	repeat Sub-Loop 0, use BG[1:0]2 = 0, BA[1:0] = 2 instead														
		3	12-15	repeat Sub-Loop 1, use BG[1:0]2 = 1, BA[1:0] = 3 instead															
		4	16-19	repeat Sub-Loop 0, use BG[1:0]2 = 0, BA[1:0] = 1 instead															
		5	20-23	repeat Sub-Loop 1, use BG[1:0]2 = 1, BA[1:0] = 2 instead															
		6	24-27	repeat Sub-Loop 0, use BG[1:0]2 = 0, BA[1:0] = 3 instead															
		7	28-31	repeat Sub-Loop 1, use BG[1:0]2 = 1, BA[1:0] = 0 instead															
		8	32-35	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 0 instead															For x4 and x8 only
		9	36-39	repeat Sub-Loop 1, use BG[1:0]2 = 3, BA[1:0] = 1 instead															
		10	40-43	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 2 instead															
		11	44-47	repeat Sub-Loop 1, use BG[1:0]2 = 3, BA[1:0] = 3 instead															
		12	48-51	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 1 instead															
		13	52-55	repeat Sub-Loop 1, use BG[1:0]2 = 3, BA[1:0] = 2 instead															
		14	56-59	repeat Sub-Loop 0, use BG[1:0]2 = 2, BA[1:0] = 3 instead															
		15	60-63	repeat Sub-Loop 1, use BG[1:0]2 = 3, BA[1:0] = 0 instead															

NOTE 1 DQS, $\overline{DQS}$ are used according to WR Commands, otherwise VDDQ.

NOTE 2 BG1 is don't care for x16 device

NOTE 3 Burst Sequence driven on each DQ signal by Write Command.

I_{DD4WC} Measurement-Loop Pattern

CK / $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ / A16	$\overline{CAS}$ / A15	$\overline{WE}$ / A14	ODT	BG[1:0][2]	BA[1:0]	A12/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=CRC
			1,2	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	–
			3,4	D#, D#	1	1	1	1	1	1	3[2]	3	0	0	0	7	F	0	–
			5	WR	0	1	1	0	0	1	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=CRC
			6,7	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	–
			8,9	D#, D#	1	1	1	1	1	1	3[2]	3	0	0	0	7	F	0	–
		2	10-14	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead														
		3	15-19	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead															
		4	20-24	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead															
		5	25-29	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2 instead															
		6	30-34	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead															
		7	35-39	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead															
		8	40-44	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead															For x4 and x8 only
		9	45-49	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 1 instead															
		10	50-54	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead															
		11	55-59	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 3 instead															
		12	60-64	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead															
		13	65-69	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 2 instead															
		14	70-74	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead															
		15	70-74	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 0 instead															

NOTE 1 DQS, $\overline{DQS}$ are VDDQ.

NOTE 2 BG1 is don't care for x16 device.

NOTE 3 Burst Sequence driven on each DQ signal by Write Command.

I_{DD5B} Measurement-Loop Pattern

CK / $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ / A16	$\overline{CAS}$ / A15	$\overline{WE}$ / A14	ODT	BG[1:0][2]	BA[1:0]	A12/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	REF	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
		1	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			3	D#, D#	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	–
			4	D#, D#	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	–
			4-7	repeat pattern 1...4, use BG[1:0]2 = 1, BA[1:0] = 1 instead															
			8-11	repeat pattern 1...4, use BG[1:0]2 = 0, BA[1:0] = 2 instead															
			12-15	repeat pattern 1...4, use BG[1:0]2 = 1, BA[1:0] = 3 instead															
			16-19	repeat pattern 1...4, use BG[1:0]2 = 0, BA[1:0] = 1 instead															
			20-23	repeat pattern 1...4, use BG[1:0]2 = 1, BA[1:0] = 2 instead															
			24-27	repeat pattern 1...4, use BG[1:0]2 = 0, BA[1:0] = 3 instead															
			28-31	repeat pattern 1...4, use BG[1:0]2 = 1, BA[1:0] = 0 instead															
			32-35	repeat pattern 1...4, use BG[1:0]2 = 2, BA[1:0] = 0 instead															For x4 and x8 only
			36-39	repeat pattern 1...4, use BG[1:0]2 = 3, BA[1:0] = 1 instead															
			40-43	repeat pattern 1...4, use BG[1:0]2 = 2, BA[1:0] = 2 instead															
			44-47	repeat pattern 1...4, use BG[1:0]2 = 3, BA[1:0] = 3 instead															
			48-51	repeat pattern 1...4, use BG[1:0]2 = 2, BA[1:0] = 1 instead															
			52-55	repeat pattern 1...4, use BG[1:0]2 = 3, BA[1:0] = 2 instead															
			56-59	repeat pattern 1...4, use BG[1:0]2 = 2, BA[1:0] = 3 instead															
			60-63	repeat pattern 1...4, use BG[1:0]2 = 3, BA[1:0] = 0 instead															
		2	64 ... nRFC - 1	repeat Sub-Loop 1, Truncate, if necessary															

NOTE 1 DQS, $\overline{DQS}$ are VDDQ.

NOTE 2 BG1 is don't care for x16 device.

NOTE 3 DQ signals are VDDQ.

I_{DD7} Measurement-Loop Pattern

CK / $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ / A16	$\overline{CAS}$ / A15	$\overline{WE}$ / A14	ODT	BG[1:0][2]	BA[1:0]	A12/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	**ACT**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1	**RDA**	0	1	1	0	1	0	0	0	0	0	1	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			3	D#	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	–
			…	repeat pattern 2...3 until nRRD - 1, if nRCD > 4. Truncate if necessary															
		1	nRRD	**ACT**	0	0	0	0	0	0	1	1	0	0	0	0	0	0	–
			nRRD + 1	**RDA**	0	1	1	0	1	0	1	1	0	0	1	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			…	repeat pattern 2 ... 3 until 2*nRRD - 1, if nRCD > 4. Truncate if necessary															
		2	2*nRRD	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead															
		3	3*nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead															
		4	4*nRRD	repeat pattern 2 ... 3 until nFAW - 1, if nFAW > 4*nRCD. Truncate if necessary															
		5	nFAW	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead															
		6	nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2 instead															
		7	nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead															
		8	nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead															
		9	nFAW + 4*nRRD	repeat Sub-Loop 4															
		10	2*nFAW	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead															For x4 and x8 only
		11	2*nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 1 instead															
		12	2*nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead															
		13	2*nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 3 instead															
		14	2*nFAW + 4*nRRD	repeat Sub-Loop 4															
		15	3*nFAW	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead															
		16	3*nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 2 instead															
		17	3*nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead															
		18	3*nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 0 instead															
		19	3*nFAW + 4*nRRD	repeat Sub-Loop 4															
		20	4*nFAW	repeat pattern 2 ... 3 until nRC - 1, if nRC > 4*nFAW. Truncate if necessary															

NOTE 1 DQS, $\overline{DQS}$ are VDDQ.

NOTE 2 BG1 is don't care for x16 device.

NOTE 3 Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

IDD Specifications

Symbol	Description	DDR4-2666			Unit
		X4	X8	X16	
I_{DD0}	Operating One Bank Active-Precharge Current (AL=0)	67.03	70.84	74.36	mA
I_{DD0A}	Operating One Bank Active-Precharge Current (AL=CL-1)	67.53	71.28	74.80	mA
I_{PP0}	Operating One Bank Active-Precharge IPP Current	3.24	4.50	5.81	mA
I_{DD1}	Operating One Bank Active-Read-Precharge Current (AL=0)	80.68	89.32	105.16	mA
I_{DD1A}	Operating One Bank Active-Read-Precharge Current (AL=CL-1)	83.68	93.28	110.44	mA
I_{PP1}	Operating One Bank Active-Read-Precharge IPP Current	3.24	4.50	5.81	mA
I_{DD2N}	Precharge Standby Current (AL=0)	50.49	51.29	52.58	mA
I_{DD2NA}	Precharge Standby Current (AL=CL-1)	50.71	51.54	53.02	mA
I_{PP2N}	Precharge Standby IPP Current	1.00	1.27	1.85	mA
I_{DD2NT}	Precharge Standby ODT Current	70.79	72.28	75.68	mA
I_{DDQ2NT}	Precharge Standby ODT IDDQ Current	1.94	3.19	5.39	mA
I_{DD2NL}	Precharge Standby Current with CAL enabled	34.00	35.61	37.00	mA
I_{DD2NG}	Precharge Standby Current with Gear Down mode enabled	50.15	50.96	52.14	mA
I_{DD2ND}	Precharge Standby Current with DLL disabled	60	60	60	mA
I_{DD2N_par}	Precharge Standby Current with CA parity enabled	62	62	62	mA
I_{DD2P}	Precharge Power-Down Current	23.26	24.14	28.36	mA
I_{PP2P}	Precharge Power-Down IPP Current	1.00	1.27	1.88	mA
I_{DD2Q}	Precharge Quiet Standby Current	33.10	34.02	38.07	mA
I_{DD3N}	Active Standby Current	71.29	72.18	75.59	mA
I_{DD3NA}	Active Standby Current (AL=CL-1)	71.57	72.52	75.89	mA
I_{PP3N}	Active Standby IPP Current	1.00	1.25	1.85	mA
I_{DD3P}	Active Power-Down Current	36.83	37.73	42.02	mA
I_{PP3P}	Active Power-Down IPP Current	1.00	1.25	1.85	mA
I_{DD4R}	Operating Burst Read Current	154.32	192.06	267.30	mA
I_{DD4RA}	Operating Burst Read Current (AL=CL-1)	164.41	209.44	301.84	mA
I_{DD4RB}	Operating Burst Read Current with Read DBI	154.37	192.94	264.22	mA
I_{PP4R}	Operating Burst Read IPP Current	1.00	1.27	1.90	mA
I_{DDQ4R}	Operating Burst Read IDDQ Current	26.78	46.20	89.32	mA
I_{DDQ4RB}	Operating Burst Read IDDQ Current with Read DBI	28.17	28.17	38.72	mA
I_{DD4W}	Operating Burst Write Current	173.65	201.96	263.12	mA
I_{DD4WA}	Operating Burst Write Current (AL=CL-1)	184.72	211.64	273.24	mA
I_{DD4WB}	Operating Burst Write Current with Write DBI	173.65	202.84	265.32	mA

I_{DD4WC}	Operating Burst Write Current with Write CRC	180.36	232.54	329.34	mA
I_{DD4W_par}	Operating Burst Write Current with CA Parity	199.87	209.87	281.16	mA
I_{PP4W}	Operating Burst Write IPP Current	1.00	1.25	1.87	mA
I_{DD5B}	Burst Refresh Current (1X REF)	145.98	150.98	155.98	mA
I_{PP5B}	Burst Refresh Write IPP Current (1X REF)	34.66	36.43	36.43	mA
I_{DD5F2}	Burst Refresh Current (2X REF)	132.78	137.78	142.78	mA
I_{PP5F2}	Burst Refresh Write IPP Current (2X REF)	29.66	30.58	30.67	mA
I_{DD5F4}	Burst Refresh Current (4X REF)	117.42	118.42	123.42	mA
I_{PP5F4}	Burst Refresh Write IPP Current (4X REF)	21.24	23.41	23.41	mA
I_{DD6N}	Self Refresh Current: Normal Temperature Range	23.69	24.64	28.19	mA
I_{PP6N}	Self Refresh IPP Current: Normal Temperature Range	1.95	3.34	3.87	mA
I_{DD6E}	Self-Refresh Current: Extended Temperature Range	27.40	28.60	31.62	mA
I_{PP6E}	Self Refresh IPP Current: Extended Temperature Range	3.10	3.12	4.05	mA
I_{DD6R}	Self-Refresh Current: Reduced Temperature Range	21.00	22.00	25.00	mA
I_{PP6R}	Self Refresh IPP Current: Reduced Temperature Range	1.35	2.73	3.26	mA
I_{DD6A}	Auto Self-Refresh Current	26.00	27.72	30.00	mA
I_{PP6A}	Auto Self-Refresh IPP Current	3.09	3.09	4.06	mA
I_{DD7}	Operating Bank Interleave Read Current	234.81	225.00	274.56	mA
I_{PP7}	Operating Bank Interleave Read IPP Current	50.00	25.34	33.48	mA
I_{DD8}	Maximum Power Down Current	18.00	22.00	22.00	mA
I_{PP8}	Maximum Power Down IPP Current	1.00	1.25	1.70	mA

Note: Published IDD values are the maximum of the distribution of the arithmetic mean and are measured at 95℃.

I_{DD6} Specification

Symbol	Temperature Range	NOTE
I_{DD6N}	0 - 85 ºC	3,4
I_{DD6E}	0 - 95 ºC	4,5,6
I_{DD6R}	0 - 45 ºC	4,6,9
I_{DD6A}	0 ºC ~ Ta	4,6,7,8
	Tb ~ Ty	4,6,7,8
	Tz ~ TOPERmax	4,6,7,8

NOTE 1 Some IDD currents are higher for x16 organization due to larger page-size architecture.

NOTE 2 Max values for IDD currents considering worst case conditions of process, temperature and voltage.

NOTE 3 Applicable for MR2 settings A6=0 and A7=0.

NOTE 4 Supplier data sheets include a max value for IDD6.

NOTE 5 Applicable for MR2 settings A6=0 and A7=1. IDD6E is only specified for devices which support the Extended Temperature Range feature.

NOTE 6 Refer to the supplier data sheet for the value specification method (e.g. max, typical) for IDD6E and IDD6A

NOTE 7 Applicable for MR2 settings A6=1 and A7=0. IDD6A is only specified for devices which support the Auto Self Refresh feature.

NOTE 8 The number of discrete temperature ranges supported and the associated Ta - Tz values are supplier/design specific. Temperature ranges are specified for all supported values of T_{OPER}. Refer to supplier data sheet for more information.

NOTE 9 Applicable for MR2 settings MR2 [A7:A6 = 01] : Reduced Temperature range. IDD6R is verified by design and characterization, and may not be subject to production test

Input / Output Capacitance

Silicon pad I/O Capacitance

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400/2666		Unit	Notes
		Min	Max	Min	Max		
C_{IO}	Input/output capacitance	0.55	1.4	0.55	1.15	pF	1,2,3
C_{DIO}	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	pF	1,2,3,11
C_{DDQS}	Input/output capacitance delta DQS and $\overline{DQS}$	-	0.05	-	0.05	pF	1,2,3,5
C_{CK}	Input capacitance, CK and $\overline{CK}$	0.2	0.8	0.2	0.7	pF	1,3
C_{DCK}	Input capacitance delta CK and $\overline{CK}$	-	0.05	-	0.05	pF	1,3,4
C_{I}	Input capacitance(CTRL, ADD, CMD pins)	0.2	0.8	0.2	0.7	pF	1,3,6
C_{DI_CTRL}	Input capacitance delta(All CTRL pins)	-0.1	0.1	-0.1	0.1	pF	1,3,7,8
$C_{DI\_ADD\_CMD}$	Input capacitance delta(All ADD/ CMD pins)	-0.1	0.1	-0.1	0.1	pF	1,2,9,10
C_{ALERT}	Input/output capacitance of $\overline{ALERT}$	0.5	1.5	0.5	1.5	pF	1,3
C_{ZQ}	Input/output capacitance of ZQ	-	2.3	-	2.3	pF	1,3,12
C_{TEN}	Input capacitance of TEN	0.2	2.3	0.2	2.3	pF	1,3,13

NOTE 1 This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure TBD.

NOTE 2 DQ, $\overline{DM}$, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$. Although the DM, TDQS and $\overline{TDQS}$ pins have different functions, the loading matches DQ and DQS.

NOTE 3 This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.

NOTE 4 Absolute value CK - $\overline{CK}$.

NOTE 5 Absolute value of CIO(DQS)-CIO ($\overline{DQS}$).

NOTE 6 CI applies to ODT, $\overline{CS}$, CKE, A0-A17, BA0-BA1, BG0-BG1, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14, $\overline{ACT}$ and PAR.

NOTE 7 CDI CTRL applies to ODT, $\overline{CS}$ and CKE.

NOTE 8 CDI_CTRL = CI(CTRL)-0.5*(CI(CK)+CI($\overline{CK}$))

NOTE 9 CDI_ADD_CMD = CI(ADD_CMD)-0.5*(CI(CK)+CI($\overline{CK}$)) .

NOTE 10 CDI_ADD_ CMD applies to, A0-A17, BA0-BA1, BG0-BG1,$\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14, $\overline{ACT}$ and PAR.

NOTE 11 CDIO = CIO(DQ,$\overline{DM}$)-0.5*(CIO(DQS)+CIO($\overline{DQS}$)) .

NOTE 12 Maximum external load capacitance on ZQ pin: TBD pF.

NOTE 13 TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case CTEN might not be valid and system shall verify TEN signal with Vendor specific information.

DRAM package electrical specifications(x4/x8)

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666		Unit	Notes
		Min	Max		
Z_{IO}	Input/output Zpkg	45	85	Ω	1,2,4,5,10,11
T_{dIO}	Input/output Pkg Delay	14	42	ps	1,3,4,5,11
L_{io}	Input/Output Lpkg	-	3.3	nH	11, 12
C_{io}	Input/Output Cpkg	-	0.78	pF	11, 13
Z_{IO} DQS	DQS, $\overline{DQS}$ Zpkg	45	85	Ω	1,2,5,10,11
T_{dIO} DQS	DQS, $\overline{DQS}$ Pkg Delay	14	42	ps	1,3,5,10,11
L_{io} DQS	DQS Lpkg	-	3.3	nH	11, 12
C_{io} DQS	DQS Cpkg	-	0.78	pF	11, 13
DZ_{DIO} DQ	Delta Zpkg DQS, $\overline{DQS}$	-	10	Ω	1,2,5,7,10
DT_{dDIO} DQS	Delta Delay DQS, $\overline{DQS}$	-	5	ps	1,3,5,7,10
Z_I CTRL	Input- CTRL pins Zpkg	50	90	Ω	1,2,5,9,10,11
T_{dI_CTRL}	Input- CTRL pins Pkg Delay	14	42	ps	1,3,5,9,10,11
L_i CTRL	Input CTRL Lpkg	-	3.4	nH	11, 12
C_i CTRL	Input CTRL Cpkg	-	0.7	pF	11, 13
Z_{IADD} CMD	Input- CMD ADD pins Zpkg	50	90	Ω	1,2,5,8,10,11
T_{dIADD} CMD	Input- CMD ADD pins Pkg Delay	14	45	ps	1,3,5,8,10,11
L_i ADD CMD	Input CMD ADD Lpkg	-	3.6	nH	11, 12
C_i ADD CMD	Input CMD ADD Cpkg	-	0.74	pF	11, 13
Z_{CK}	CK, $\overline{CK}$ Zpkg	50	90	Ω	1,2,5,10,11
T_{dCK}	CK, $\overline{CK}$ Pkg Delay	14	42	ps	1,3,5,10,11
L_i CLK	Input CLK Lpkg	-	3.4	nH	11, 12
C_i CLK	Input CLK Cpk	-	0.7	pF	11, 13
DZ_{DCK}	Delta Zpkg CK, $\overline{CK}$	-	10	Ω	1,2,5,6,10
DT_{dCK}	Delta Delay CK, $\overline{CK}$	-	5	ps	1,3,5,6,10
Z_O ZQ	ZQ Zpkg	-	100	Ω	1,2,5,10,11
T_{dO} ZQ	ZQ Delay	20	90	ps	1,3,5,10,11
Z_O ALERT	ALERT Zpkg	40	100	Ω	1,2,5,10,11
T_{dO} ALERT	ALERT Delay	20	55	ps	1,3,5,10,11

NOTE 1 This parameter is not subject to production test. It is verified by design and characterization. The package parasitic (L & C) are validated using package only samples. The capacitance is measured with VDD, VDDQ, VSS, VSSQ shorted with all other signal pins floating. The inductance is measured with VDD, VDDQ, VSS and VSSQ shorted and all other signal pins shorted at the die side (not pin). Measurement procedure TBD.

NOTE 2 Package only impedance (Zpkg) is calculated based on the Lpkg and Cpkg total for a given pin where:

Zpkg (total per pin) = $\sqrt{Lpkg / Cpkg}$

NOTE 3 Package only delay(Tpkg) is calculated based on Lpkg and Cpkg total for a given pin where:

Tdpkg (total per pin) = $\sqrt{Lpkg \times Cpkg}$

NOTE 4 Z & Td IO applies to DQ, $\overline{DM}$, DQS, $\overline{DQS}$, TDQS and $\overline{TDQS}$.

NOTE 5 This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.

NOTE 6 Absolute value of ZCK-Z$\overline{CK}$ for impedance(Z) or absolute value of TdCK-Td$\overline{CK}$ for delay(Td).

NOTE 7 Absolute value of ZIO(DQS)-ZIO ($\overline{DQS}$) for impedance(Z) or absolute value of TdIO(DQS)-TdIO ($\overline{DQS}$) for delay(Td).

NOTE 8 ZI & Td ADD CMD applies to A0-A13, A17, $\overline{ACT}$ BA0-BA1, BG0-BG1, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14 and $\overline{PAR}$.

NOTE 9 ZI & Td CTRL applies to ODT, $\overline{CS}$ and CKE.

NOTE 10 This table applies to monolithic X4 and X8 devices.

NOTE 11 Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum values shown.

NOTE 12 It is assumed that Lpkg can be approximated as Lpkg = Zo x Td.

NOTE 13 It is assumed that Cpkg can be approximated as Cpkg = Td / Zo.

DRAM package electrical specifications(X16)

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666		Unit	Notes
		Min	Max		
Z_{IO}	Input/output Zpkg	45	85	W	1
T_{dIO}	Input/output Pkg Delay	14	45	ps	1
L_{io}	Input/Output Lpkg	-	3.4	nH	1, 2
C_{io}	Input/Output Cpkg	-	0.82	pF	1, 3
Z_{IO} DQS	DQS, $\overline{DQS}$ Zpkg	45	85	W	1
T_{dIO} DQS	DQS, $\overline{DQS}$ Pkg Delay	14	45	ps	1
L_{io} DQS	DQS Lpkg	-	3.4	W	1, 2
C_{io} DQS	DQS Cpkg	-	0.82	W	1, 3
DZ_{DIO} DQ	Delta Zpkg DQS, $\overline{DQS}$	-	10	ps	-
DT_{dDIO} DQS	Delta Delay DQS, $\overline{DQS}$	-	5	ps	-
Z_I CTRL	Input- CTRL pins Zpkg	50	90	W	-
T_{dI_CTRL}	Input- CTRL pins Pkg Delay	14	42	ps	-
L_i CTRL	Input CTRL Lpkg	-	3.4	nH	1
C_i CTRL	Input CTRL Cpkg	-	0.7	W	1
Z_{IADD} CMD	Input- CMD ADD pins Zpkg	50	90	W	1, 2
T_{dIADD} CMD	Input- CMD ADD pins Pkg Delay	14	52	ps	1, 3
L_i ADD CMD	Input CMD ADD Lpkg	-	3.9	nH	1
C_i ADD CMD	Input CMD ADD Cpkg	-	0.86	pF	1
Z_{CK}	CK, $\overline{CK}$ Zpkg	50	90	W	1, 2
T_{dCK}	CK, $\overline{CK}$ Pkg Delay	14	42	ps	1, 3
L_i CLK	Input CLK Lpkg	-	3.4	nH	1
C_i CLK	Input CLK Cpk	-	0.7	pF	1
DZ_{DCK}	Delta Zpkg CK, $\overline{CK}$	-	10	W	1, 2
DT_{dCK}	Delta Delay CK, $\overline{CK}$	-	5	ps	1, 3
Z_O ZQ	ZQ Zpkg	-	100	W	-
T_{dO} ZQ	ZQ Delay	20	90	ps	-
Z_O ALERT	ALERT Zpkg	40	100	W	-
T_{dO} ALERT	ALERT Delay	20	55	ps	-

NOTE 1 Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum value shown.

NOTE 2 It is assumed that Lpkg can be approximated as Lpkg = Zo x Td.

NOTE 3 It is assumed that Cpkg can be approximated as Cpkg = Td / Zo.

Electrical Characteristics & AC Timing

Reference Load for AC Timing and Output Slew Rate

Reference Load for AC Timing and Output Slew Rate represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

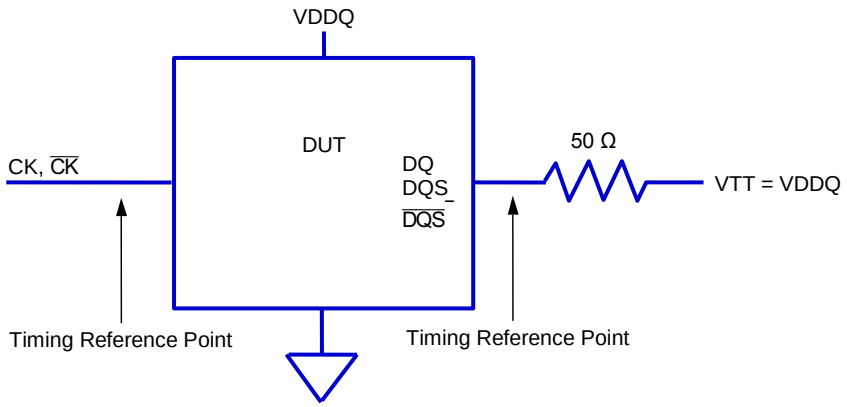
Ron nominal of DQ, DQS and $\overline{DQS}$ drivers uses 34 ohms to specify the relevant AC timing parameter values of the device.

- The maximum DC High level of Output signal = 1.0 * VDDQ,
- The minimum DC Low level of Output signal = {34 / (34 + 50)} *VDDQ = 0.4* VDDQ
- The nominal reference level of an Output signal can be approximated by the following:
- The center of maximum DC High and minimum DC Low = {(1 + 0.4) / 2} * VDDQ = 0.7 * VDDQ

The actual reference level of Output signal might vary with driver Ron and reference load tolerances. Thus, the actual reference

level or midpoint of an output signal is at the widest part of the output signal's eye. Prior to measuring AC parameters, the reference level of the verification tool should be set to an appropriate level.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



tREFI

Average periodic Refresh interval (tREFI) of DDR4 SDRAM is defined.

Parameter	Symbol		4 Gb	Units
Average periodic refresh interval	**tREFI**	TCASE ≤85ºC	7.8	µs
		85ºC≤TCASE ≤95ºC	3.9	µs

Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR4 SDRAM device.

Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject to production test.

Definition for tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK(abs)j \right) / N \qquad N = 200$$

Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCHj \right) / \{ N \times tCK(avg) \} \qquad N = 200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCLj \right) / \{ N \times tCK(avg) \} \qquad N = 200$$

Definition for tERR(nper)

tERR is defined as the cumulative error across n consecutive cycles of n x tCK(avg). tERR is not subject to production test.

AC&DC Operating conditions

Timing Parameter(Data rate 1600, 1866, 2133 specifications and conditions)

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	ns	
Average Clock Period	tCK(avg)	Refer to "Speed Bin" section						ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	Min: tCK(avg)min + tJIT(per)min_to t Max: tCK(avg)m ax + tJIT(per)m ax_tot						tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-63	63	-54	54	-47	47	ps	23
Clock Period Jitter- deterministic	JIT(per)_dj	-31	31	-27	27	-23	23	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-50	50	-43	43	-38	38	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	-	125	-	107	-	94	ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	-	100	-	86	-	75	ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR(2per)	-92	92	-79	79	-69	69	ps	
Cumulative error across 3 cycles	tERR(3per)	-109	109	-94	94	-82	82	ps	
Cumulative error across 4 cycles	tERR(4per)	-121	121	-104	104	-91	91	ps	
Cumulative error across 5 cycles	tERR(5per)	-131	131	-112	112	-98	98	ps	
Cumulative error across 6 cycles	tERR(6per)	-139	139	-119	119	-104	104	ps	
Cumulative error across 7 cycles	tERR(7per)	-145	145	-124	124	-109	109	ps	
Cumulative error across 8 cycles	tERR(8per)	-151	151	-129	129	-113	113	ps	
Cumulative error across 9 cycles	tERR(9per)	-156	156	-134	134	-117	117	ps	
Cumulative error across 10 cycles	tERR(10per)	-160	160	-137	137	-120	120	ps	
Cumulative error across 11 cycles	tERR(11per)	-164	164	-141	141	-123	123	ps	
Cumulative error across 12 cycles	tERR(12per)	-168	168	-144	144	-126	126	ps	
Cumulative error across 13 cycles	tERR(13per)	-172	172	-147	147	-129	129	ps	
Cumulative error across 14 cycles	tERR(14per)	-175	175	-150	150	-131	131	ps	
Cumulative error across 15 cycles	tERR(15per)	-178	178	-152	152	-133	133	ps	
Cumulative error across 16 cycles	tERR(16per)	-180	189	-155	155	-135	135	ps	
Cumulative error across 17 cycles	tERR(17per)	-183	183	-157	157	-137	137	ps	
Cumulative error across 18 cycles	tERR(18per)	-185	185	-159	159	-139	139	ps	
Cumulative error across n = 13, 14 . . .49, 50 cycles	tERR(nper)	tERR (nper)min = ((1 + 0.68ln(n)) * tJIT (per)_total min) tERR (nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)						ps	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Command and Address setup time to CK,$\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	**tIS(base)**	115	-	100	-	80	-	ps	
Command and Address setup time to CK,$\overline{CK}$ referenced to Vref levels	**tIS(Vref)**	215	-	200	-	180	-	ps	
Command and Address hold time to CK,$\overline{CK}$ referenced to Vih(dc) / Vil(dc) levels	**tIH(base)**	140	-	125	-	105	-	ps	
Command and Address hold time to CK,$\overline{CK}$ referenced to Vref levels	**tIH(Vref)**	215	-	200	-	180	-	ps	
Control and Address Input pulse width for each input	**tIPW**	600	-	525	-	460	-	ps	
Command and Address Timing									
$\overline{CAS}$ to $\overline{CAS}$ command delay for same bank group	**tCCD_L**	max(5nCK ,6.250 ns)	-	max(5nCK ,5.355 ns)	-	max(5nCK ,5.355 ns)	-	nCK	34
$\overline{CAS}$ to $\overline{CAS}$ command delay for different bank group	**tCCD_S**	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	**tRRD_S(2K)**	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	**tRRD_S(1K)**	Max(4nCK,5ns)	-	Max(4nCK,4.2ns)	-	Max(4nCK,3.7ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	**tRRD_S(1/2K)**	Max(4nCK,5ns)	-	Max(4nCK,4.2ns)	-	Max(4nCK,3.7ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	**tRRD_L(2K)**	Max(4nCK,7.5ns)	-	Max(4nCK,6.4ns)	-	Max(4nCK,6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	**tRRD_L(1K)**	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	**tRRD_L(1/2K)**	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK	34
Four activate window for 2KB page size	**tFAW_2K**	Max(28nCK,35ns)	-	Max(28nCK,30ns)	-	Max(28nCK,30ns)	-	ns	34
Four activate window for 1KB page size	**tFAW_1K**	Max(20nCK,25ns)	-	Max(20nCK,23ns)	-	Max(20nCK,21ns)	-	ns	34
Four activate window for 1/2KB page size	**tFAW_1/2K**	Max (16nCK,20ns)	-	Max (16nCK,17ns)	-	Max (16nCK,15ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	**tWTR_S**	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-		1,2,e,34
Delay from start of internal write transaction to internal read command for same bank group	**tWTR_L**	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-		1,34
Internal READ Command to PRECHARGE Command delay	**tRTP**	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-		
WRITE recovery time	**tWR**	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	**tWR_CRC_DM**	tWR+max (4nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	ns	1, 28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	**tWTR_S_CRC_DM**	tWTR_S+max (4nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	ns	2, 29, 34

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+max (4nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	ns	3,30, 34
DLL locking time	tDLLK	597	-	597	-	768	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-		50
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	nCK	33
Multi-Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	-	
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))						nCK	
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	UI	45,47
DQ0 or DQL0 driven to 0 hold time from last DQS falling edge	tPDA_H	0.5	-	0.5	-	0.5	-	UI	46,47
$\overline{CS}$ to Command Address Latency									
$\overline{CS}$ to Command Address Latency	tCAL	max(3 nCK,3.748 ns)	-	max(3 nCK,3.748 ns)	-	max(3 nCK,3.748 ns)	-	nCK	
Mode Register Set command cycle time in CAL mode	tMRD_tCAL	tMOD+tCAL	-	tMOD+tCAL	-	tMOD+tCAL	-	nCK	
Mode Register Set update delay in CALmode	tMOD_tCAL	tMOD+tCAL	-	tMOD+tCAL	-	tMOD+tCAL	-	nCK	
DRAM Data Timing									
DQS,$\overline{DQS}$ to DQ skew, per group, per access	tDQSQ	-	0.16	-	0.16	-	0.16	tCK(avg) /2	13,18, 39, 49
DQ output hold time per group, per access from DQS, $\overline{DQS}$	tQH	0.76	-	0.76	-	0.76	-	tCK(avg) /2	13,17,18 , 39, 49
Data Valid Window per device per UI:(tQH-tDQSQ) of each UI on a given DRAM	tDVWd	0.63	-	0.63	-	0.64	-	UI	17, 18 39, 49
Data Valid Window per pin per UI:(tQH - tDQSQ) each UI on a pin of a given DRAM	tDVWp	0.66	-	0.66	-	0.69	-	UI	17, 18 39, 49
DQ low impedance time from CK, $\overline{CK}$	tLZ(DQ)	-450	225	-390	195	-360	180	ps	39
DQ high impedance time from CK, $\overline{CK}$	tHZ(DQ)	-	225	-	195	-	180	ps	39
Data Strobe Timing									
DQS,$\overline{DQS}$ differential READ Preamble(1 clock preamble)	tRPRE	0.9	NOTE 44	0.9	NOTE 44	0.9	NOTE 44	tCK	40
DQS,$\overline{DQS}$ differential READ Preamble(2 clock preamble)	tRPRE2	NA	NA	NA	NA	NA	NA	tCK	41
DQS,$\overline{DQS}$ differential READ Postamble	tRPST	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	tCK	
DQS,$\overline{DQS}$ differential output high time	tQSH	0.4	-	0.4	-	0.4	-	tCK	21
DQS,$\overline{DQS}$ differential output low time	tQSL	0.4	-	0.4	-	0.4	-	tCK	20
DQS,$\overline{DQS}$ differential WRITE Preamble (1 clock preamble)	tWPRE	0.9	-	0.9	-	0.9	-	tCK	42
DQS,$\overline{DQS}$ differential WRITE Preamble (2 clock preamble)	tWPRE2	NA	-	NA	-	NA	-	tCK	43
DQS,$\overline{DQS}$ differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	tCK	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
DQS and $\overline{DQS}$ low-impedance time (Referenced from RL-1)	**tLZ(DQS)**	-450	225	-390	195	-360	180	ps	
DQS and $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	**tHZ(DQS)**	-	225	-	195	-	180	ps	
DQS,$\overline{DQS}$ differential input low pulse width	**tDQSL**	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS,$\overline{DQS}$ differential input high pulse width	**tDQSH**	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS,$\overline{DQS}$ rising edge to CK,$\overline{CK}$ rising edge (1 clock preamble)	**tDQSS**	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	42
DQS,$\overline{DQS}$ rising edge to CK,$\overline{CK}$ rising edge (2 clock preamble)	**tDQSS2**	NA	NA	NA	NA	NA	NA	tCK	43
DQS,$\overline{DQS}$ falling edge setup time to CK,$\overline{CK}$ rising edge	**tDSS**	0.18	-	0.18	-	0.18	-	tCK	
DQS,$\overline{DQS}$ falling edge hold time from CK,$\overline{CK}$ rising edge	**tDSH**	0.18	-	0.18	-	0.18	-	tCK	
DQS,$\overline{DQS}$rising edge output timing location from rising CK, $\overline{CK}$ with DLL On mode	**tDQSCK (DLL On)**	-225	225	-195	195	-180	180	ps	37,38,39
DQS, $\overline{DQS}$ rising edge output variance window per DRAM	**tDQSCKI (DLL On)**	-	370	-	330	-	310	ps	37,38,39
MPSM Timing									
Command path disable delay upon MPSM entry	**tMPED**	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-		
Valid clock requirement after MPSM entry	**tCKMPE**	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-		
Valid clock requirement before MPSM exit	**tCKMPX**	tCKSRX(min)		tCKSRX(min)		tCKSRX(min)			
Exit MPSM to commands not requiring a locked DLL	**tXMP**	tXS(min)	-	tXS(min)	-	tXS(min)	-		
Exit MPSM to commands requiring a locked DLL	**tXMPDLL**	tXMP(min) + tXSDLL(min)		tXMP(min) + tXSDLL(min)		tXMP(min) + tXSDLL(min)			
CS setup time to CKE	**tMPX_S**	tISmin + tIHmin	-	tISmin + tIHmin	-	tISmin + tIHmin	-		
Calibration Timing									
Power-up and RESET calibration time	**tZQinit**	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	**tZQoper**	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	**tZQCS**	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing									
Exit Reset from CKE HIGH to a valid command	**tXPR**	Max (5nCK,tRFC(min) +10ns)	-	Max (5nCK,tRFC(min) +10ns)	-	Max (5nCK,tRFC(min) +10ns)	-		
Exit Self Refresh to commands not requiring a locked DLL	**tXS**	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-		
SRX to commands not requiring a locked DLL in Self Refresh ABORT	**tXS_ABORT (min)**	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-		
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	**tXS_FAST (min)**	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-		

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-		
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+ 1nCK	-	tCKE(min)+ 1nCK	-	tCKE(min)+ 1nCK	-		
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max (5nCK,10ns)+PL	-	max (5nCK,10ns)+PL	-	max (5nCK,10ns)+PL	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-		
Power Down Timing									
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-		
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-		31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI		6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS,C4OTF)	tWRPDEN	WL+4+(tWR/tCK (avg))	-	WL+4+(tWR/tCK (avg))	-	WL+4+(tWR/tCK (avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS,BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRPBC4DEN	WL+2+(tWR/tCK (avg))	-	WL+2+(tWR/tCK (avg))	-	WL+2+(tWR/tCK (avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPBC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
PDA Timing									
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	nCK	
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD							
ODT Timing									
Asynchronous RTT turn-on delay (Power- Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power- Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Unit	Notes
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Write Leveling Timing									
First DQS/$\overline{DQS}$ rising edge after write leveling mode is programmed	**tWLMRD**	40	-	40	-	40	-	nCK	12
DQS/$\overline{DQS}$ delay after write leveling mode is programmed	**tWLDQSEN**	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK/$\overline{CK}$ crossing to rising DQS/$\overline{DQS}$ crossing	**tWLS**	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS/$\overline{DQS}$ crossing to rising CK/$\overline{CK}$ crossing	**tWLH**	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	**tWLO**	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	**tWLOE**							ns	
CA Parity Timing									
Commands not guaranteed to be executed during this time	**tPAR_UNKNOWN**	-	PL	-	PL	-	PL		
Delay from errant command to $\overline{ALERT}$ assertion	**tPAR_ALERT_ON**	-	PL+6ns	-	PL+6ns	-	PL+6ns		
Pulse width of $\overline{ALERT}$ signal when asserted	**tPAR_ALERT_PW**	48	96	56	112	64	128	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	**tPAR_ALERT_RSP**	-	43	-	50	-	57	nCK	
Parity Latency	**PL**	4		4		4		nCK	
CRC Error Reporting									
CRC error to $\overline{ALERT}$ latency	**tCRC_ALERT**	3	13	3	13	3	13	ns	
CRC $\overline{ALERT}$ pulse width	**CRC_ALERT_PW**	6	10	6	10	6	10	nCK	
tREFI									
tRFC1 (min)	**4Gb**	260	-	260	-	260	-	ns	34
tRFC2 (min)	**4Gb**	160	-	160	-	160	-	ns	34
tRFC4 (min)	**4Gb**	110	-	110	-	110	-	ns	34

Timing Parameter(Data rate 2400, 2666 specifications and conditions)

Speed		DDR4-2400		DDR4-2666		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max		
Clock Timing							
Minimum Clock Cycle Time (DLL off mode)	**tCK (DLL_OFF)**	8	20	8	20	ns	
Average Clock Period	**tCK(avg)**	Refer to "Speed Bin" section				ns	35,36
Average high pulse width	**tCH(avg)**	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	**tCL(avg)**	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	**tCK(abs)**	Min: tCK(avg)min+tJIT(per)min_tot Max: tCK(avg)max+ tJIT(per)max_tot				tCK(avg)	
Absolute clock HIGH pulse width	**tCH(abs)**	0.45	–	0.45	–	tCK(avg)	23
Absolute clock LOW pulse width	**tCL(abs)**	0.45	–	0.45	–	tCK(avg)	24
Clock Period Jitter- total	**JIT(per)_tot**	-42	42	-38	38	ps	25
Clock Period Jitter- deterministic	**JIT(per)_dj**	-21	21	-19	19	ps	26
Clock Period Jitter during DLL locking period	**tJIT(per, lck)**	-33	33	-30	30	ps	
Cycle to Cycle Period Jitter	**tJIT(cc)**	–	83	–	75	ps	
Cycle to Cycle Period Jitter during DLL locking period	**tJIT(cc, lck)**	–	67	–	60	ps	
Duty Cycle Jitter	**tJIT(duty)**	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	**tERR(2per)**	-61	61	-55	55	ps	
Cumulative error across 3 cycles	**tERR(3per)**	-73	73	-66	66	ps	
Cumulative error across 4 cycles	**tERR(4per)**	-81	81	-73	73	ps	
Cumulative error across 5 cycles	**tERR(5per)**	-87	87	-78	78	ps	
Cumulative error across 6 cycles	**tERR(6per)**	-92	92	-83	83	ps	
Cumulative error across 7 cycles	**tERR(7per)**	-97	97	-87	87	ps	
Cumulative error across 8 cycles	**tERR(8per)**	-101	101	-91	91	ps	
Cumulative error across 9 cycles	**tERR(9per)**	-104	104	-94	94	ps	
Cumulative error across 10 cycles	**tERR(10per)**	-107	107	-96	96	ps	
Cumulative error across 11 cycles	**tERR(11per)**	-110	110	-99	99	ps	
Cumulative error across 12 cycles	**tERR(12per)**	-112	112	-101	101	ps	
Cumulative error across 13 cycles	**tERR(13per)**	-114	114	-103	103	ps	
Cumulative error across 14 cycles	**tERR(14per)**	-116	116	-104	104	ps	
Cumulative error across 15 cycles	**tERR(15per)**	-118	118	-106	106	ps	
Cumulative error across 16 cycles	**tERR(16per)**	-120	120	-108	108	ps	
Cumulative error across 17 cycles	**tERR(17per)**	-122	122	-110	110	ps	
Cumulative error across 18 cycles	**tERR(18per)**	-124	124	-112	112	ps	
Cumulative error across n = 13, 14 . . .49, 50 cycles	**tERR(nper)**	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)				ps	
Command and Address setup time to CK,$\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	**tIS(base)**	62	–	55	–	ps	

Speed		DDR4-2400		DDR4-2666		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max		
Command and Address setup time to CK,$\overline{CK}$ referenced to Vref levels	**tIS(Vref)**	162	–	145	–	ps	
Command and Address hold time to CK,$\overline{CK}$ referenced to Vih(dc) / Vil(dc) levels	**tIH(base)**	87	–	80	–	ps	
Command and Address hold time to CK,$\overline{CK}$ referenced to Vref levels	**tIH(Vref)**	162	–	145	–	ps	
Control and Address Input pulse width for each input	**tIPW**	410	–	385	–	ps	
Command and Address Timing							
$\overline{CAS}$ to $\overline{CAS}$ command delay for same bank group	**tCCD_L**	max (5 nCK, 5 ns)	–	max (5 nCK, 5 ns)	–	nCK	34
$\overline{CAS}$ to $\overline{CAS}$ command delay for different bank group	**tCCD_S**	4	–	4	–	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	**tRRD_S(2K)**	Max(4nCK, 5.3ns)	–	Max(4nCK, 5.3ns)	–	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	**tRRD_S(1K)**	Max(4nCK, 3.3ns)	–	Max(4nCK, 3ns)	–	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	**tRRD_S(1/2K)**	Max(4nCK,3.3ns)	–	Max(4nCK, 3ns)	–	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	**tRRD_L(2K)**	Max(4nCK, 6.4ns)	–	Max(4nCK, 6.4ns)	–	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	**tRRD_L(1K)**	Max(4nCK, 4.9ns)	–	Max(4nCK, 4.9ns)	–	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	**tRRD_L(1/2K)**	Max(4nCK, 4.9ns)	–	Max(4nCK, 4.9ns)	–	nCK	34
Four activate window for 2KB page size	**tFAW_2K**	Max(28nCK,30ns)	–	Max(28nCK,30ns)	–	ns	34
Four activate window for 1KB page size	**tFAW_1K**	Max(20nCK ,21ns)	-	Max(20nCK,21ns)	-	ns	34
Four activate window for 1/2KB page size	**tFAW_1/2K**	Max(16nCK,13ns)	–	Max(16nCK,12ns)	–	ns	34
Delay from start of internal write transaction to internal read command for different bank group	**tWTR_S**	max (2nCK, 2.5ns)	–	max (2nCK, 2.5ns)	–	ns	1,2,e,34
Delay from start of internal write transaction to internal read command for same bank group	**tWTR_L**	max (4nCK,7.5ns)	–	max (4nCK,7.5ns)	–	ns	1,34
Internal READ Command to PRECHARGE Command delay	**tRTP**	max (4nCK,7.5ns)	–	max (4nCK,7.5ns)	–		34
WRITE recovery time	**tWR**	15	–	15	–		1
Write recovery time when CRC and DM are enabled	**tWR_CRC_DM**	tWR+max(5nCK,3.75ns)	–	tWR+max(5nCK,3.75ns)	–	ns	1, 28

Speed		DDR4-2400		DDR4-2666		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max		
Command and Address Timing							
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	**tWTR_S_CRC_DM**	tWTR_S+ max(5nCK, 3.75ns)	–	tWTR_S+ max(5nCK, 3.75ns)	–	ns	2, 29,34
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	**tWTR_L_CRC_DM**	tWTR_L+ max(5nCK, 3.75ns)	–	tWTR_L+ max(5nCK, 3.75ns)	–	ns	3, 30,34
DLL locking time	**tDLLK**	768	–	1024	–	ns	
Mode Register Set command cycle time	**tMRD**	8	–	8	–	nCK	
Mode Register Set command update delay	**tMOD**	max(24nCK, 15ns)	–	max(24nCK, 15ns)	–	nCK	50
Multi-Purpose Register Recovery Time	**tMPRR**	1	–	1	–	nCK	33
Multi-Purpose Register Write Recovery Time	**tWR_MPR**	tMOD (min) + AL + PL	–	tMOD (min) + AL + PL	–	nCK	
Auto precharge write recovery + precharge time	**tDAL(min)**	Programmed WR + roundup (tRP / tCK(avg))				nCK	
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	**tPDA_S**	0.5	–	0.5	–	UI	45,47
DQ0 or DQL0 driven to 0 hold time from last DQS falling edge	**tPDA_H**	0.5	–	0.5	–	UI	46,47
$\overline{CS}$ to Command Address Latency							
$\overline{CS}$ to Command Address Latency	**tCAL**	max (3 nCK, 3.748 ns)	–	max (3 nCK, 3.748 ns)	–	nCK	
Mode Register Set command cycle time in CAL mode	**tMRD_tCAL**	tMOD+ tCAL	–	tMOD+ tCAL	–	nCK	
Mode Register Set update delay in CALmode	**tMOD_tCAL**	tMOD+ tCAL	–	tMOD+ tCAL	–	nCK	
DRAM Data Timing							
DQS,$\overline{DQS}$ to DQ skew, per group, per access	**tDQSQ**	–	0.17	–	0.18	tCK(avg)/2	13,18, 39,49
DQ output hold time per group, per access from DQS, $\overline{DQS}$	**tQH**	0.74	–	0.74	–	tCK(avg)/2	13,17,18 ,39,49
Data Valid Window per device per UI:(tQH-tDQSQ) of each UI on a given DRAM	**tDVWd**	0.64	–	TBD	–	UI	17,18, 39, 49
Data Valid Window per pin per UI:(tQH - tDQSQ) each UI on a pin of a given DRAM	**tDVWp**	0.72	–	0.72	–	UI	17,18, 39, 49
DQ low impedance time from CK, $\overline{CK}$	**tLZ(DQ)**	-330	175	-310	170	ps	39
DQ high impedance time from CK, $\overline{CK}$	**tHZ(DQ)**	–	175	–	170	ps	39
Data Strobe Timing							
DQS,$\overline{DQS}$ differential READ Preamble(1 clock preamble)	**tRPRE**	0.9	NOTE 44	0.9	NOTE 44	tCK	39, 40
DQS,$\overline{DQS}$ differential READ Preamble(2 clock preamble)	**tRPRE2**	1.8	NOTE 44	1.8	NOTE 44	tCK	39, 41
DQS,$\overline{DQS}$ differential READ Postamble	**tRPST**	0.33	NOTE 45	0.33	NOTE 45	tCK	39
DQS,$\overline{DQS}$ differential output high time	**tQSH**	0.4	–	0.4	–	tCK	21, 39
DQS,$\overline{DQS}$ differential output low time	**tQSL**	0.4	–	0.4	–	tCK	20, 39

Speed		DDR4-2400		DDR4-2666		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max		
Data Strobe Timing							
DQS,$\overline{DQS}$ differential WRITE Preamble (1 clock preamble)	**tWPRE**	0.9	–	0.9	–	tCK	42
DQS,$\overline{DQS}$ differential WRITE Preamble (2 clock preamble)	**tWPRE2**	1.8	–	1.8	–	tCK	43
DQS,$\overline{DQS}$ differential WRITE Postamble	**tWPST**	0.33	–	0.33	–	tCK	
DQS and $\overline{DQS}$ low-impedance time (Referenced from RL-1)	**tLZ(DQS)**	-330	175	-310	170	ps	39
DQS and $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	**tHZ(DQS)**	–	175	–	170	ps	39
DQS,$\overline{DQS}$ differential input low pulse width	**tDQSL**	0.46	0.54	0.46	0.54	tCK	
DQS,$\overline{DQS}$ differential input high pulse width	**tDQSH**	0.46	0.54	0.46	0.54	tCK	
DQS,$\overline{DQS}$ rising edge to CK,$\overline{CK}$ rising edge (1 clock preamble)	**tDQSS**	-0.27	0.27	-0.27	0.27	tCK	42
DQS,$\overline{DQS}$ rising edge to CK,$\overline{CK}$ rising edge (2 clock preamble)	**tDQSS2**	TBD	TBD	TBD	TBD	tCK	43
DQS,$\overline{DQS}$ falling edge setup time to CK,$\overline{CK}$ rising edge	**tDSS**	0.18	–	0.18	–	tCK	
DQS,$\overline{DQS}$ falling edge hold time from CK,$\overline{CK}$ rising edge	**tDSH**	0.18	–	0.18	–	tCK	
DQS,$\overline{DQS}$rising edge output timing location from rising CK, $\overline{CK}$ with DLL On mode	**tDQSCK (DLL On)**	-175	175	-170	170	ps	37,38, 39
DQS, $\overline{DQS}$ rising edge output variance window per DRAM	**tDQSCKI (DLL On)**	–	290	–	270	ps	37,38, 39
MPSM Timing							
Command path disable delay upon MPSM entry	**tMPED**	tMOD(min) +tCPDED(min)	–	tMOD(min) +tCPDED(min)	–		
Valid clock requirement after MPSM entry	**tCKMPE**	tMOD(min) +tCPDED(min)	–	tMOD(min) +tCPDED(min)	–		
Valid clock requirement before MPSM exit	**tCKMPX**	tCKSRX(min)	–	tCKSRX(min)	–		
Exit MPSM to commands not requiring a locked DLL	**tXMP**	tXS(min)	–	tXS(min)	–		
Exit MPSM to commands requiring a locked DLL	**tXMPDLL**	tXMP(min) +tXSDLL(min)	–	tXMP(min) +tXSDLL(min)	–		
CS setup time to CKE	**tMPX_S**	tISmin+tIHmin	–	tISmin+tIHmin	–		
Calibration Timing							
Power-up and RESET calibration time	**tZQinit**	1024	–	1024	–	nCK	
Normal operation Full calibration time	**tZQoper**	512	–	512	–	nCK	
Normal operation Short calibration time	**tZQCS**	128	–	128	–	nCK	

Speed		DDR4-2400		DDR4-2666		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max		
Reset/Self Refresh Timing							
Exit Reset from CKE HIGH to a valid command	**tXPR**	Max (5nCK,tRFC(min)+10ns)	–	Max (5nCK,tRFC(min)+10ns)	–	nCK	
Exit Self Refresh to commands not requiring a locked DLL	**tXS**	tRFC(min)+ 10ns	–	tRFC(min)+ 10ns	–	nCK	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	**tXS_ABORT(min)**	tRFC4(min)+10ns	–	tRFC4(min)+10ns	–	nCK	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	**tXS_FAST(min)**	tRFC4(min)+10ns	–	tRFC4(min)+10ns	–	nCK	
Exit Self Refresh to commands requiring a locked DLL	**tXSDLL**	tDLLK(min)	–	tDLLK(min)	–	nCK	
Minimum CKE low width for Self refresh entry to exit timing	**tCKESR**	tCKE(min)+ 1nCK	–	tCKE(min)+ 1nCK	–	nCK	
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	**tCKESR_PAR**	tCKE(min)+ 1nCK+PL	–	tCKE(min)+ 1nCK+PL	–	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	**tCKSRE**	max (5nCK,10ns)	–	max (5nCK,10ns)	–	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	**tCKSRE_PAR**	max (5nCK,10ns)+PL	–	max (5nCK,10ns)+PL	–	nCK	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	**tCKSRX**	max (5nCK,10ns)	–	max (5nCK,10ns)	–	nCK	
Power Down Timing							
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	**tXP**	max (4nCK,6ns)	–	max (4nCK,6ns)	–	nCK	
CKE minimum pulse width	**tCKE**	max (3nCK, 5ns)	–	max (3nCK, 5ns)	–	nCK	31,32
Command pass disable delay	**tCPDED**	4	–	4	–	nCK	
Power Down Entry to Exit Timing	**tPD**	tCKE(min)	9xtREFI	tCKE(min)	9xtREFI	nCK	6
Timing of ACT command to Power Down entry	**tACTPDEN**	2	–	2	–	nCK	7
Timing of PRE or PREA command to Power Down entry	**tPRPDEN**	2	–	2	–	nCK	7
Timing of RD/RDA command to Power Down entry	**tRDPDEN**	RL+4+1	–	RL+4+1	–	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS,C4OTF)	**tWRPDEN**	WL+4+(tWR/tCK(avg))	–	WL+4+(tWR/tCK(avg))	–	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS,BC4OTF)	**tWRAPDEN**	WL+4+WR+1	–	WL+4+WR+1	–	nCK	5

Speed		DDR4-2400		DDR4-2666		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max		
Timing of WR command to Power Down entry (BC4MRS)	tWRPBC4DEN	WL+2+(tWR/tCK(avg))	–	WL+2+(tWR/tCK(avg))	–	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPBC4DEN	WL+2+WR+1	–	WL+2+WR+1	–	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	2	–	2	–	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	–	tMOD(min)	–	nCK	
PDA Timing							
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max (16nCK, 10ns)	–	max (16nCK, 10ns)	–	nCK	
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD				nCK	
ODT Timing							
Asynchronous RTT turn-on delay (Power- Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power- Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.28	0.72	tCK(avg)	
Write Leveling Timing							
First DQS/$\overline{DQS}$ rising edge after write leveling mode is programmed	tWLMRD	40	–	40	–	nCK	12
DQS/$\overline{DQS}$ delay after write leveling mode is programmed	tWLDQSEN	25	–	25	–	nCK	12
Write leveling setup time from rising CK/$\overline{CK}$ crossing to rising DQS/$\overline{DQS}$ crossing	tWLS	0.13	–	0.13	–	tCK(avg)	
Write leveling hold time from rising DQS/$\overline{DQS}$ crossing to rising CK/$\overline{CK}$ crossing	tWLH	0.13	–	0.13	–	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE	0	2	0	2	ns	
CA Parity Timing							
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	–	PL	–	PL	nCK	
Delay from errant command to $\overline{ALERT}$ assertion	tPAR_ALERT_ON	–	PL+6ns	–	PL+6ns	nCK	
Pulse width of $\overline{ALERT}$ signal when asserted	tPAR_ALERT_PW	72	144	80	160	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	–	64	–	71	nCK	
Parity Latency	PL	5		5		nCK	
CRC Error Reporting							
CRC error to $\overline{ALERT}$ latency	tCRC_ALERT	3	13	3	13	ns	
CRC $\overline{ALERT}$ pulse width	CRC_ALERT_PW	6	10	6	10	nCK	

Speed		DDR4-2400		DDR4-2666		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max		
Geardown timing							
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	**tXPR_GEAR**	–	–	tXPR	–		
CKE High Assert to Gear Down Enable time(T2/CKE)	**tXS_GEAR**	–	–	tXS	–		
MRS command to Sync pulse time(T3)	**tSYNC_GEAR**	–	–	tMOD+4nCK	–		27
Sync pulse to First valid command(T4)	**tCMD_GEAR**	–		tMOD			27
Geardown setup time	**tGEAR_setup**	–	–	2	–	nCK	27
Geardown hold time	**tGEAR_hold**	–	–	2	–	nCK	
tREFI							
tRFC1 (min)	**4Gb**	260	–	260	–	ns	34
tRFC2 (min)	**4Gb**	160	–	160	–	ns	34
tRFC4 (min)	**4Gb**	110	–	110	–	ns	34

NOTE 1 Start of internal write transaction is defined as follows: For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL. For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL. For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.

NOTE 2 A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled.

NOTE 3 Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.

NOTE 4 tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.

NOTE 5 WR in clock cycles as programmed in MR0.

NOTE 6 tREFI depends on TOPER.

NOTE 7 CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.

NOTE 8 For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied

NOTE 9 When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.

NOTE 10 When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.

NOTE 11 When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.

NOTE 12 The max values are system dependent.

NOTE 13 DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are TBD.

NOTE 14 The deterministic component of the total timing. Measurement method TBD.

NOTE 15 DQ to DQ static offset relative to strobe per group. Measurement method TBD.

NOTE 16 This parameter will be characterized and guaranteed by design.

NOTE 17 When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example TBD.

NOTE 18 DRAM DBI mode is off.

NOTE 19 DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.

NOTE 20 tQSL describes the instantaneous differential output low pulse width on DQS - $\overline{\text{DQS}}$, as measured from on falling edge to the next consecutive rising edge.

NOTE 21 tQSH describes the instantaneous differential output high pulse width on DQS - $\overline{\text{DQS}}$, as measured from on falling edge to the next consecutive rising edge.

NOTE 22 There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI.

NOTE 23 tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

NOTE 24 tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

NOTE 25 Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are TBD.

NOTE 26 The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.

NOTE 27 This parameter has to be even number of clocks.

NOTE 28 When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.

NOTE 29 When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.

NOTE 30 When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.

NOTE 31 After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).

NOTE 32 After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).

NOTE 33 Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.

NOTE 34 Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.

NOTE 35 This parameter must keep consistency with Speed-Bin Tables.

NOTE 36 DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.

NOTE 37 applied when DRAM is in DLL ON mode.

NOTE 38 Assume no jitter on input clock signals to the DRAM

NOTE 39 Value is only valid for RONNOM = 34 ohms

NOTE 40 1tCK toggle mode with setting MR4:A11 to 0

NOTE 41 2tCK toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2400/2666 speed grade.

NOTE 42 1tCK mode with setting MR4:A12 to 0

NOTE 43 2tCK mode with setting MR4:A12 to 1, which is valid for DDR4-2400/2666 speed grade.

NOTE 44 The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side. See Clock to Data Strobe Rela-tionship --- “Clock to Data Strobe Relationship”. Boundary of DQS Low-Z occur one cycle earlier in 2tCK toggle mode which is illustrated in Read Preamble ---- “Read Preamble”.

NOTE 45 DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point

NOTE 46 last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High

NOTE 47 VrefDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.

NOTE 48 The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See Clock to Data Strobe Relationship

NOTE 49 Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately 0.7 * VDDQ as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to VTT = VDDQ

NOTE 50 For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.

Rounding Algorithms

Software algorithms for calculation of timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 933.33... MHz, or a clock period of 1.0714... ns. Similarly, a system with a memory clock frequency of 1066.66... MHz yields mathematically a clock period of 0.9375... ns. In most cases, it is impossible to express all digits after the decimal point exactly, and rounding must be done because the DDR4 SDRAM specification establishes a minimum granularity for timing parameters of 1 ps.

Rules for rounding must be defined to allow optimization of device performance without violating device parameters. These algorithms rely on results that are within correction factors on device testing and specification to avoid losing performance due to rounding errors.

These rules are:

•Clock periods such as tCKAVGmin are defined to 1 ps of accuracy; for example, 0.9375... ns is defined as 937 ps and 1.0714... ns is defined as 1071 ps.

•Using real math, parameters like tAAmin, tRCDmin, etc. which are programmed in systems in numbers of clocks (nCK) but expressed in units of time (in ns) are divided by the clock period (in ns) yielding a unitless ratio, a correction factor of 2.5% is subtracted, then the result is set to the next higher integer number of clocks:

nCK = ceiling [(parameter_in_ns / application_tCK_in_ns) - 0.025]

•Alternatively, programmers may prefer to use integer math instead of real math by expressing timing in ps, scaling the desired parameter value by 1000, dividing by the application clock period, adding an inverse correction factor of 97.4%, dividing the result by 1000, then truncating down to the next lower integer value:

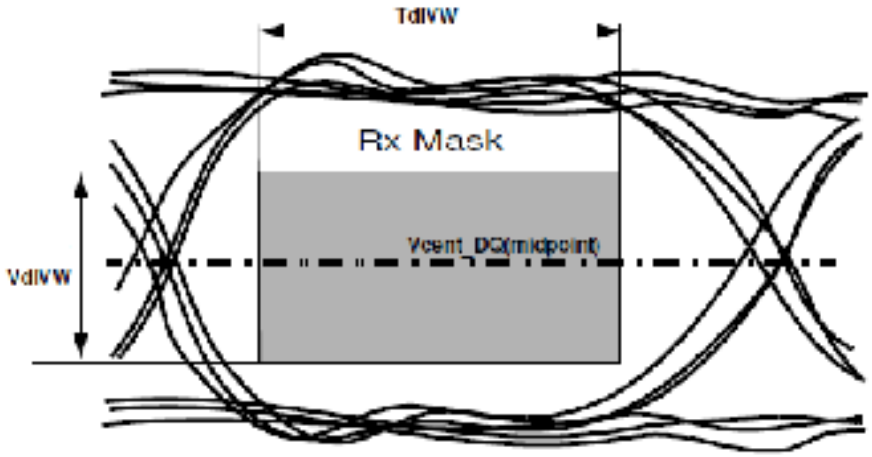
nCK = truncate [{(parameter_in_ps x 1000) / (application_tCK_in_ps) + 974} / 1000]

•Either algorithm yields identical results. In case of conflict between results, the preferred algorithm is the integer math algorithm. This algorithm applies to all timing parameters documented in a Serial Presence Detect(SPD) when converting from ns to nCK. Other timing parameters may use a simpler algorithm nCK = ceiling (parameter_in_ns ÷ application_tCK_in_ns).

The DQ input receiver compliance mask for voltage and timing

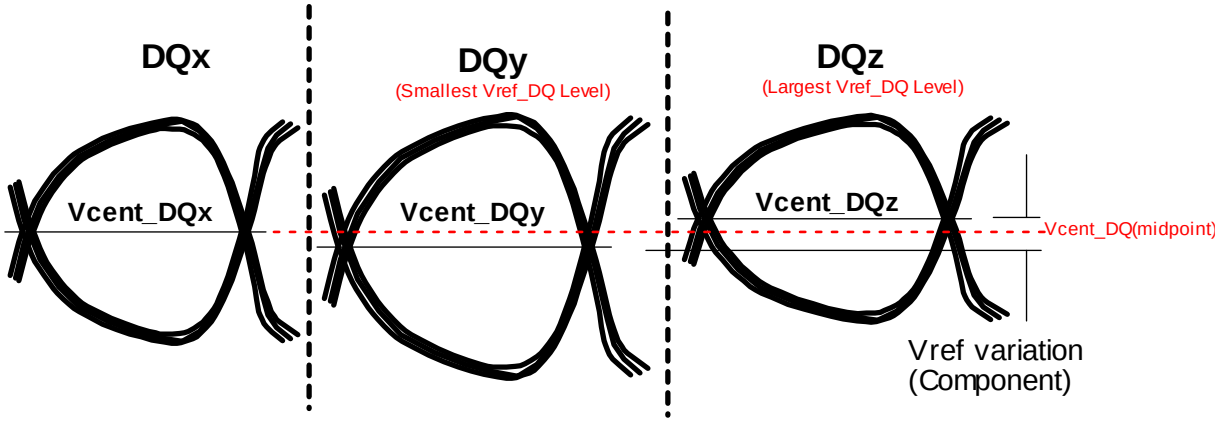
The DQ input receiver uses a compliance mask (Rx) for voltage and timing as shown in the figure below. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal with BER of 1e-16; any input signal encroaching within the Rx Mask is subject to being invalid data. The Rx Mask is the receiver property for each DQ input pin and it is not the valid data-eye.

DQ Receiver(Rx) compliance mask



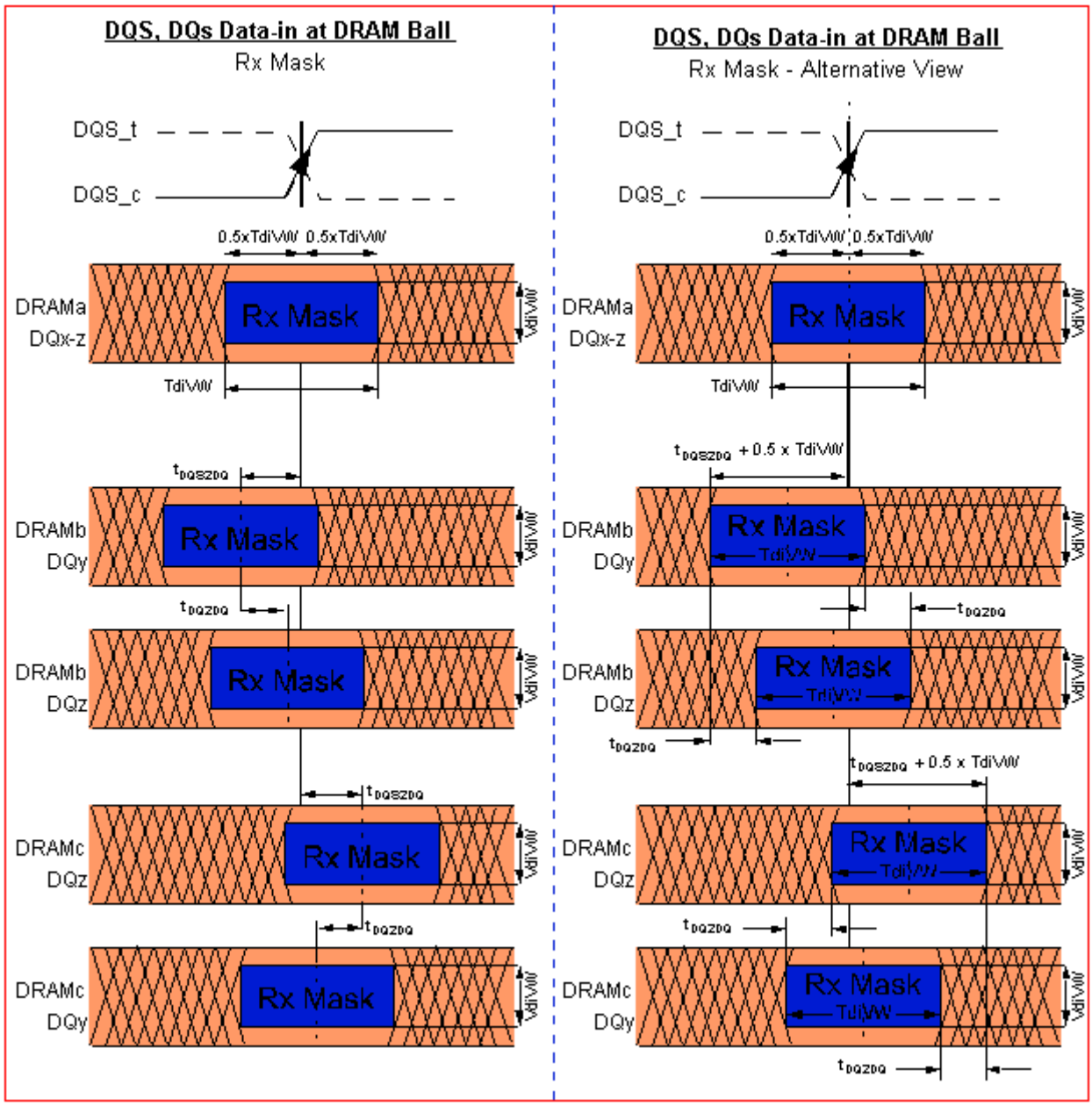
Vcent_DQ Variation to Vcent_DQ(midpoint)

The Vref_DQ voltage is an internal reference voltage level that shall be set to the properly trained setting, which is generally Vcent_DQ(midpoint), in order to have valid Rx Mask values.



Vcent_DQ(midpoint) is defined as the midpoint between the largest V_{REFDQ} voltage level and the smallest V_{REFDQ} voltage level across all DQ pins for a given DRAM. Each DQ pin's V_{REFDQ} is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in below. This means a DRAM's level variation is accounted for within the DRAM Rx mask. The DRAM V_{REFDQ} level will be set by the system to account for Ron and ODT settings.

DQS to DQ and DQ to DQ Timings at DRAM Balls



NOTE :

DQx represents an optimally centered mask

DQy represents earliest valid mask.

DQz represents latest valid mask.

DRAMa represents a DRAM without any DQS/DQ skews.

DRAMb represents a DRAM with early skews (negative tDQS2DQ).

DRAMc represents a DRAM with delayed skews (positive tDQS2DQ).

Figures show skew allowed between DRAM to DRAM and DQ to DQ for a DRAM. Signals assume data centered aligned at DRAM Latch. TdiPW is not shown; composite data-eyes shown would violate TdiPW.VCENT DQ(midpoint) is not shown but is assummed to be midpoint of VdiVW.

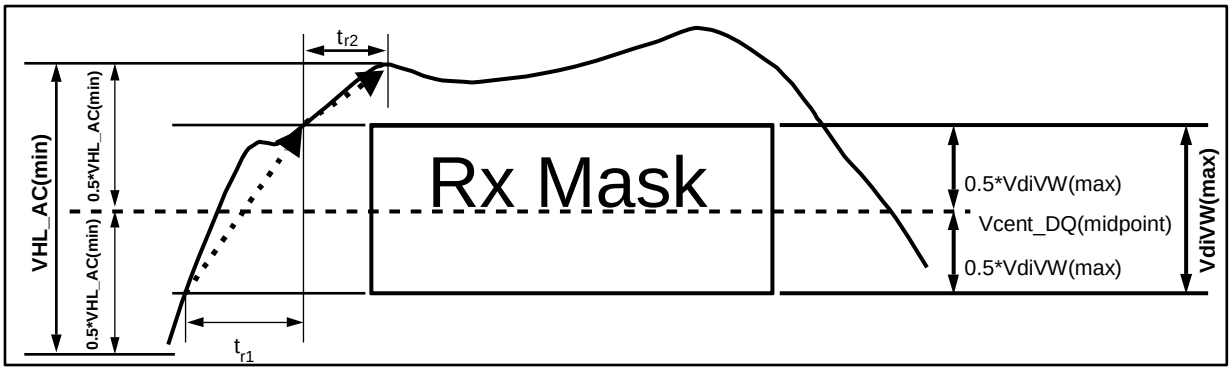
Slew Rate Conditions for Rising Transition

The rising edge slew rates are defined by srr1 and srr2. The slew rate measurement points for a rising edge are shown in below: A low to high transition tr1 is measured from 0.5*VdiVW(max) below Vcent_DQ(midpoint) to the last transition through 0.5*VdiVW(max) above Vcent_DQ(midpoint) while tr2 is measured from the last transition through 0.5*VdiVW(max) above Vcent_DQ(midpoint) to the first transition through the 0.5*VIHL_AC(min) above Vcent_DQ(midpoint).

Rising edge slew rate equations:

srr1 = VdIVW(max) / tr1

*srr2 = (VIHL_AC(min) – VdIVW(max)) / (2*tr2)*



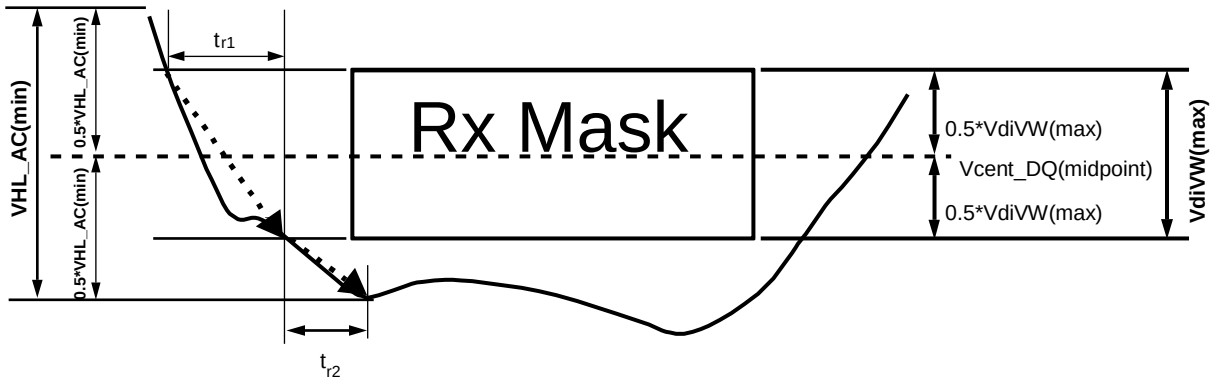
Slew Rate Conditions for Falling Transition

The falling edge slew rates are defined by srf1 and srf2. The slew rate measurement points for a falling edge are shown in below: A high to low transition tf1 is measured from 0.5*VdiVW(max) above Vcent_DQ(midpoint) to the last transition through 0.5*VdiVW(max) below Vcent_DQ(midpoint) while tf2 is measured from the last transition through 0.5*VdiVW(max) below Vcent_DQ(midpoint) to the first transition through the 0.5*VIHL_AC(min) below Vcent_DQ (pin mid).

Falling edge slew rate equations:

srf1 = VdIVW(max) / tf1

*srf2 = (VIHL_AC(min) – VdIVW(max)) / (2*tf2)*



DRAM DQs in Receive Mode

Symbol	Parameter	DDR4-1600/ 1866/2133		DDR4-2400		DDR4-2666		Unit	Notes
		Min	Max	Min	Max	Min	Max		
VdIVW	Rx Mask voltage - pk-pk	–	136	–	130	–	120	mV	1,2,10
TdIVW	Rx timing window	–	0.2	–	0.2	–	0.22	UI	1,2,10
VIHL_AC	DQ AC input swing pk-pk	186	–	160	–	150		mV	3,4,10
TdIPW	DQ input pulse width	0.58	–	0.58	–	0.58	–	UI	5,10
tDQS2DQ	Rx Mask DQS to DQ offset	-0.17	0.17	-0.17	0.17	-0.19	0.19	UI	6,10
tDQ2DQ	Rx Mask DQ to DQ offset	–	TBD	–	TBD	–	0.105	UI	7
srr1, srf1	Input Slew Rate over Vdlvw if tCK >=0.937ns	1.0	9	1.0	9	1.0	9	V/ns	8,10
	Input Slew Rate over Vdivw if 0.937ns>tCK>=0.625ns	–	–	1.25	9	1.25	9	V/ns	8,10
srr2	Rising Input Slew Rate over 1/2 VIHL_AC	0.2*srr1	9	0.2*srr1	9	0.2*srr1	9	V/ns	9,10
srf2	Falling Input Slew Rate over 1/2 VIHL_AC	0.2*srf1	9	0.2*srf1	9	0.2*srf1	9	V/ns	9,10

UI=TCK(avg)min/2

NOTE 1 Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent_DQ (midpoint) after VrefDQ training is completed. The data Rx mask is applied per bit and should include voltage and temperature drift terms. The input buffer design specification is to achieve at least a BER = e-16 when the RxMask is not violated The BER will be characterized and extrapolated if necessary using a dual dirac method from a higher BER(tbd).

NOTE 2 Defined over the DQ internal Vref range 1.

NOTE 3 Overshoot and Undershoot Specifications see AC overshoot/undershoot specification

NOTE 4 DQ input pulse signal swing into the receiver must meet or exceed VIHL AC(min). VIHL_AC(min) is to be achieved on an UI basis when a rising and falling edge occur in the same UI, i.e. a valid TdiPW.

NOTE 5 DQ minimum input pulse width defined at the Vcent_DQ(midpoint).

NOTE 6 DQS to DQ offset is skew between DQS and DQs within a nibble (x4) or word (x8, x16) at the DDR4 SDRAM balls over process, voltage, and temperature.

NOTE 7 DQ to DQ offset is skew between DQs within a nibble (x4) or word (x8, x16) at the DDR4 SDRAM balls for a given component over process, voltage, and temperature.

NOTE 8 Input slew rate over VdIVW Mask centered at Vcent_DQ(midpoint). Slowest DQ slew rate to fastest DQ slew rate per transition edge must be within 1.7 V/ns of each other.

NOTE 9 Input slew rate between VdIVW Mask edge and VIHL_AC(min) points.

NOTE 10 All Rx Mask specifications must be satisfied for each UI. For example, if the minimum input pulse width is violated when satisfying TdiVW(min), VdiVW(max), and minimum slew rate limits, then either TdiVW(min) or minimum slew rates would have to be increased to the point where the minimum input pulse width would no longer be violated.

Command, Control, and Address Setup, Hold, and Derating

The total tIS (setup time) and tIH (hold time) required is calculated to account for slew rate variation by adding the data sheet tIS (base) values, the VIL(AC)/VIH(AC) points, and tIH (base) values, the VIL(DC)/VIH(DC) points; to the ΔtIS and ΔtIH derating values, respectively. The base values are derived with single-end signals at 1V/ns and differential clock at 2V/ns. Example: tIS (total setup time) = tIS (base) + ΔtIS. For a valid transition, the input signal has to remain above/below VIH(AC)/VIL(AC) for the time defined by tVAC.

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached VIH(AC)/VIL(AC) at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach VIH(AC)/VIL(AC). For slew rates that fall between the values listed in derating tables, the derating values may be obtained by linear interpolation.

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VIH(AC)min that does not ring back below VIH(DC)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VIL(AC)max that does not ring back above VIL(DC)max.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VIH(AC)min that does not ring back below VIH(DC)min. Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VIL(AC)min that does not ring back above VIL(DC)max.

Command, Address, Control Setup and Hold Values

DDR4	1600	1866	2133	2400	2666	Unit	Reference
tIS(base, AC100)	115	100	80	62	-	ps	VIH/L(ac)
tIH(base, DC75)	140	125	105	87	-	ps	VIH/L(dc)
tIS(base, AC 90)	-	-	-	-	55	ps	VIH/L(ac)
tIH(base, DC 65)	-	-	-	-	80	ps	VIH/L(dc)
tIS/tIH @ VREF	215	200	180	162	145	ps	

NOTE 1 Base ac/dc referenced for 1V/ns slew rate and 2 V/ns clock slew rate.
NOTE 2 Values listed are referenced only; applicable limits are defined elsewhere.

Command, Address, Control Input Voltage Values

DDR4	1600	1866	2133	2400	2666	Unit	Reference
VIH.CA(AC)min	100	100	100	100	90	mV	VIH/L(ac)
VIH.CA(DC)min	75	75	75	75	65	mV	VIH/L(dc)
VIL.CA(DC)max	-75	-75	-75	-75	-65	mV	VIH/L(ac)
VIL.CA(AC)max	-100	-100	-100	-100	-90	mV	VIH/L(dc)

NOTE 1 Command, Address, Control input levels relative to VREFCA.
NOTE 2 Values listed are referenced only; applicable limits are defined elsewhere.

Derating values DDR4-1600/1866/2133/2400 tIS/tIH - ac/dc based

ΔtIS, ΔIH derating in [ps] AC/DC based [1]																
		CK, $\overline{CK}$ Differential Slew Rate														
		10.0 V/ns		8.0 V/ns		6.0 V/ns		4.0 V/ns		3.0V/ns		2.0V/ns		1.5 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD, ADDR, CNTL Input Slew rate V/ns	7.0	76	54	76	55	77	56	79	58	82	60	86	64	94	73	111	89
	6.0	73	53	74	53	75	54	77	56	79	58	83	63	92	71	108	88
	5.0	70	50	71	51	72	52	74	54	76	56	80	60	88	68	105	85
	4.0	65	46	66	47	67	48	69	50	71	52	75	56	83	65	100	81
	3.0	57	40	57	41	58	42	60	44	63	46	67	50	75	58	92	75
	2.0	40	28	41	28	42	29	44	31	46	33	50	38	58	46	75	63
	1.5	23	15	24	16	25	17	27	19	29	21	33	25	42	33	58	50
	1.0	-10	-10	-9	-9	-8	-8	-6	-6	-4	-4	0	0	8	8	25	25
	0.9	-17	-14	-16	-14	-15	-13	-13	-10	-11	-8	-7	-4	1	4	18	21
	0.8	-26	-19	-25	-19	-24	-18	-22	-16	-20	-14	-16	-9	-7	-1	9	16
	0.7	-37	-26	-36	-25	-35	-24	-33	-22	-31	-20	-27	-16	-18	-8	-2	9
	0.6	-52	-35	-51	-34	-50	-33	-48	-31	-46	-29	-42	-25	-33	-17	-17	-0
	0.5	-73	-48	-72	-47	-71	-46	-69	-44	-67	-42	-63	-38	-54	-29	-38	-13
	0.4	104	-66	-103	-66	-102	-65	-100	-63	-98	-60	-94	-56	-85	-48	-69	-31

NOTE 1 VIH/L(ac) = +/-100mV, VIH/L(dc) = +/-75mV; relative to VREFCA

Derating values DDR4-2666 tIS/tIH - ac/dc based

ΔtIS, ΔIH derating in [ps] AC/DC based [1]																
		CK, $\overline{CK}$ Differential Slew Rate														
		10.0 V/ns		8.0 V/ns		6.0 V/ns		4.0 V/ns		3.0V/ns		2.0V/ns		1.5 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD, ADDR, CNTL Input Slew rate V/ns	7.0	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd
	6.0	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd
	5.0	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd
	4.0	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd
	3.0	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd
	2.0	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd
	1.5	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd
	1.0	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	0	0	tbd	tbd	tbd	tbd
	0.9	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd
	0.8	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd
	0.7	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd
	0.6	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd
	0.5	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd
	0.4	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd

NOTE 1 VIH/L(ac) = +/-tbd mV, VIH/L(dc) = +/- tbd mV; relative to VREFCA

DDR4 Function Matrix

Function Matrix by Organization (V:Supported, Blank:Not supported)

Functions	X4	X8	X16
Write Leveling	V	V	V
Temperature controlled Refresh	V	V	V
Low Power Auto Self Refresh	V	V	V
Fine Granularity Refresh	V	V	V
Multi-Purpose Register	V	V	V
Data Mask		V	V
Data Bus Inversion		V	V
TDQS		V	
ZQ calibration	V	V	V
DQ Vref Training	V	V	V
Per DRAM Addressability	V	V	V
Mode Register Readout	V	V	V
CAL	V	V	V
WRITE CRC	V	V	V
CA Parity	V	V	V
Control Gear Down Mode	V	V	V
Programmable Preamble	V	V	V
Maximum Power Down Mode	V	V	
Boundary Scan Mode (Connectivity Test Mode)			V
Additive Latency	V	V	

Function Matrix by Speed (V:Supported, Blank:Not supported)

Functions	DLL off Mode	DLL on Mode		
	equal or slower than 250Mbps	DDR4-1600/1866/2133	DDR4-2400	DDR4-2666
Write Leveling	V	V	V	V
Temperature controlled Refresh	V	V	V	V
Low Power Auto Self Refresh	V	V	V	V
Fine Granularity Refresh	V	V	V	V
Multi-Purpose Register	V	V	V	V
Data Mask	V	V	V	V
Data Bus Inversion	V	V	V	V
TDQS		V	V	V
ZQ calibration	V	V	V	V
DQ Vref Training	V	V	V	V
Per DRAM Addressability		V	V	V
Mode Register Readout	V	V	V	V
CAL		V	V	V
WRITE CRC		V	V	V
CA Parity		V	V	V
Control Gear Down Mode				V
Programmable Preamble (= 2tCK)			V	V
Maximum Power Down Mode		V	V	V
Boundary Scan Mode (Connectivity Test Mode)	V	V	V	V

Revision History

Version	Page	Modified	Description	Released
1.0	-	-	Official Release.	07/2018
1.1	P.3,20	CL 12	Add CL 12	09/2018
1.2	P.187	Connectivity test	Align equation with JEDEC	09/2018
1.3	P.2-4	X4 specification	Add part number: NT5AD1024M4D3-HR	10/2018
	P.259-260	IDD table	Add x4 IDD and modify IDD table	
1.4	All	-	Align JESD79-4C	12/2018
1.5	P.2-3	Part number	Update I/T grade part number	12/2018

http://www.nanya.com/