Feature

- Double-data rate architecture; two data transfer per clock cycle
- Bidirectional, data strobe (DQS) is transmitted/received with data, to be used in capturing data at the receiver
- Differential clock inputs (CK and /CK)
- Bidirectional data strobe per byte of data (DQS)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Four internal banks for concurrent operation
- Data mask (DM) for write data – one mask per byte
- Programmable Burst Lengths: 2, 4 ,8 or 16
- Burst type: Sequential or interleave
- Clock Stop capability
- Concurrent Auto Precharge option is supported
- Configurable Drive Strength (DS)
- Auto Refresh and Self Refresh Modes
- Optional Partial Array Self Refresh (PASR) and Temperature Compensated Self Refresh (TCSR)
- Deep Power Down Mode (DPD)
- 1.8V LVCMOS-compatible inputs
- V_{DD}/V_{DDQ}= 1.70~1.95V
- Status Read Register (SRR)
- 64ms refresh

Table 1: Key Timing Parameters (CL=3)

Speed Grade	tCK (ns)	Clock Rate (MHz)	Access Time(ns)
T1	5	200	5.0
T2	5.4	185	5.0
T3	6	166	5.5
T4	7.5	133	6.0

Options — Marking

- V_{DD} /V_{DDQ}
  - -1.8V/1.8V — M
- Configuration
  - -32Meg x 16 (8 Meg x 16 x 4 banks) — 32M16
  - -16Meg x 32 (4 Meg x 32 x 4 banks) — 16M32
- Row-size option
  - -JEDEC-standard addressing
  - -JEDEC reduced page-size addressing
- RoHS compliance and Halogen free
- Package
  - -60-ball VFBGA (x16) — D
  - -90-ball VFBGA (x32) — C
- Timing – cycle time
  - -5.0ns @ CL=3 — T1
  - -5.4ns @ CL=3 — T2
  - -6.0ns @ CL=3 — T3
  - -7.5ns @ CL=3 — T4
- Power
  - -Standard Idd2/Idd6
  - -Low-power Idd2/Idd6
- Operating temperature range
  - -Commercial (-25℃ to +85℃)
  - -Industrial (-40℃ to +85℃)

Table 2: Configuration Addressing

Architecture	Standard		Reduced page-size
	32Meg x 16	16Meg x 32	16Meg x 32
Configuration	8Meg x 16 x 4banks	4Meg x 32 x 4banks	4Meg x 32 x 4banks
Refresh count	8k	8k	8k
Row addressing	8k (A0-A12)	8k (A0-A12)	16k (A0-A13)
Column addressing	1k (A0-A9)	512 (A0-A8)	256 (A0-A7)

Description

The 512Mb Mobile LPDDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM.

The 512Mb chip is organized as 8Mbit x 4 banks x 16 I/O or 4Mbit x 4 banks x 32 I/O device. Each of the x16's 134,217,728-bit banks is organized as 8,192 rows by 1,024 columns by 16 bits. Each of the x32's 134,217,728-bit banks is organized as 8,192 rows by 512 columns by 32 bits. In the reduced page-size option, each of the x32's 134,217,728-bit banks are organized as 16,384 rows by 256 columns by 32 bits. To achieve high-speed operation, our LPDDR SDRAM uses the double data rate architecture and adopt 2n-prefetch interface designed to transfer two data per clock cycle at the I/O pins.

The chip is designed to comply with all key Mobile Double-Data-Rate SDRAM key features. All of the control and address inputs are synchronized with a pair of externally supplied differential clocks, and latched at the cross point of differential clocks (CK rising and CK falling). The input data is registered at both edges of DQS, and the output data is referenced to both edges of DQS, as well as to both edges of CK. DQS is a bidirectional data strobe signal, transmitted by the LPDDR SDRAM during READs (edge-aligned with data), and by the memory controller during WRITEs (center-aligned with data).

LPDDR SDRAM, Read and Write access are burst oriented. The address bits registered coincident with the ACTIVE command to select the row in the specific bank. And then the address bits registered with the READ or WRITE command to select the starting column location in the bank for the burst access. The burst length can be programmed as 2, 4, 8 or 16. An Auto Precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of burst access.

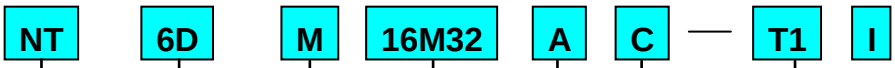
LPDDR SDRAM with Auto Refresh mode, and the Power-down mode for power saving. And the Deep Power Down Mode can achieve the maximum power reduction by removing the memory array power within Low Power DDR SDRAM. With this feature, the system can cut off almost all DRAM power without adding the cost of a power switch and giving up month-board power-line layout flexibility. Self Refresh mode with Temperature Compensated Self Refresh (TCSR) and Partial Array Self Refresh (PASR) options, which allow users to achieve additional power saving. The TCSR and PASR options can be programmed via the extended mode register. The two features may be combined to achieve even greater power saving. The DLL that is typically used on standard DDR devices is not necessary on the Mobile DDR SDRAM. It has been omitted to save power.

All inputs are LVCMOS compatible. Devices will have a V_{DD} and V_{DDQ} supply of 1.8V (nominal).

Ordering Information

Organization	Part Number	Package	Speed			
			^{t}CK (ns)	Clock (MHz)	Data Rate (Mb/s/pin)	CL
32M x 16	NT6DM32M16AD-T1	60-Ball FBGA	5.0	200	400	3
	NT6DM32M16AD-T1I		5.0	200	400	3
	NT6DM32M16AD-T3		6.0	166	333	3
	NT6DM32M16AD-T3I		6.0	166	333	3
16M x32	NT6DM16M32AC-T1	90-Ball FBGA	5.0	200	400	3
	NT6DM16M32AC-T1I		5.0	200	400	3
	NT6DM16M32AC-T3		6.0	166	333	3
	NT6DM16M32AC-T3I		6.0	166	333	3

NANYA Mobile Component/Wafer Part Numbering Guide:



NANYA Technology

Product Family

6D =LPDDR SDRAM

6V =LPDDR2-S2 SDRAM

6T = LPDDR2-S4 SDRAM

6X = LPSDR/DDR comb

6Y = LPDDR2-S2/S4 comb

Interface & Power (V_{DD} & V_{DDQ})

M = LVCMOS (1.8V, 1.8V)

Interface & Power (V_{DD1} , V_{DD2} , V_{DDQ})

H = HSUL_12 (1.8V, 1.35V, 1.2V)

Organization (Depth, Width): M=Mono; T=DDP[1] ; F=QDP[2]

256Mb = 16M16 = 8M32 = 8M32R[3]

512Mb = 32M16 = 16M32 = 16M32R

1Gb = 64M16 = 32M32 = 32M32R

2Gb = 256M8 = 128M16 = 64M32 = 64M32R

4Gb = 256M16 = 128M32 = 64T64

8Gb = 128T64 = 128F64

Note1: DDP – Dual Die Package

Note2: F = Quartic Die Package

Note3: R= Reduced page size

Device Version

A = 1st version

B = 2nd version

C = 3rd version

Grade

I =Industrial Grade

N/A =Commercial Grade

Speed

LPSDR

S1 = 166MHz @ CL=3

S2 = 133MHz @ CL=3

LPDDR

T1 = 5.0ns @ CL=3

T2 = 5.4ns @ CL=3

T3 = 6.0ns @ CL=3

T4 = 7.5ns @ CL=3

LPDDR2-S2

T1 = 5.0ns @ RL=3

T3 = 6.0ns @ RL=3

LPDDR2-S4

G0 = 1.8ns @ RL=8

G1 = 2.5ns @ RL=6

G2 = 3.0ns @ RL=5

G3 = 3.7ns @ RL=4

G4 = 5.0ns @ RL=3

Package Code ()

G = 54-Ball BGA (LPSDR, x16)

D = 60-Ball BGA (LPDDR, x16)

K = 90-Ball BGA (LPSDR, x32)

C = 90-Ball BGA (LPDDR, x32)

A = 79-Ball BGA (LPDDR2, x16)

I = 134-Ball BGA (LPDDR2, x32)

Q = 168-Ball PoP-VFBGA (LPDDR2)

R = 216-Ball PoP-VFBGA (LPDDR2)

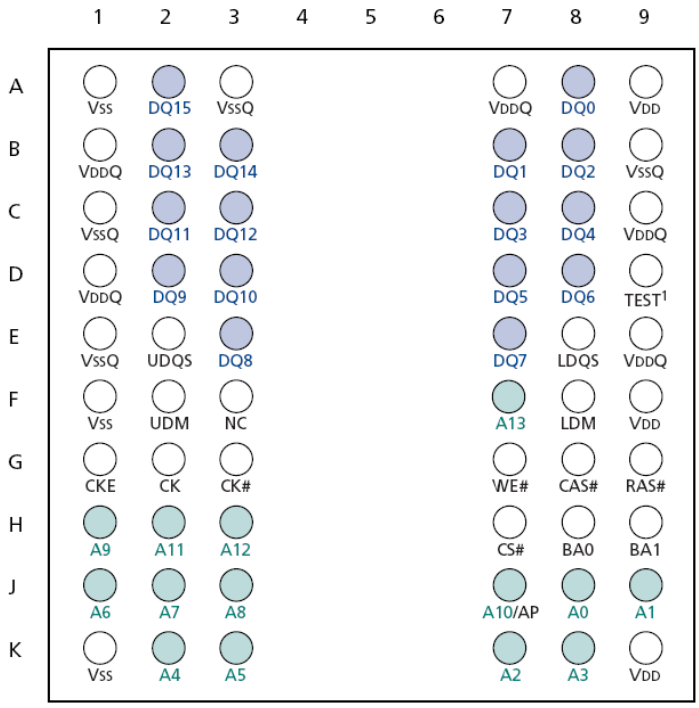
3 = 240-Ball PoP-VFBGA (LPDDR2)

0 = Wafer (KGD)

Pin Configuration – 60 balls BGA Package (x16)

< TOP View>

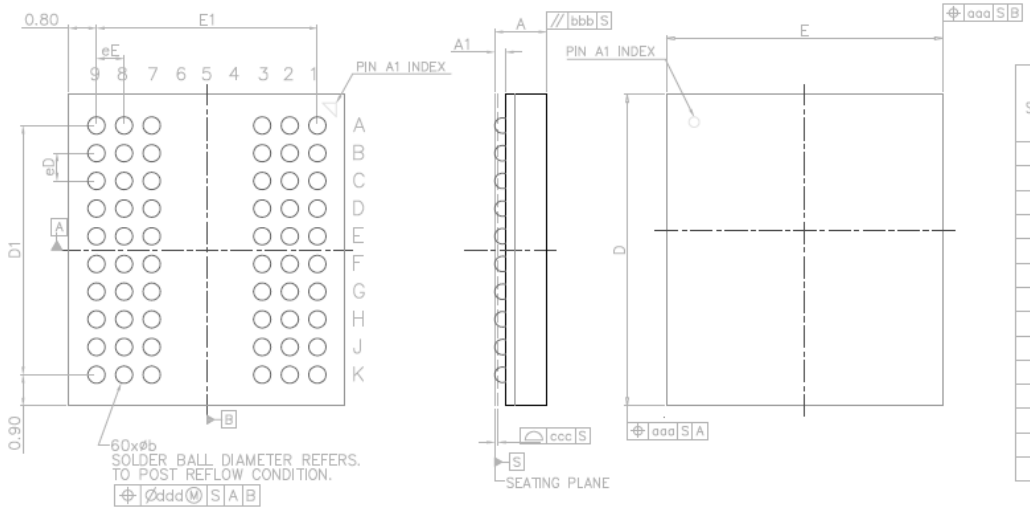
See the balls through the package



Notes:

1. D9 is a test pin that must be tied to VSS or VSSQ in normal operations.
2. Unused address pins become RFU.

Package Dimensions (x16; 60 balls; 0.8mmx0.8mm Pitch; 8 x 9mm FBGA Package)

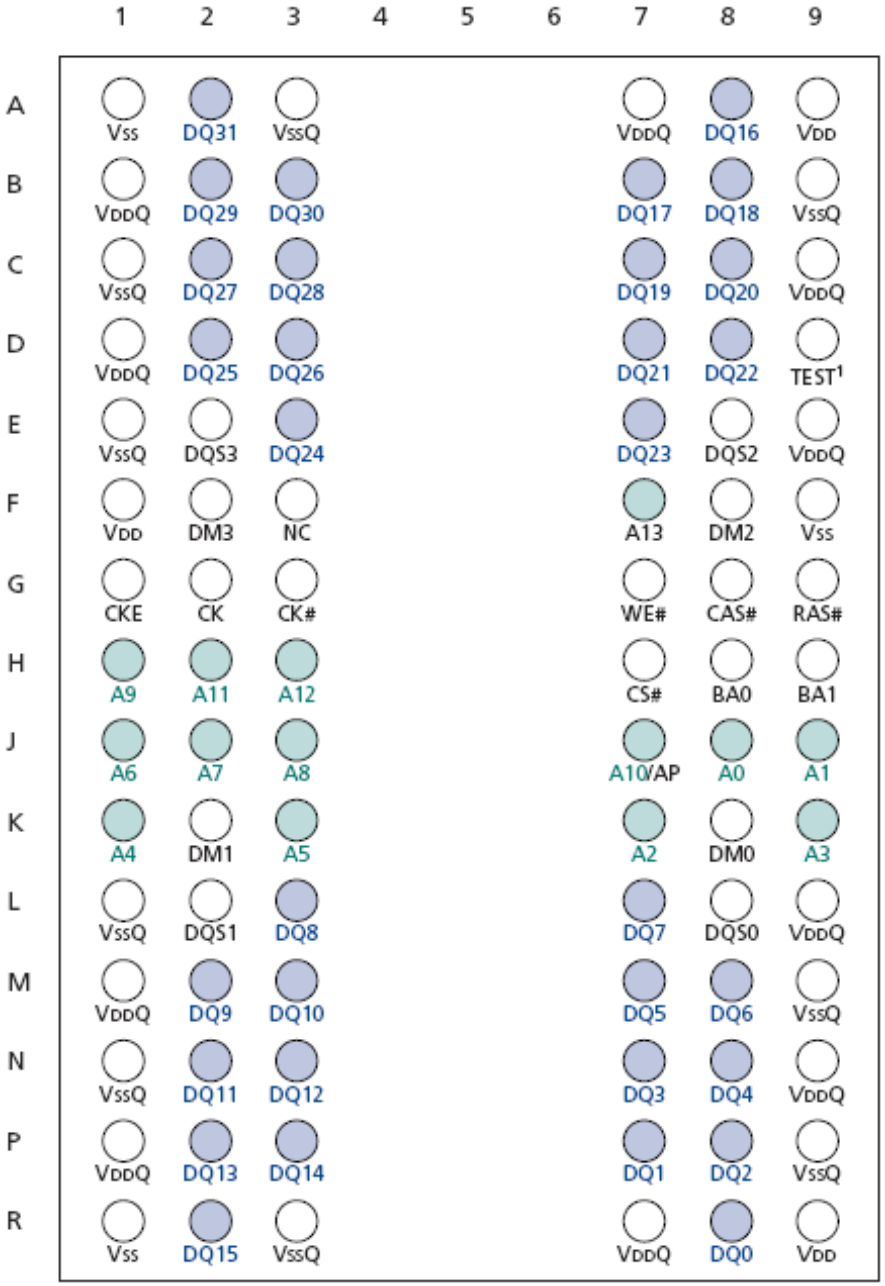


SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	0.86	0.93	1.00
A1	0.30	0.35	0.40
b	0.40	0.45	0.50
D	8.90	9.00	9.10
E	7.90	8.00	8.10
D1	7.20 BSC		
E1	6.40 BSC.		
eE	0.80 BSC.		
eD	0.80 BSC.		
aaa	0.15		
bbb	---	---	0.100
ccc	---	---	0.100
ddd	---	---	0.080
N	60		

Pin Configuration – 90 balls BGA Package (x32)

< TOP View>

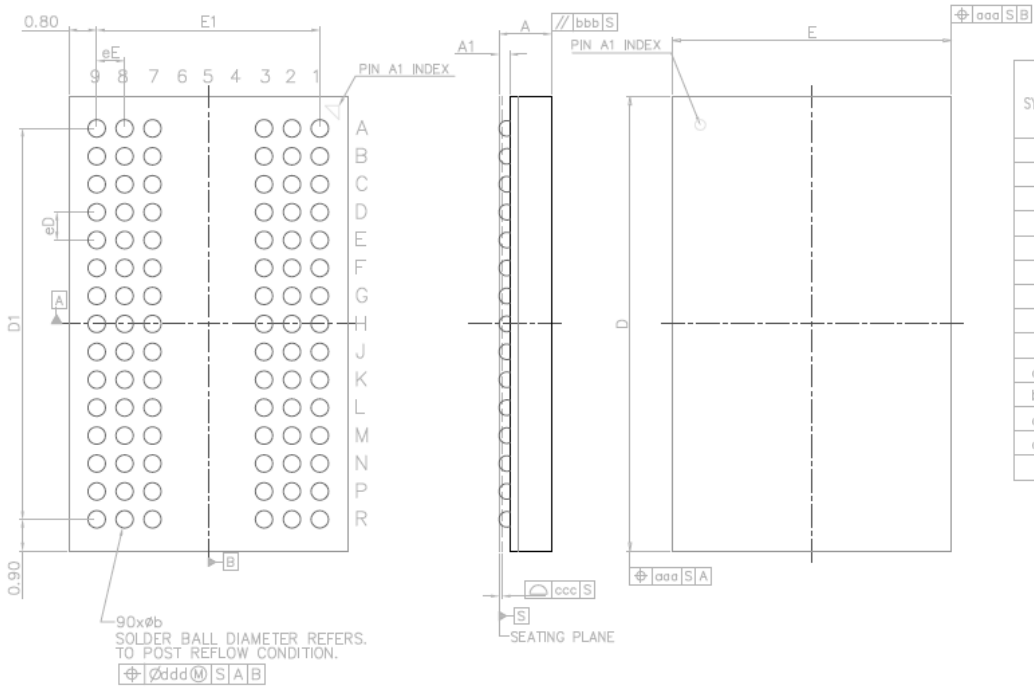
See the balls through the package



Notes:

1. D9 is a test pin that must be tied to VSS or VSSQ in normal operations.
2. Unused address pins become RFU.

Package Dimensions (x32; 90 balls; 0.8mmx0.8mm Pitch; 8 x 13mm FBGA Package)



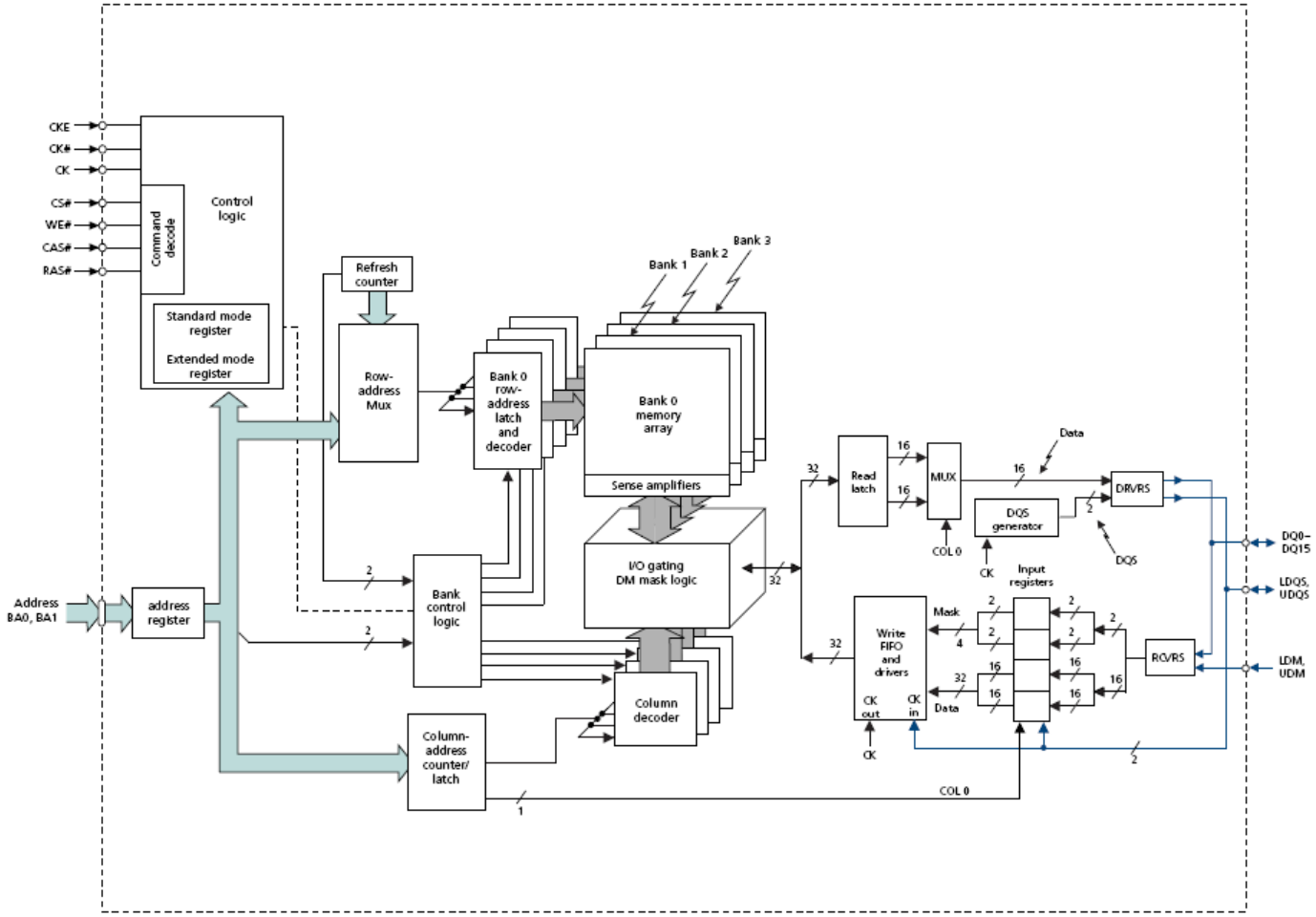
SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	0.86	0.93	1.00
A1	0.30	0.35	0.40
b	0.40	0.45	0.50
D	12.90	13.00	13.10
E	7.90	8.00	8.10
D1	11.2 BSC		
E1	6.40 BSC.		
eE	0.80 BSC.		
eD	0.80 BSC.		
aaa	0.15		
bbb	--	--	0.100
ccc	--	--	0.100
ddd	--	--	0.080
N	90		

Input / Output Functional Description

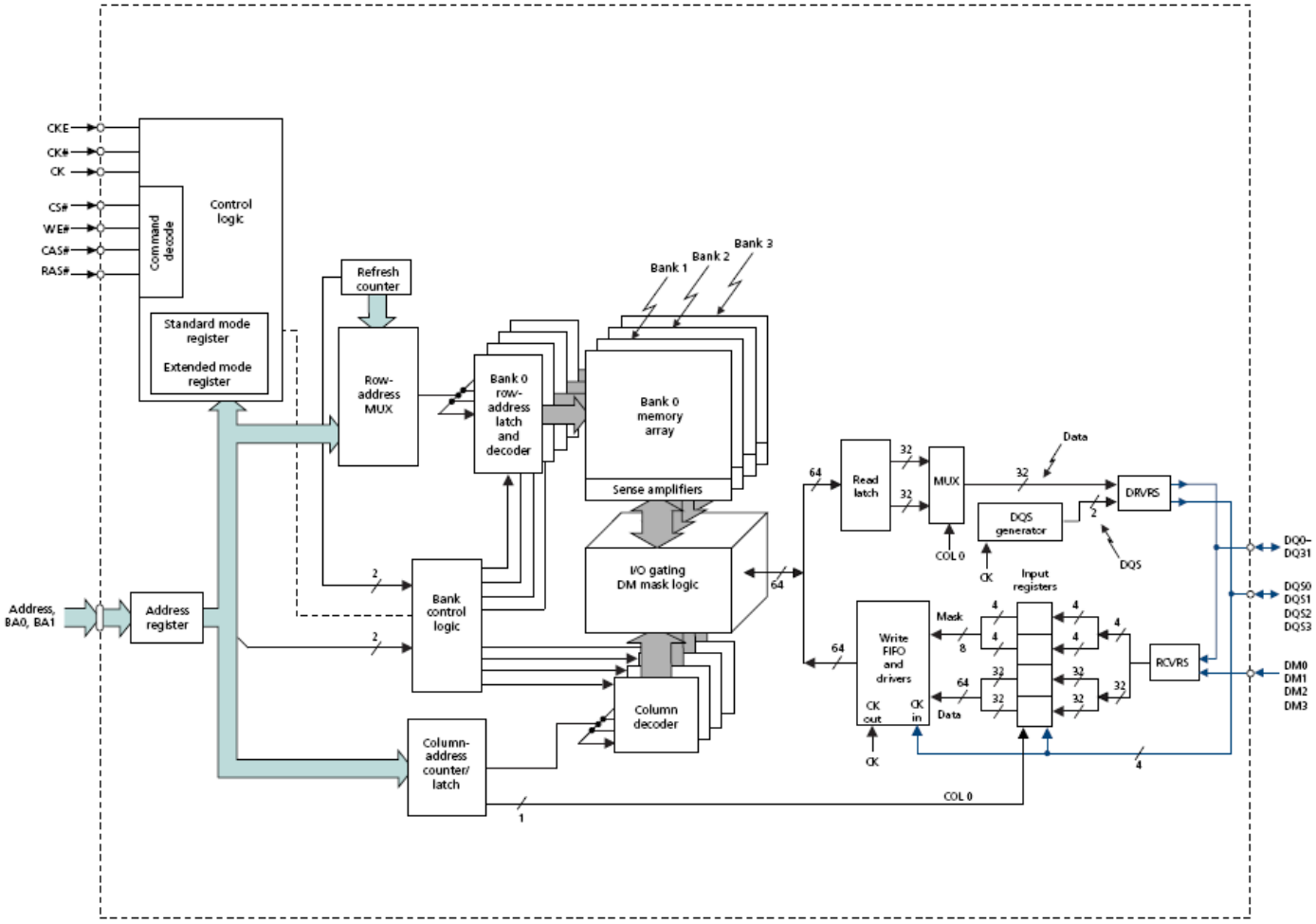
Symbol	Type	Function
CK, /CK	Input	**Clock:** CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Input and output data is referenced to the crossing of CK and /CK (both directions of crossing). Internal clock signals are derived from CK, /CK.
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWERDOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for SELF REFRESH EXIT, which is achieved asynchronously. Input buffers, excluding CK, /CK and CKE, are disabled during power-down and self refresh mode which are contrived for low standby power consumption.
/CS	Input	**Chip Select:** /CS enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when /CS is registered HIGH. /CS provides for external bank selection on systems with multiple banks. /CS is considered part of the command code.
/RAS, /CAS, /WE	Input	**Command Inputs:** /RAS, /CAS and /WE (along with /CS) define the command being entered.
DM For x16: LDM, UDM For x32: DM0-DM3	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading matches the DQ and DQS loading. For x16 devices, LDM corresponds to the data on DQ0-DQ7, UDM corresponds to the data on DQ8-DQ15. For x32 devices, DM0 corresponds to the data on DQ0-DQ7, DM1 corresponds to the data on DQ8-DQ15, DM2 corresponds to the data on DQ16-DQ23, and DM3 corresponds to the data on DQ24-DQ31.
DQ For x16: DQ0-DQ15 For x32: DQ0-DQ31	Input/output	**Data Bus:** Bi-directional Input / Output data bus.
DQS For x16: LDQS, UDQS For x32: DQS0-DQS3	Input/output	**Data Strobe:** Output with read data, input with write data. Edge-aligned with read data, centered with write data. Used to capture write data. For x16 device, LDQS corresponds to the data on DQ0-DQ7, UDQS corresponds to the data on DQ8-DQ15. For x32 device, DQS0 corresponds to the data on DQ0-DQ7, DQS1 corresponds to the data on DQ8-DQ15, DQS2 corresponds to the data on DQ16-DQ23, and DQS3 corresponds to the data on DQ24-DQ31.
BA0, BA1	Input	**Bank Address Inputs:** BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.

A13 - A0	Input	**Address Inputs:** provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ / WRITE commands, to select one location out of the memory array in the respective bank. The address inputs also provide the opcode during a MODE REGISTER SET command.
NC	-	**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** Isolated on the die for improved noise immunity.
V_{SSQ}	Supply	**DQ Ground:** Isolated on the die for improved noise immunity.
V_{DD}	Supply	**Power Supply**
V_{SS}	Supply	**Ground**
TEST	Input	**Test pin:** Must be tied to V_{SS} or V_{SSQ} in normal operations.

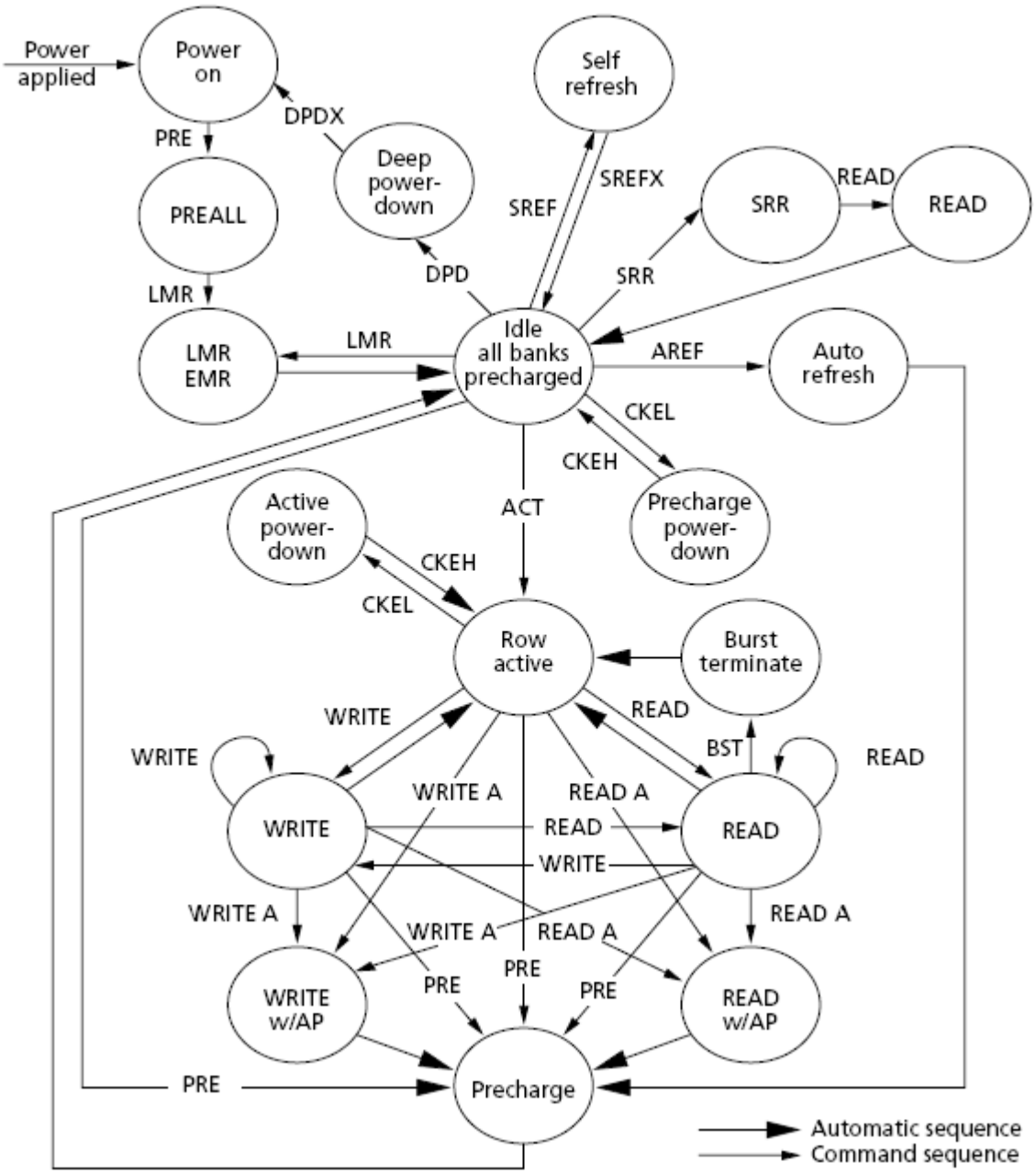
Functional Block Diagram – LPDDR 32Mx16



Functional Block Diagram – LPDDR 16Mx32



Simplified State Diagram



Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Active	LMR	Load mode register	PRE	Precharge
READ	Read (w/o Autoprecharge)	CKEH	Exit power-down	PREALL	Precharge all banks
READ A	Read (w/ Autoprecharge)	CKEL	Enter power-down	AREF	Auto Refresh
WRITE	Write (w/o Autoprecharge)	DPD	Enter Deep Power Down	SREF	Enter self refresh
WRITE A	Write (w/ Autoprecharge)	DPDX	Exit Deep Power Down	SREFX	Exit self refresh
EMR	Load extended mode registe	BST	Burst Terminate	SRR	Status Register Read

Electrical Specifications

Absolute Maximum DC Ratings

Symbol	Parameter	Min	Max	Units
V_{DD} / V_{DDQ}	V_{DD} / V_{DDQ} supply voltage relative to Vss	-1.0	2.4	V
Vin	Voltage on any pin relative to Vss	-0.5	2.4 or (V_{DDQ} + 0.3V), Whichever is less	V
Tstg	Storage Temperature (plastic)	-55	+150	°C

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM.
3. V_{DD} and V_{DDQ} must be within 300mV of each other at all times. V_{DDQ} must not exceed V_{DD}.

Input / Output Capacitance (x16, x32)

Symbol	Parameter	Min	Max	Unit	Notes
CCK	Input capacitance: CK, /CK	1.5	3.0	pF	
CDCK	Delta Input capacitance: CK, /CK	-	0.25	pF	2
CI	Input capacitance: command, address	1.5	3.0	pF	
CDI	Delta Input capacitance: command, address	-	0.5	pF	2
CIO	Input/output capacitance: DQs, DQS, DM	2.0	4.5	pF	
CDIO	Delta Input/output capacitance: DQs, DQS, DM	-	0.5	pF	3

Notes:

1. This parameter is sampled. V_{DD1}/V_{DDQ} = 1.70-1.95V, (1.2V I/O option: V_{DDQ} = 1.14-1.30V), f=100MHz, T_A=25C, Vout(DC) = VDDQ/2, Vout(peak-to-peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
2. The input capacitance per pin group will not differ by more than this maximum amount for any given device.
3. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.

AC/DC Electrical Characteristics and Operating Conditions

V_{DD} / V_{DDQ} = 1.70 ~ 1.95V

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	Supply voltage	1.7	1.95	V	6,7
V_{DDQ}	I/O Supply voltage	1.7	1.95	V	6,7
Address and Command inputs					
V_{IH}	Input voltage high	0.8 x V_{DDQ}	V_{DDQ} + 0.3	V	8, 9
V_{IL}	Input voltage low	-0.3	0.2 x V_{DDQ}	V	8, 9
Clock inputs (CK, /CK)					
V_{IN}	DC input voltage	-0.3	V_{DDQ} + 0.3	V	10
$V_{ID(DC)}$	DC input differential voltage	0.4 x V_{DDQ}	V_{DDQ} + 0.6	V	10, 11
$V_{ID(AC)}$	AC input voltage	0.6 x V_{DDQ}	V_{DDQ} + 0.6	V	10, 11
V_{IX}	AC input differential voltage	0.4 x V_{DDQ}	0.6 x V_{DDQ}	V	10, 12
Data inputs					
$V_{IH(DC)}$	DC input high voltage	0.7 x V_{DDQ}	V_{DDQ} + 0.3	V	8, 9, 13
$V_{IL(DC)}$	DC input low voltage	-0.3	0.3 x V_{DDQ}	V	8, 9, 13
$V_{IH(AC)}$	AC input high voltage	0.8 x V_{DDQ}	V_{DDQ} + 0.3	V	8, 9, 13
$V_{IL(AC)}$	AC input low voltage	-0.3	0.2 x V_{DDQ}	V	8, 9, 13
Data outputs					
V_{OH}	DC output high voltage: Logic 1 (I_{OH} = -0.1mA)	0.9 x V_{DDQ}	-	V	
V_{OL}	DC output low voltage: Logic 0 (I_{OL} = -0.1mA)	-	0.1 x V_{DDQ}	V	
Leakage current					
I_I	Input leakage current Any input 0 ≦ V_{IN} ≦ V_{DD}, All other pins not under test = 0V	-1	1	uA	
I_{OZ}	Output leakage current DQs are disabled; 0 ≦ V_{OUT} ≦ V_{DDQ}	-5	5	uA	
Operating temperature					
T_A	Commercial	-25	+85	°C	
T_A	Industrial	-40	+85	°C	

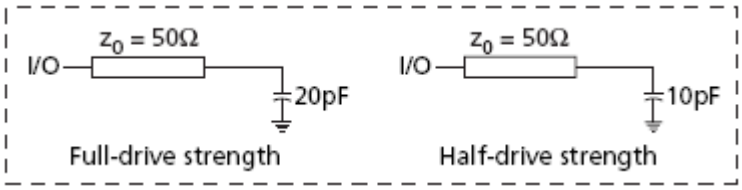
AC/DC Electrical Characteristics and Operating Conditions

V_{DD} = 1.70 ~ 1.95V, V_{DDQ} = 1.14 ~ 1.30V

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	Supply voltage	1.7	1.95	V	6,7
V_{DDQ}	I/O Supply voltage	1.14	1.30	V	6,7
Address and Command inputs					
V_{IH}	Input voltage high	0.9 x V_{DDQ}	V_{DDQ} + 0.2	V	8, 9
V_{IL}	Input voltage low	-0.2	0.1 x V_{DDQ}	V	8, 9
Clock inputs (CK, /CK)					
V_{IN}	DC input voltage	-0.2	V_{DDQ} + 0.2	V	10
$V_{ID(DC)}$	DC input differential voltage	0.4 x V_{DDQ}	V_{DDQ} + 0.4	V	10, 11
$V_{ID(AC)}$	AC input voltage	0.6 x V_{DDQ}	V_{DDQ} + 0.4	V	10, 11
V_{IX}	AC input differential voltage	0.4 x V_{DDQ}	0.6 x V_{DDQ}	V	10, 12
Data inputs					
$V_{IH(DC)}$	DC input high voltage	0.8 x V_{DDQ}	V_{DDQ} + 0.2	V	8, 9, 13
$V_{IL(DC)}$	DC input low voltage	-0.2	0.2 x V_{DDQ}	V	8, 9, 13
$V_{IH(AC)}$	AC input high voltage	0.9 x V_{DDQ}	V_{DDQ} + 0.2	V	8, 9, 13
$V_{IL(AC)}$	AC input low voltage	-0.2	0.1 x V_{DDQ}	V	8, 9, 13
Data outputs					
V_{OH}	DC output high voltage: Logic 1 (I_{OH} = -0.1mA)	0.9 x V_{DDQ}	-	V	
V_{OL}	DC output low voltage: Logic 0 (I_{OL} = -0.1mA)	-	0.1 x V_{DDQ}	V	
Leakage current					
I_I	Input leakage current Any input 0 ≦ V_{IN} ≦ V_{DD}, All other pins not under test = 0V	-1	1	uA	
I_{OZ}	Output leakage current DQs are disabled; 0 ≦ V_{OUT} ≦ V_{DDQ}	-5	5	uA	
Operating temperature					
T_A	Commercial	0	+70	°C	
T_A	Industrial	-40	+85	°C	
T_A	Automotive	-40	+105	°C	

Notes:

1. All voltage referenced to Vss.
2. All parameters assume proper device initialization.
3. Test for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal supply voltage levels, but the related specifications and device operation guaranteed for the full voltage range specified.
4. Outputs measured with equivalent load; transmission line delay is assumed to be very small:



5. Timing and IDD tests may use a VIL-to-VIH swing of up to 1.5V in the test environment, but input timing is still referenced to $V_{DDQ}/2$ (or to the crossing point for CK, /CK). The output timing reference voltage level is $V_{DDQ}/2$.

6. Any positive glitch must be less than 1/3 of the clock cycle and not more than +200mV or 2.0V, whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either –150mV or +1.6V, whichever is more positive.

7. V_{DD} and V_{DDQ} must track each other and V_{DDQ} must be less than or equal to V_{DD}.

8. To maintain a valid level, the transitioning edge of the input must:
   8a. Sustain a constant slew rate from the current AC level through to the target AC level, $V_{IL(AC)}$ or $V_{IH(AC)}$.
   8b. Reach at least the target AC level.
   8c. After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL(DC)}$ or $V_{IH(DC)}$.

9. VIH overshoot: $V_{IH\,(MAX)} = V_{DDQ}$ + 1.0V for a pulse width ≤3ns and the pulse width cannot be greater than 1/3 of the cycle rate. VIL undershoot: $V_{IL\,(MIN)}$ = –1.0V for a pulse width ≤3ns and the pulse width cannot be greater than 1/3 of the cycle rate.

10. CK and /CK input slew rate must be ≥1 V/ns (2 V/ns if measured differentially).

11. V_{ID} is the magnitude of the difference between the input level on CK and the input level on /CK.

12. The value of V_{IX} is expected to equal $V_{DDQ}/2$ of the transmitting device and must track variations in the DC level of the same.

13. DQ and DM input slew rates must not deviate from DQS by more than 10 percent. 50ps must be added to ^{t}DS and ^{t}DH for each 100 mV/ns reduction in slew rate. If slew rate exceeds 4 V/ns, functionality is uncertain.

IDD Specifications and Measurement Conditions

32Mx16 IDD Specifications; V_{DD}/V_{DDQ} = 1.70~1.95V (1.2V I/O Option: V_{DDQ} =1.14~1.30V)

Symbol	Parameter/Condition	Speed Grade				Unit	Notes
		T1 (-5)	T2 (-54)	T3 (-6)	T4 (-75)		
IDD0	**Operating one bank active-precharge current:** TRC=^{t}RC(min); ^{t}CK=^{t}CK(min);CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching; Data bus inputs are stable.	60	55	50	45	mA	6
IDD2P	**Precharge power-down standby current:** All banks idle; ^{t}CK=^{t}CK(min);CKE is LOW; CS is HIGH; Address and control inputs are switching; Data bus inputs are stable.	300				uA	7,8
IDD2PS	**Precharge power-down standby current with clock stopped:** All banks idle; CKE is LOW; CS is HIGH; CK=Low, /CK=HIGH; Address and control inputs are switching; Data bus inputs are stable.	300				uA	7
IDD2N	**Precharge non power-down standby current:** All banks idle; ^{t}CK=^{t}CK(min);CKE is HIGH; CS is HIGH; Address and control inputs are switching; Data bus inputs are stable.	11	11	11	10	mA	9
IDD2NS	**Precharge non power-down standby current with clock stopped:** All banks idle; ^{t}CK=^{t}CK(min);CKE is HIGH; CS is HIGH; Address and control inputs are switching; Data bus inputs are stable.	6	6	6	6	mA	9
IDD3P	**Active power-down standby current:** One bank active; ^{t}CK=^{t}CK(min);CKE is LOW; CS is HIGH; Address and control inputs are switching; Data bus inputs are stable.	1				mA	8
IDD3PS	**Active power-down standby current with clock stopped:** One bank active; CKE is LOW; CS is HIGH; CK=Low, /CK=HIGH; Address and control inputs are switching; Data bus inputs are stable.	1				mA	
IDD3N	**Active non power-down standby current:** One bank active; ^{t}CK=^{t}CK(min);CKE is HIGH; CS is HIGH; Address and control inputs are switching; Data bus inputs are stable.	10	10	10	10	mA	6
IDD3NS	**Active non power-down standby current with clock stopped:** One bank active; ^{t}CK=^{t}CK(min);CKE is HIGH; CS is HIGH; Address and control inputs are switching; Data bus inputs are stable.	6	6	6	6	mA	6
IDD4R	**Operating burst read current:** One bank active; ^{t}CK=^{t}CK(min);BL=4; CL=3; continuous read bursts; I_{OUT}=0mA; Address inputs are switching; 50% Data changing each burst.	80	75	70	65	mA	6
IDD4W	**Operating burst write current:** One bank active; ^{t}CK=^{t}CK(min);BL=4; continuous write bursts; Address inputs are switching; 50% Data changing each burst.	80	75	70	65	mA	6
IDD5	**Auto Refresh current:** Burst refresh; CKE=HIGH; Address and control inputs are switching; Data bus inputs are stable. — ^{t}RFC = 110ns (< 256Mb/512Mb≧1Gb)	55	55	55	55	mA	10
IDD5A	^{t}RFC = ^{t}RFI	2	2	2	2	mA	10,11
IDD8	**Deep power-down current:** Address and control pins are stable; Data bus inputs are stable.	10				uA	7

16Mx32 IDD Specifications; V_{DD}/V_{DDQ} = 1.70~1.95V (1.2V I/O Option: V_{DDQ} =1.14~1.30V)

Symbol	Parameter/Condition		Speed Grade				Unit	Notes
			T1 (-5)	T2 (-54)	T3 (-6)	T4 (-75)		
IDD0	**Operating one bank active-precharge current:** TRC=tRC(min); tCK=tCK(min);CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching; Data bus inputs are stable.	JEDEC-standard option	60	55	50	45	mA	6
IDD2P	**Precharge power-down standby current:** All banks idle; tCK=tCK(min);CKE is LOW; CS is HIGH; Address and control inputs are switching; Data bus inputs are stable.		300				uA	7,8
IDD2PS	**Precharge power-down standby current with clock stopped:** All banks idle; CKE is LOW; CS is HIGH; CK=Low, /CK=HIGH; Address and control inputs are switching; Data bus inputs are stable.		300				uA	7
IDD2N	**Precharge non power-down standby current:** All banks idle; tCK=tCK(min);CKE is HIGH; CS is HIGH; Address and control inputs are switching; Data bus inputs are stable.		11	11	11	10	mA	9
IDD2NS	**Precharge non power-down standby current with clock stopped:** All banks idle; tCK=tCK(min);CKE is HIGH; CS is HIGH; Address and control inputs are switching; Data bus inputs are stable.		6	6	6	6	mA	9
IDD3P	**Active power-down standby current:** One bank active; tCK=tCK(min);CKE is LOW; CS is HIGH; Address and control inputs are switching; Data bus inputs are stable.		1				mA	8
IDD3PS	**Active power-down standby current with clock stopped:** One bank active; CKE is LOW; CS is HIGH; CK=Low, /CK=HIGH; Address and control inputs are switching; Data bus inputs are stable.		1				mA	
IDD3N	**Active non power-down standby current:** One bank active; tCK=tCK(min);CKE is HIGH; CS is HIGH; Address and control inputs are switching; Data bus inputs are stable.		10	10	10	10	mA	6
IDD3NS	**Active non power-down standby current with clock stopped:** One bank active; tCK=tCK(min);CKE is HIGH; CS is HIGH; Address and control inputs are switching; Data bus inputs are stable.		6	6	6	6	mA	6
IDD4R	**Operating burst read current:** One bank active; tCK=tCK(min);BL=4; CL=3; continuous read bursts; I_{OUT}=0mA; Address inputs are switching; 50% Data changing each burst.		95	90	85	80	mA	6
IDD4W	**Operating burst write current:** One bank active; tCK=tCK(min);BL=4; continuous write bursts; Address inputs are switching; 50% Data changing each burst.		95	90	85	80	mA	6
IDD5	**Auto Refresh current:** Burst refresh; CKE=HIGH; Address and control inputs are switching; Data bus inputs are stable.	tRFC = 110ns (< 256Mb/512Mb≧1Gb)	55	55	55	55	mA	10
IDD5A		tRFC = tRFI	2	2	2	2	mA	10,11
IDD8	**Deep power-down current:** Address and control pins are stable; Data bus inputs are stable.		10				uA	7

IDD6 Self-refresh current; V_{DD}/V_{DDQ} = 1.70~1.95V (1.2V I/O Option: V_{DDQ} =1.14~1.30V)

Symbol	Parameter / Condition			Max	Unit	Notes
IDD6	**Self refresh current:** CKE=LOW; ^{t}CK=^{t}CK(min); Address and control inputs are stable; Data bus inputs are stable.	85°C	Full Array	600	uA	
			1/2 Array	480		
			1/4 Array	420		
			1/8 Array	420		
			1/16 Array	390		
		45°C	Full Array	360		
			1/2 Array	360		
			1/4 Array	240		
			1/8 Array	240		
			1/16 Array	230		

Notes:

1. All voltages referenced to V_{SS}.
2. Tests for I_{DD} may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage and temperature range specified.
3. Timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to $V_{DDQ}/2$ (or, to the crossing point for CK and /CK). The output timing reference voltage level is $V_{DDQ}/2$.
4. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time with the outputs open.
5. I_{DD} specifications are tested after the device is properly initialized, and are averaged at the defined cycle rate.
6. MIN (^{t}RC or ^{t}RFC) for IDD measurements is the smallest multiple of ^{t}CK that meets the minimum absolute value for the respective parameter. ^{t}RAS (MAX) for IDD measurements is the largest multiple of ^{t}CK that meets the maximum absolute value for ^{t}RAS.
7. Measurement is taken 500ms after entering into this operating mode to provide settling time for the tester.
8. V_{DD} must not vary more than 4 percent if CKE is not active while any bank is active.
9. IDD2N specifies DQ, DQS, and DM to be driven to a valid HIGH or LOW logic level.
10. CKE must be active (HIGH) during the entire time a REFRESH command is executed. From the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge until ^{t}RFC later.
11. This limit is a nominal value and does not result in a fail. CKE is HIGH during REFRESH command period (^{t}RFC [MIN]) else CKE is LOW (for example, during standby).
12. Values for IDD6 85°C are guaranteed for the entire temperature range. IDD6 45C are typical value.

Electrical Characteristics and Recommended AC Operating Conditions

V_{DD}/V_{DDQ} = 1.70~1.95V (1.2V I/O Option: V_{DDQ} =1.14~1.30V)

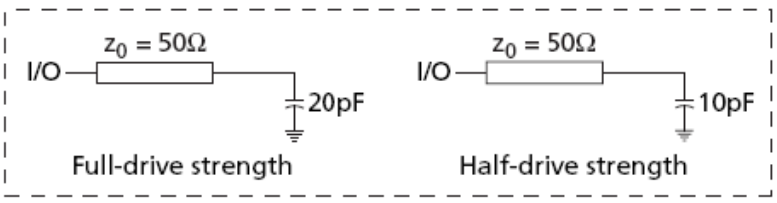
Symbol	Parameter		T1(-5)		T2(-54)		T3(-6)		T4(-75)		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Clock parameters												
^tAC	Access window of DQs from Ck, /CK	CL=3	2.0	4.8	2.0	5.0	2.0	5.5	2.0	6.0	ns	
		CL=2	2.0	6.5	2.0	6.5	2.0	6.5	2.0	6.5		
^tCK	Clock cycle time	CL=3	5.0	-	5.4	-	6	-	7.5	-	ns	10
		CL=2	12	-	12	-	12	-	12	-		
^tCH	CK high-level width		0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	^tCK	
^tCL	CK low-level width		0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	^tCK	
^tHP	Half-clock period		^tCH, ^tCL	-	^tCH, ^tCL	-	^tCH, ^tCL	-	^tCH, ^tCL	-	ns	17
CKE input parameters												
^tCKE	CKE min. pulse width (high and low)		1*^tCK	-	1*^tCK	-	1*^tCK	-	1*^tCK	-	ns	
Read parameters												
^tDQSCK	Access window of DQS from CK, /CK	CL=3	2.0	5.0	2.0	5.0	2.0	5.5	2.0	6.0	ns	
		CL=2	2.0	6.5	2.0	6.5	2.0	6.5	2.0	6.5	ns	
^tDQSQ	DQS-DQ skew, DQS to last DQ valid, per group, per access		-	0.4	-	0.45	-	0.45	-	0.6	ns	12,16
^tQHS	Data Hold Skew Factor		-	0.5	-	0.5	-	0.65	-	0.75	ns	
^tQH	DQ-DQS hold, DQS to first DQ to go non-valid, per access		^tHP - ^tQHS	-	^tHP - ^tQHS	-	^tHP - ^tQHS	-	^tHP - ^tQHS	-	ns	12,16
n/a	Data Valid output window (DVW)		^tQH – ^tDQSQ		^tQH – ^tDQSQ		^tQH – ^tDQSQ		^tQH – ^tDQSQ		ns	16
^tHZ	Data-out high-z window from CK, /CK	CL=3	-	5.0	-	5.0	-	5.5	-	6.0	ns	18,19
		CL=2	-	6.5	-	6.5	-	6.5	-	6.5	ns	
^tLZ	Data-out Low-z window from CK, /CK		1.0	-	1.0	-	1.0	-	1.0	-	ns	18
^tRPRE	DQS read preamble	CL=3	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	^tCK	
		CL=2	0.5	1.1	0.5	1.1	0.5	1.1	0.5	1.1	^tCK	
^tRPST	DQS read postamble		0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	^tCK	
^tSRC	Read of SRR to next valid command		CL+1	-	CL+1	-	CL+1	-	CL+1	-	^tCK	
^tSRR	SRR-to-READ		2	-	2	-	2	-	2	-	^tCK	
^tTQ	Internal temperature sensor valid temperature output enable		2	-	2	-	2	-	2	-	ms	

Symbol	Parameter	T1(-5)		T2(-54)		T3(-6)		T4(-75)		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write parameters											
^tDH_f	DQ and DM input hold time relative to DQS (fast slew rate)	0.48	-	0.54	-	0.6	-	0.8	-	ns	12,13, 14
^tDH_s	DQ and DM input hold time relative to DQS (slow slew rate)	0.58	-	0.64	-	0.7	-	0.9	-	ns	
^tDS_f	DQ and DM input setup time relative to DQS (fast slew rate)	0.48	-	0.54	-	0.6	-	0.8	-	ns	12,13, 14
^tDS_s	DQ and DM input setup time relative to DQS (slow slew rate)	0.58	-	0.64	-	0.7	-	0.9	-	ns	
^tDIPW	DQ and DM input pulse width (for each input)	1.4	-	1.5	-	1.6	-	1.6	-	ns	15
^tDQSS	WRITE command to first DQS latching transition	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	^tCK	
^tDQSH	DQS input high pulse width	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	^tCK	
^tDQSL	DQS input low pulse width	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	^tCK	
^tDSH	DQS falling edge from CK rising – hold time	0.2	-	0.2	-	0.2	-	0.2	-	^tCK	
^tDSS	DQS falling edge from CK rising – setup time	0.2	-	0.2	-	0.2	-	0.2	-	^tCK	
^tWPRE	DQS write preamble	0.25	-	0.25	-	0.25	-	0.25	-	^tCK	
^tWPRES	DQS write preamble setup time	0	-	0	-	0	-	0	-	ns	23,24
^tWPST	DQS write postamble	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	^tCK	25
Command / Address Input parameters											
^tIH_f	Address and Control input hold time (fast slew rate)	0.9	-	1.0	-	1.1	-	1.3	-	ns	14,20
^tIH_s	Address and Control input hold time (slow slew rate)	1.1	-	1.2	-	1.2	-	1.5	-	ns	
^tIS_f	Address and Control input setup time (fast slew rate)	0.9	-	1.0	-	1.1	-	1.3	-	ns	14,20
^tIS_s	Address and Control input setup time (slow slew rate)	1.1	-	1.2	-	1.2	-	1.5	-	ns	
^tIPW	Address and Control input pulse width	2.3	-	2.5	-	2.6	-	$^tIS + ^tIH$	-	ns	15
Mode register parameters											
^tMRD	Load MODE Register command cycle time	2	-	2	-	2	-	2	-	^tCK	
SDRAM core parameters											
^tRAS	ACTIVE to PRECHARGE command	40	70,000	41.8	70,000	41.8	70,000	45	70,000	ns	21
^tRC	ACTIVE to ACTIVE / ACTIVE to AUTO REFRESH command period	55	-	58.2	-	59.8	-	67.5	-	ns	

Symbol	Parameter	T1(-5)		T2(-54)		T3(-6)		T4(-75)		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
tRCD	ACTIVE to READ or WRITE delay	15	-	16.2	-	18	-	22.5	-	ns	
tRP	PRECHARGE command period	15	-	16.2	-	18	-	22.5	-	ns	
tRRD	ACTIVE *bank-a* to ACTIVE *bank-b* command	10	-	10.8	-	12	-	15	-	ns	
tDAL	Auto precharge write recovery + precharge time	-	-	-	-	-	-	-	-	-	11
tWR	Write recovery time	15	-	15	-	15	-	15	-	ns	26
tWTR	Internal WRITE to READ command delay	2	-	2	-	1	-	1	-	tCK	
tXP	Exit power-down mode to first valid command	6	-	6	-	6	-	7.5	-	ns	
tXSR	Exit SELF REFRESH to first valid command	112.5	-	112.5	-	112.5	-	112.5	-	ns	27
tREF	Refresh period	-	64	-	64	-	64	-	64	ms	
tREFI	Average periodic refresh interval	-	7.8	-	7.8	-	7.8	-	7.8	us	22
tRFC	Auto Refresh command period	72	-	72	-	72	-	72	-	ns	

Notes:

1. All voltages referenced to Vss.
2. All parameters assume proper device initialization.
3. Tests for AC timing, and electrical AC and DC characteristics may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
4. The circuit shown below represents the timing reference load used in defining the relevant timing parameters of the device. It is not intended to be either a precise representation of the typical system environment or a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to system environment. Specifications are correlated to production test conditions (generally a coaxial transmission line terminated at the tester electronics). For the half-strength driver with a nominal 10pF load, parameters tAC and tQH are expected to be in the same range. However, these parameters are not subject to production test but are estimated by design/characterization. Use of IBIS or other simulation tools for system design validation is suggested.



5. The CK, /CK input reference voltage level (for timing referenced to CK, /CK) is the point at which CK and /CK cross; the input reference voltage level for signals other than CK, /CK is $V_{DDQ}/2$.
6. A CK and /CK input slew rate ≥1 V/ns (2 V/ns if measured differentially) is assumed for all parameters.
7. All AC timings assume an input slew rate of 1 V/ns.

8. CAS latency definition: with CL = 2, the first data element is valid at (^{t}CK + ^{t}AC) after the clock at which the READ command was registered; for CL = 3, the first data element is valid at (2 × ^{t}CK + ^{t}AC) after the first clock at which the READ command was registered.

9. Timing tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{DDQ}/2 or to the crossing point for CK, /CK. The output timing reference voltage level is V_{DDQ}/2.

10. Clock frequency change is supported only during a clock stop, power-down, or self-refresh mode.

11. ^{t}DAL = (^{t}WR/^{t}CK) + (^{t}RP/^{t}CK): for each term, if not already an integer, round to the next higher integer.

12. Referenced to each output group: for x16, LDQS with DQ0–DQ7; and UDQS with DQ8–DQ15. For x32, DQS0 with DQ0–DQ7; DQS1 with DQ8–DQ15; DQS2 with DQ16–DQ23; and DQS3 with DQ24–DQ31.

13. DQ and DM input slew rates must not deviate from DQS by more than 10 percent. If the DQ/DM/DQS slew rate is less than 1.0 V/ns, timing must be derated: 50ps must be added to ^{t}DS and ^{t}DH for each 100 mV/ns reduction in slew rate. If slew rate exceeds 4 V/ns, functionality is uncertain.

14. The transition time for input signals (/CAS, CKE, /CS, DM, DQ, DQS, /RAS, /WE, and addresses) are measured between $V_{IL(DC)}$ to $V_{IH(AC)}$ for rising input signals and $V_{IH(DC)}$ to $V_{IL(AC)}$ for falling input signals.

15. These parameters guarantee device timing but are not tested on each device.

16. The valid data window is derived by achieving other specifications: ^{t}HP (^{t}CK/2), ^{t}DQSQ, and ^{t}QH (^{t}HP - ^{t}QHS). The data valid window derates directly proportional with the clock duty cycle and a practical data valid window can be derived. The clock is provided a maximum duty cycle variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio.

17. ^{t}HP (MIN) is the lesser of ^{t}CL (MIN) and ^{t}CH (MIN) actually applied to the device CK and /CK inputs, collectively.

18. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (^{t}HZ) or begins driving (^{t}LZ).

19. ^{t}HZ (MAX) will prevail over ^{t}DQSCK (MAX) + ^{t}RPST (MAX) condition.

20. Fast command/address input slew rate ≥1 V/ns. Slow command/address input slew rate ≥0.5 V/ns. If the slew rate is less than 0.5 V/ns, timing must be derated: ^{t}IS has an additional 50ps per each 100 mV/ns reduction in slew rate from the 0.5 V/ns. ^{t}IH has 0ps added, therefore, it remains constant. If the slew rate exceeds 4.5 V/ns, functionality is uncertain.

21. READs and WRITEs with auto precharge must not be issued until ^{t}RAS (MIN) can be satisfied prior to the internal PRECHARGE command being issued.

22. The refresh period equals 64ms. This equates to an average refresh rate of 7.8125µs.

23. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.

24. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on ^{t}DQSS.

25. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

26. At least one clock cycle is required during ^{t}WR time when in auto precharge mode.

27. Clock must be toggled a minimum of two times during the ^{t}XSR period.

Target Output Drive Characteristics (Full Strength)

Characteristics are specified under best and worst process variation/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	2.8	18.53	–2.80	–18.53
0.20	5.6	26.8	–5.60	–26.80
0.30	8.4	32.8	–8.40	–32.80
0.40	11.2	37.05	–11.20	–37.05
0.50	14	40	–14.00	–40.00
0.60	16.8	42.5	–16.80	–42.50
0.70	19.6	44.57	–19.60	–44.57
0.80	22.4	46.5	–22.40	–46.50
0.85	23.8	47.48	–23.80	–47.48
0.90	23.8	48.5	–23.80	–48.50
0.95	23.8	49.4	–23.80	–49.40
1.00	23.8	50.05	–23.80	–50.05
1.10	23.8	51.35	–23.80	–51.35
1.20	23.8	52.65	–23.80	–52.65
1.30	23.8	53.95	–23.80	–53.95
1.40	23.8	55.25	–23.80	–55.25
1.50	23.8	56.55	–23.80	–56.55
1.60	23.8	57.85	–23.80	–57.85
1.70	23.8	59.15	–23.80	–59.15
1.80	–	60.45	–	–60.45
1.90	–	61.75	–	–61.75

Notes:

1. Table values based on nominal impedance of 25Ω (full-drive) at $V_{DDQ}/2$.
2. The full variation in drive current, from minimum to maximum—due to process, voltage, and temperature—will lie within the outer bounding lines of the I-V curves.

Target Output Drive Characteristics (Three-Quarter Strength)

Characteristics are specified under best and worst process variation/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	1.96	12.97	-1.96	-12.97
0.20	3.92	18.76	-3.92	-18.76
0.30	5.88	22.96	-5.88	-22.96
0.40	7.84	25.94	-7.84	-25.94
0.50	9.8	28	-9.8	-28
0.60	11.76	29.75	-11.76	-29.75
0.70	13.72	31.2	-13.72	-31.2
0.80	15.68	32.55	-15.68	-32.55
0.85	16.66	33.24	-16.66	-33.24
0.90	16.66	33.95	-16.66	-33.95
0.95	16.66	34.58	-16.66	-34.58
1.00	16.66	35.04	-16.66	-35.04
1.10	16.66	35.95	-16.66	-35.95
1.20	16.66	36.86	-16.66	-36.86
1.30	16.66	37.77	-16.66	-37.77
1.40	16.66	38.68	-16.66	-38.68
1.50	16.66	39.59	-16.66	-39.59
1.60	16.66	40.5	-16.66	-40.5
1.70	16.66	41.41	-16.66	-41.41
1.80	–	42.32	–	-42.32
1.90	–	43.23	–	-43.23

Notes:

1. Table values based on nominal impedance of 37Ω (three-quarter drive strength) at $V_{DDQ}/2$.
2. The full variation in drive current, from minimum to maximum—due to process, voltage, and temperature—will lie within the outer bounding lines of the I-V curves.
3. Contact factory for availability of three-quarter drive strength.

Target Output Drive Characteristics (One-half Strength)

Characteristics are specified under best and worst process variation/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	1.27	8.42	–1.27	–8.42
0.20	2.55	12.3	–2.55	–12.30
0.30	3.82	14.95	–3.82	–14.95
0.40	5.09	16.84	–5.09	–16.84
0.50	6.36	18.2	–6.36	–18.20
0.60	7.64	19.3	–7.64	–19.30
0.70	8.91	20.3	–8.91	–20.30
0.80	10.16	21.2	–10.16	–21.20
0.85	10.8	21.6	–10.80	–21.60
0.90	10.8	22	–10.80	–22.00
0.95	10.8	22.45	–10.80	–22.45
1.00	10.8	22.73	–10.80	–22.73
1.10	10.8	23.21	–10.80	–23.21
1.20	10.8	23.67	–10.80	–23.67
1.30	10.8	24.14	–10.80	–24.14
1.40	10.8	24.61	–10.80	–24.61
1.50	10.8	25.08	–10.80	–25.08
1.60	10.8	25.54	–10.80	–25.54
1.70	10.8	26.01	–10.80	–26.01
1.80	–	26.48	–	–26.48
1.90	–	26.95	–	–26.95

Notes:

1. Table values based on nominal impedance of 55Ω (half-drive strength) at $V_{DDQ}/2$.
2. The full variation in drive current, from minimum to maximum—due to process, voltage, and temperature—will lie within the outer bounding lines of the I-V curves.
3. The I-V curve for one-quarter drive strength is approximately 50 percent of one-half drive strength.

Target Output Drive Characteristics, 1.2V I/O (Full-Drive Strength)

Characteristics are specified under best and worst process variation/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	2.8	13.4	–2.80	–13.40
0.20	5.6	18.52	–5.60	–18.52
0.30	8.4	22.25	–8.40	–22.25
0.40	11.2	25.46	–11.20	–25.46
0.50	14	29.07	–14.00	–29.07
0.60	15.86	32.33	–15.86	–32.33
0.70	15.86	35.54	–15.86	–35.54
0.80	15.86	38.85	–15.86	–38.85
0.90	15.86	42.32	–15.86	–42.32
1.00	15.86	45.58	–15.86	–45.58
1.10	15.86	49.14	–15.86	–49.14
1.20	15.86	53.19	–15.86	–53.19
1.30	–	57.55	–	–57.55

Notes: 1. Table values based on nominal impedance of 25Ω (full-drive strength) at $V_{DDQ}/2$.

2. The full variation in drive current, from minimum to maximum—due to process, voltage, and temperature—will lie within the outer bounding lines of the I-V curves.

Target Output Drive Characteristics, 1.2V I/O (Three-Quarter Drive Strength)

Characteristics are specified under best and worst process variation/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	1.96	9.38	–1.96	–9.38
0.20	3.92	12.97	–3.92	–12.97
0.30	5.88	15.87	–5.88	–15.87
0.40	7.84	18.33	–7.84	–18.33
0.50	9.8	20.34	–9.80	–20.34
0.60	11.1	22.63	–11.10	–22.63
0.70	11.1	25.03	–11.10	–25.03
0.80	11.1	27.14	–11.10	–27.14
0.90	11.1	29.91	–11.10	–29.91
1.00	11.1	32.18	–11.10	–32.18
1.10	11.1	34.95	–11.10	–34.95
1.20	11.1	37.78	–11.10	–37.78
1.30	–	40.58	–	–40.58

Notes: 1. Table values based on nominal impedance of 36Ω (**Three-Quarter** drive strength) at $V_{DDQ}/2$.

2. The full variation in drive current, from minimum to maximum—due to process, voltage, and temperature—will lie within the outer bounding lines of the I-V curves.

Target Output Drive Characteristics, 1.2V I/O (Half-Drive Strength)

Characteristics are specified under best and worst process variation/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	1.27	6.15	–1.27	–6.15
0.20	2.55	8.42	–2.55	–8.42
0.30	3.82	10.15	–3.82	–10.15
0.40	5.09	11.6	–5.09	–11.60
0.50	6.36	13.25	–6.36	–13.25
0.60	7.2	14.67	–7.20	–14.67
0.70	7.2	15.91	–7.20	–15.91
0.80	7.2	17.38	–7.20	–17.38
0.90	7.2	18.99	–7.20	–18.99
1.00	7.2	20.6	–7.20	–20.60
1.10	7.2	22.21	–7.20	–22.21
1.20	7.2	23.82	–7.20	–23.82
1.30	–	25.53	–	–25.53

Notes: 1. Table values based on nominal impedance of 55Ω (full-drive strength) at $V_{DDQ}/2$.

2. The full variation in drive current, from minimum to maximum—due to process, voltage, and temperature—will lie within the outer bounding lines of the I-V curves.

Basic Functionality

The LPDDR SDRAM is a high-speed CMOS, dynamic random access memory internally configured as a four-bank DRAM. The double data rate architecture is essentially a 2n prefetch with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the LPDDR SDRAM effectively consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write access to the LPDDR SDRAM are burst oriented; access start at a selected location and continue for a programmed number of locations in a programmed sequence. Operation begins with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and the row to be activated (BA0-BA1 select the bank; A0-A13 select the row). The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst operation. The Mobile DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4, 8, or 16. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access. As with standard DDR SDRAMs, the pipelined, multibank architecture of the Mobile DDR SDRAMs supports concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power saving power-down mode. Deep power-down mode is offered to achieve maximum power reduction by eliminating the power of the memory array. Data will not be retained after device enters deep power-down mode. Two self refresh features, temperature-compensated self refresh (TCSR) and partial array self refresh (PASR), offer additional power saving. TCSR is controlled by the automatic on-chip temperature sensor. The PASR can be customized using the extended mode register settings. The two features may be combined to achieve even greater power saving. The DLL that is typically used on standard DDR devices is not necessary on the Mobile DDR SDRAM. It has been omitted to save power.

Prior to normal operation, the LPDDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

LPDDR SDRAMs must be powered up and initialized in a predefined manner. Operations procedures other than those specified may result in undefined operation. And any interruption to the device power, the initialization routine should be followed to ensure proper functionality of the Mobile DDR SDRAM.

The Following sequence is required for POWER UP and Initialization

1. Apply power, the device core power (V_{DD}) and the device I/O power (V_{DDQ}) must be brought up simultaneously to prevent device latch-up. It is recommended that V_{DD} and V_{DDQ} be from the same power source or V_{DDQ} must never exceed V_{DD}. Assert and hold CKE HIGH.

2. When power supply voltages are stable and the CKE has been driven HIGH, it's safe to apply the clock.

3. There must be at least 200us of valid clocks before any command may be given to the DRAM. During this time, NOP or DESELECT commands must be issued on the command bus.

4. Issue a PRECHARGE ALL command.

5. Provide NOPs or DESELECT commands for at least ^{t}RP time.

6. Issue AUTO REFRESH command followed by NOPs or DESELECT commands for at least ^{t}RFC time. And Issue the second AUTO REFRESH command followed by NOPs or DESELECT command for at least ^{t}RFC time. Two AUTO REFRESH commands must be issued. Typically, both of these commands are issued at this stage as described above.

7. Issue MRS Command to load the base mode register as desired.

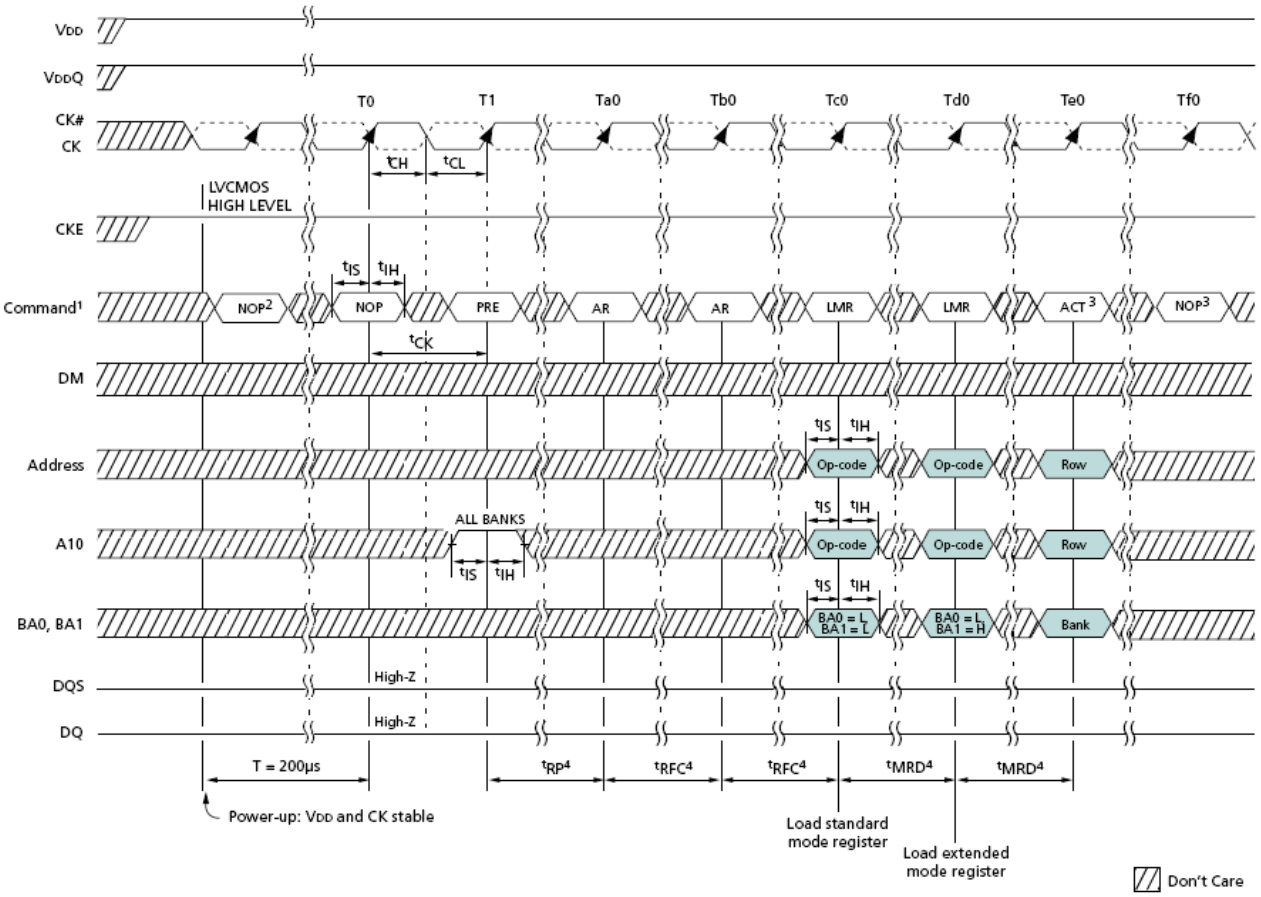
8. Issue NOPs or DESELECT commands for at least ^{t}MRD time.

9. Issue MRS Command to program the extended mode register for the desired operating modes. Note that the sequence in which the standard and extended mode registers are programmed is not critical.

10. Issue NOP or DESELECT commands for at least ^{t}MRD time.

After steps 1 through 10 are completed, the Mobile DDR SDRAM has been properly initialized and is ready for any valid command.

Initialization Sequence



Notes:

1. PRE = PRECHARGE command; LMR = LOAD MODE REGISTER command; AR = AUTO REFRESH command; ACT = ACTIVE command.
2. NOP or DESELECT commands are required for at least 200us.
3. Other valid commands are possible.
4. NOPs or DESELECTs are required during this time.

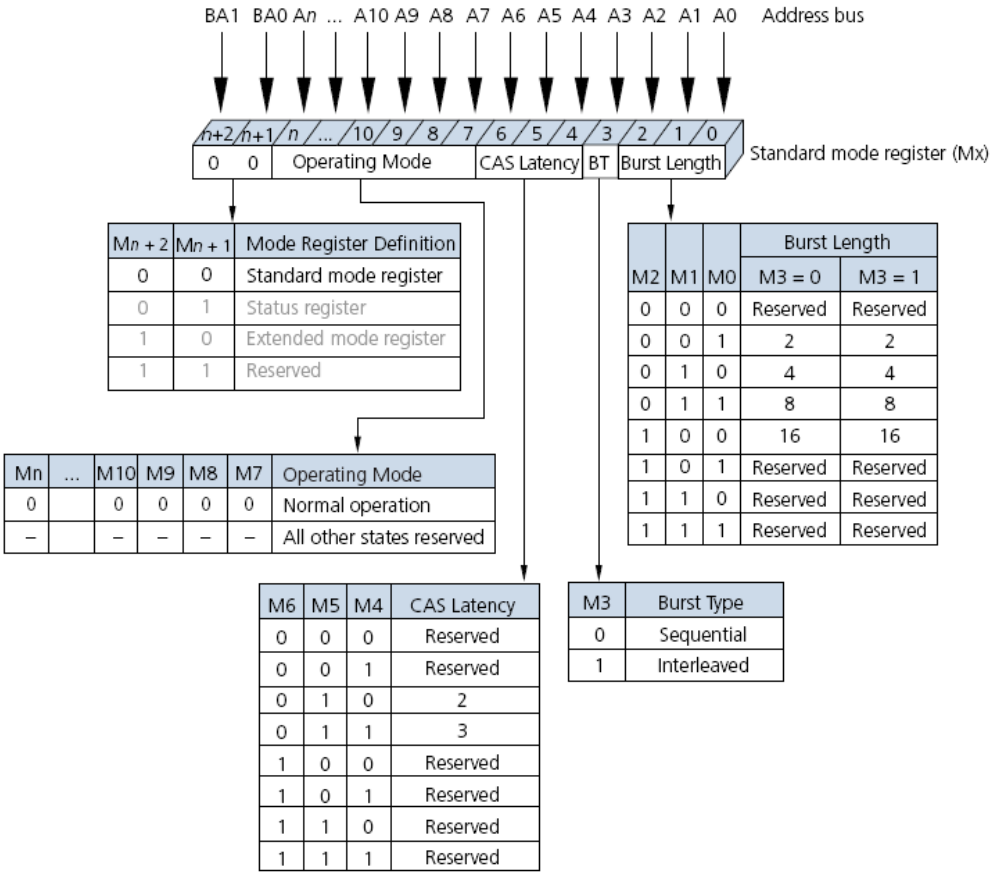
Register Definition

Mode Registers and Extended Mode Registers

The Mode Registers are used to define the specific mode of operation of the LPDDR SDRAM. This define includes the definition of a burst length, a burst type, a CAS latency. Additionally, driver strength, Temperature Compensated Self Refresh (TCSR), and Partial Array Self Refresh (PASR) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. The default value of the mode register is not defined, therefore the mode register must be written after power up for proper operation. The Mode Register must be loaded when all banks are idle and no bursts are progress, and the controller must wait the specific time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation. The MRS contents won't be changed until it is reprogrammed, the device goes into Deep Power-Down, or the device loses power.

The mode register is written by asserting low on /CS, /RAS, /CAS, /WE, BA0 and BA1, while controlling the state of address pins A0~A13. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on the functionality. Burst length is defined by A0~A2 with options of 2, 4, 8 and 16 bit burst length. Burst address sequence type is defined by A3 and /CAS latency is defined by A4~A6. A7~A13 must be set to low to ensure future compatibility.

Standard Mode Register definition



Mn + 2	Mn + 1	Mode Register Definition
0	0	Standard mode register
0	1	Status register
1	0	Extended mode register
1	1	Reserved

Mn	...	M10	M9	M8	M7	Operating Mode
0		0	0	0	0	Normal operation
–		–	–	–	–	All other states reserved

			Burst Length	
M2	M1	M0	M3 = 0	M3 = 1
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	16	16
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

Notes: 1. The integer *n* is equal to the most significant address bit.

Burst Length, Type, and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 as above figure. The ordering of access within a burst is determined by the burst length, burst type, and the starting column address. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. The burst length is defined by bits A0-A2. Burst length options include 2, 4, 8 or 16 for both the sequential and the interleaved burst types.

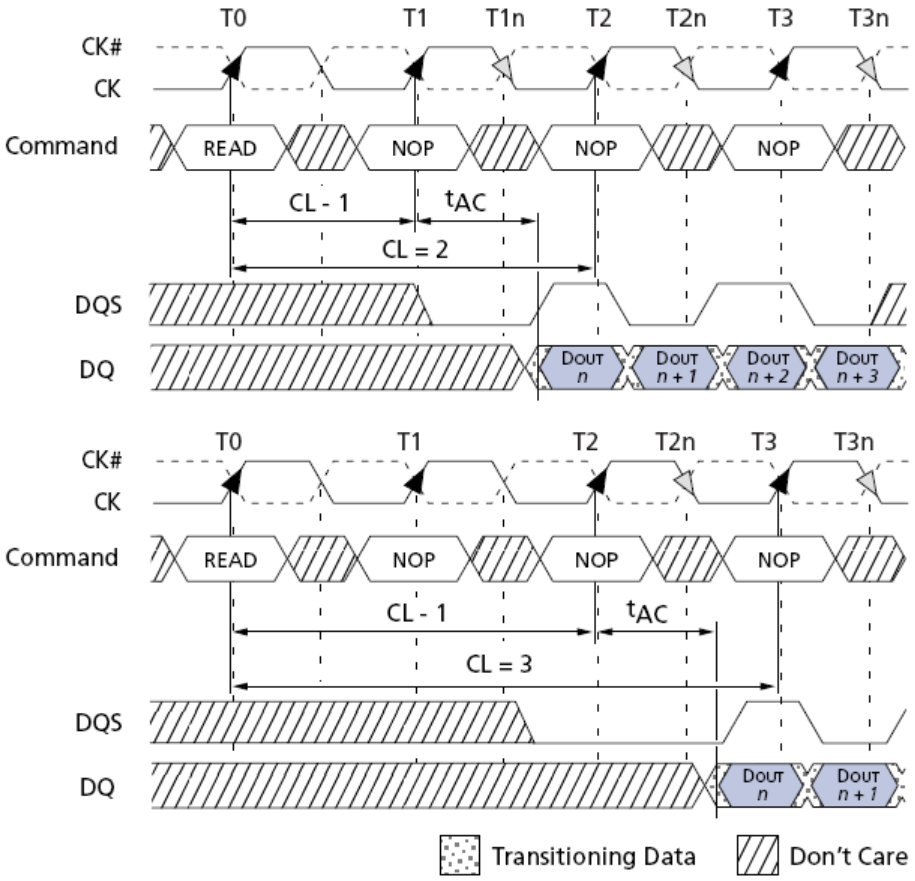
When a READ or WRITE command is issued, a block of columns equal to the BL is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap when a boundary is reached. The block is uniquely selected by A1–Ai when BL = 2, by A2–Ai when BL = 4, by A3–Ai when BL = 8, and by A4–Ai when BL = 16, where Ai is the most significant column address bit for a given configuration. The remaining (least significant) address bits are used to specify the starting location within the block. The programmed BL applies to both READ and WRITE bursts. Accesses within a given burst may be programmed to be either sequential or interleaved via the standard mode register.

Burst Type and Burst Order

Burst Length	Starting Column Address (A3, A2,A1,A0)	Burst type = Sequential A3 = 0	Burst type = Interleaved A3 = 1
2	0000	0,1	0,1
	0001	1,0	1,0
4	0000	0,1,2,3	0,1,2,3
	0001	1,2,3,0	1,0,3,2
	0010	2,3,0,1	2,3,0,1
	0011	3,0,1,2	3,2,1,0
8	0000	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
	0001	1,2,3,4,5,6,7,0	1,0,3,2,5,4,7,6
	0010	2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
	0011	3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
	0100	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
	0101	5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
	0110	6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
	0111	7,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0
16	0000	0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F	0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F
	0001	1,2,3,4,5,6,7,8,9,A,B,C,D,E,F,0	1,0,3,2,5,4,7,6,9,8,B,A,D,C,F,E
	0010	2,3,4,5,6,7,8,9,A,B,C,D,E,F,0,1	2,3,0,1,6,7,4,5,A,B,8,9,E,F,C,D
	0011	3,4,5,6,7,8,9,A,B,C,D,E,F,0,1,2	3,2,1,0,7,6,5,4,B,A,9,8,F,E,D,C
	0100	4,5,6,7,8,9,A,B,C,D,E,F,0,1,2,3	4,5,6,7,0,1,2,3,C,D,E,F,8,9,A,B
	0101	5,6,7,8,9,A,B,C,D,E,F,0,1,2,3,4	5,4,7,6,1,0,3,2,D,C,F,E,9,8,B,A
	0110	6,7,8,9,A,B,C,D,E,F,0,1,2,3,4,5	6,7,4,5,2,3,0,1,E,F,C,D,A,B,8,9
	0111	7,8,9,A,B,C,D,E,F,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0,F,E,D,C,B,A,9,8
	1000	8,9,A,B,C,D,E,F,0,1,2,3,4,5,6,7	8,9,A,B,C,D,E,F,0,1,2,3,4,5,6,7
	1001	9,A,B,C,D,E,F,0,1,2,3,4,5,6,7,8	9,8,B,A,D,C,F,E,1,0,3,2,5,4,7,6
	1010	A,B,C,D,E,F,0,1,2,3,4,5,6,7,8,9	A,B,8,9,E,F,C,D,2,3,0,1,6,7,4,5
	1011	B,C,D,E,F,0,1,2,3,4,5,6,7,8,9,A	B,A,9,8,F,E,D,C,3,2,1,0,7,6,5,4
	1100	C,D,E,F,0,1,2,3,4,5,6,7,8,9,A,B	C,D,E,F,8,9,A,B,4,5,6,7,0,1,2,3
	1101	D,E,F,0,1,2,3,4,5,6,7,8,9,A,B,C	D,C,F,E,,9,8,B,A,5,4,7,6,1,0,3,2
	1110	E,F,0,1,2,3,4,5,6,7,8,9,A,B,C,D	E,F,C,D,A,B,8,9,6,7,4,5,2,3,0,1
	1111	F,0,1,2,3,4,5,6,7,8,9,A,B,C,D,E	F,E,D,C,B,A,9,8,7,6,5,4,3,2,1,0

CAS Latency (CL)

The CAS Latency, or READ latency is the delay, in clock cycles, between the registration of a Read command and the availability of the first bit of output data. CAS Latency is defined by bit A6~A4 in the standard mode register. If a READ command is registered at a clock edge n, and the CAS latency is 3 clocks, the first data element will be valid at (n + 2^{t}CK + ^{t}AC). If a READ command is registered at a clock edge n, and the CAS latency is 2 clocks, the first data element will be valid at (n + 1^{t}CK + ^{t}AC).



Extended Mode Register definition

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include output drive strength selection, Temperature Compensated Self Refresh (TCSR) and Partial Array Self Refresh (PASR). TCSR and PASR are effective in Self Refresh mode only. The extended mode register is programmed via the LOAD MODE REGISTER command with BA0=0 and BA1=1, and the information won't be changed until it is reprogrammed, the device goes into deep power-down mode, or the device loses power. The EMRS must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation. Address bits A0-A2 specify PASR, A3-A4 the TCSR, A5-A6 the Drive Strength. A logic 0 should be programmed to all the undefined addresses bits to ensure future compatibility.

Temperature Compensated Self Refresh (TCSR)

On this version of the LPDDR SDRAM, the internal temperature sensor is implemented to adjust the self refresh oscillator automatically base on the case temperature. To maintain backward compatibility, the programming of TCSR bits no effect on the device. The address bits, A3 and A4 are ignore (don't care) during EMRS programming.

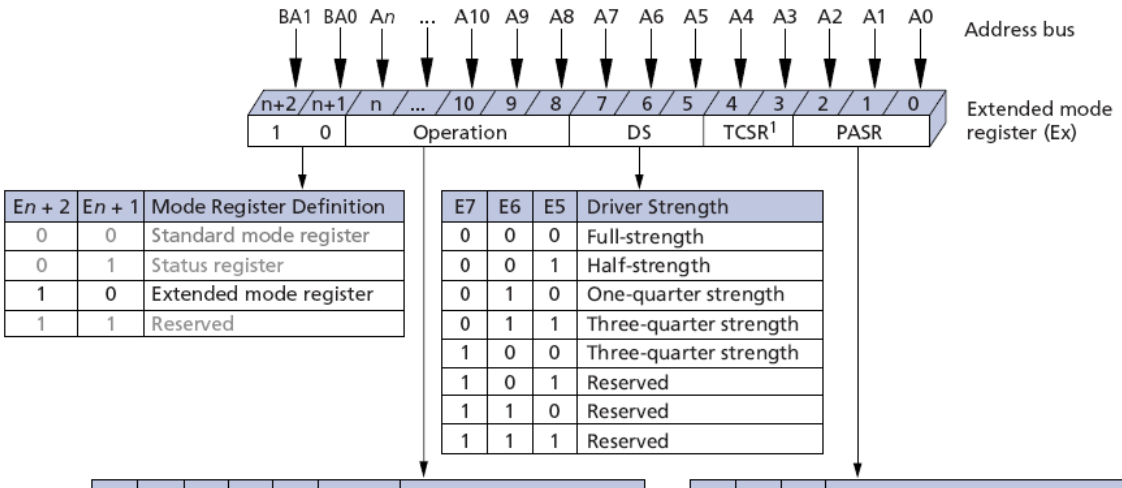
Partial-Array Self Refresh (PASR)

For further power savings during self refresh, the PASR feature may allow the self refresh to be restricted to a variable portion of the total array. They are full array (default: banks 0, 1, 2, and 3), 1/2 array (banks 0 and 1), 1/4 array (bank 0), 1/8 array (bank 0 with row

address MSB=0), and 1/16 array (bank 0 with row address MSB=0, and row address MSB-1=0). Data outside the defined area will be lost. Address bits A0 to A2 are used to set PASR.

Output Drive Strength

LPDDR SDRAM provides the option to control the drive strength of the output buffers for the smaller systems or point-to-point environments. The value was selected based on the expected loading of the memory bus. Total four values provided, and they are 25 ohm, 36ohm, 55ohm, and 80ohm internal impedance. They are full, three-quarter, one-half, and one-quarter drive strengths, respectively.



En + 2	En + 1	Mode Register Definition
0	0	Standard mode register
0	1	Status register
1	0	Extended mode register
1	1	Reserved

E7	E6	E5	Driver Strength
0	0	0	Full-strength
0	0	1	Half-strength
0	1	0	One-quarter strength
0	1	1	Three-quarter strength
1	0	0	Three-quarter strength
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

En	...	E10	E9	E8	E7–E0	
0	0	0	0	0	Valid	Normal AR Operation
–	–	–	–	–	–	All other states reserved

E2	E1	E0	Partial-Array Self Refresh Coverage
0	0	0	Full array
0	0	1	Half array
0	1	0	Quarter array
0	1	1	Reserved
1	0	0	Reserved
1	0	1	One-eighth array
1	1	0	One-sixteenth array
1	1	1	Reserved

Extended Mode Register

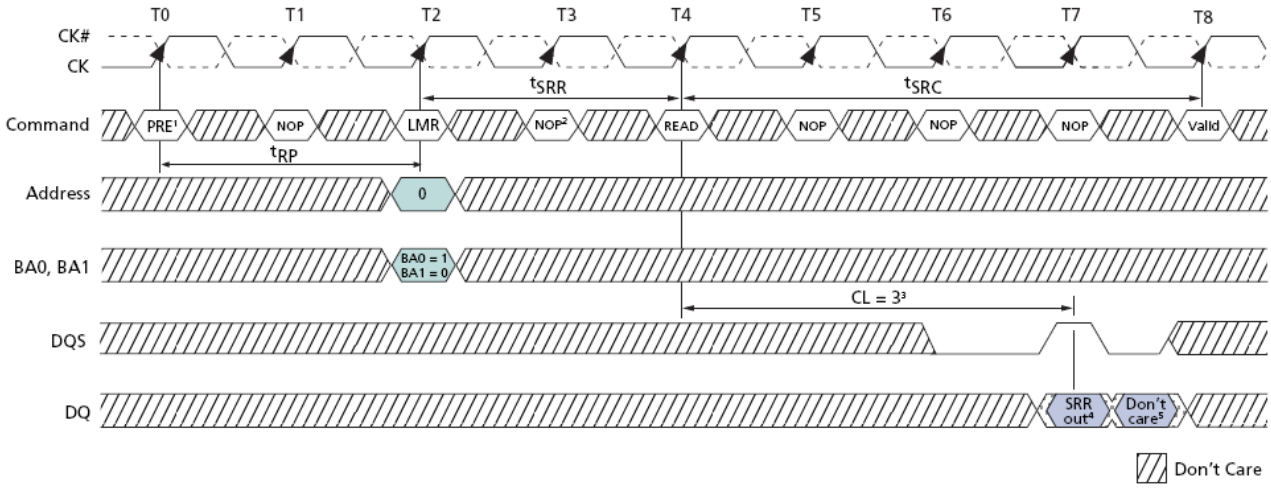
Notes:

1. On-die temperature sensor is used in place of TCSR. Setting these bits will have no effect.
2. The integer n is equal to the most significant address bit.

Status Read Register (SRR)

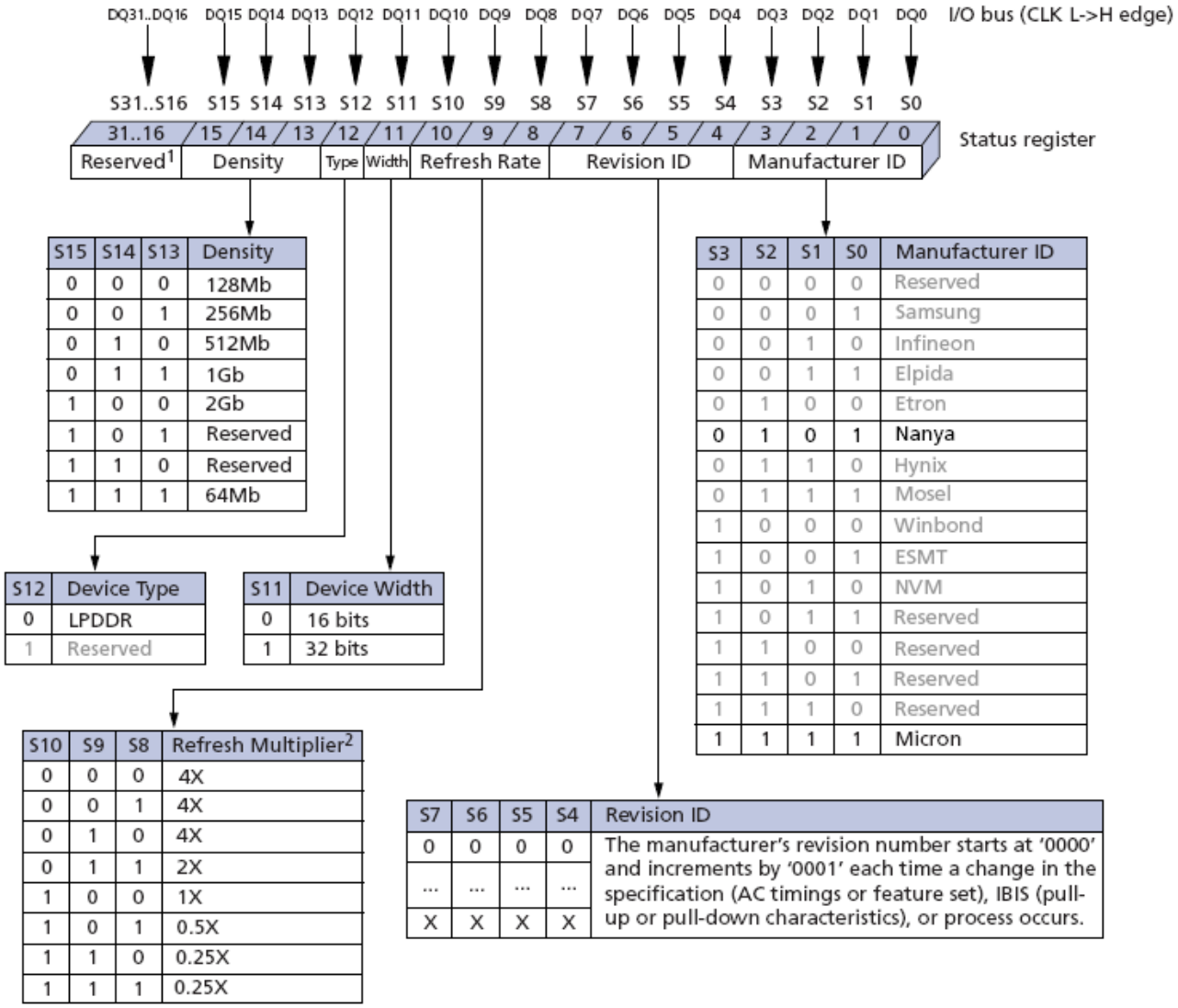
The status read register (SRR) is only for READ, and contains the specific die information such as density, device type, data bus width, refresh rate, revision ID and manufactures. The SRR is read via the LOAD MODE REGISTER command with BA0=1 and BA1=0. The sequence to perform an SRR command is as follows:

- The device had been properly initialized and in the idle or all banks precharge state.
- Issue a LMR command with BA [1:0] = "01".
- Wait ^{t}SRR; only NOP or DESELECT commands are supported during this period.
- Issue a READ command with all address pins set to "0".
- CAS latency cycles later, the device returns the registers data. The SRR read with fixed burst length 2, first bit of the burst output SRR data, and second bit of the burst is "Don't Care".
- The next command to the SDRAM must be issued ^{t}SRC after the SRR READ command is issued; only NOP or DESELECT commands are supported during this period.



Notes:

1. SRR can only be issued after power-up sequence is complete, and all banks are precharged and in the idle state.
2. NOP or DESELECT commands are required between LMR and READ command (^{t}SRR) and between READ and next VALID command (^{t}SRC)
3. CAS latency is predetermined by the programming of the mode register. Here CL=3 as an example only.
4. Burst length is fixed to 2 for SRR regardless of the value programmed by the mode register.
5. The second bit of the data-out burst is a "Don't Care".



S15	S14	S13	Density
0	0	0	128Mb
0	0	1	256Mb
0	1	0	512Mb
0	1	1	1Gb
1	0	0	2Gb
1	0	1	Reserved
1	1	0	Reserved
1	1	1	64Mb

S12	Device Type
0	LPDDR
1	Reserved

S11	Device Width
0	16 bits
1	32 bits

S10	S9	S8	Refresh Multiplier[2]
0	0	0	4X
0	0	1	4X
0	1	0	4X
0	1	1	2X
1	0	0	1X
1	0	1	0.5X
1	1	0	0.25X
1	1	1	0.25X

S3	S2	S1	S0	Manufacturer ID
0	0	0	0	Reserved
0	0	0	1	Samsung
0	0	1	0	Infineon
0	0	1	1	Elpida
0	1	0	0	Etron
0	1	0	1	Nanya
0	1	1	0	Hynix
0	1	1	1	Mosel
1	0	0	0	Winbond
1	0	0	1	ESMT
1	0	1	0	NVM
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Micron

S7	S6	S5	S4	Revision ID
0	0	0	0	The manufacturer's revision number starts at '0000' and increments by '0001' each time a change in the specification (AC timings or feature set), IBIS (pull-up or pull-down characteristics), or process occurs.
...	...	...	...	
X	X	X	X	

Status Register Definition

Notes:

1. Reserved bits should be set to zero for future compatibility.
2. Refresh multiplier is based on the memory device's on-board temperature sensor. Required average periodic refresh interval = ^{t}REFI x multiplier.

LPDDR SDRAM Command Description and Operation

Command Truth Table

NANE (Function)	Abbreviation	/CS	/RAS	/CAS	/WE	BA	A10/AP	ADDR	NOTES
DESELECT	DESELECT	H	X	X	X	X	X	X	2
NO OPERATION	NOP	L	H	H	H	X	X	X	2
ACTIVE (select bank and active row)	ACT	L	L	H	H	Valid	Row	Row	
READ (select bank, column, and start read burst)	READ	L	H	L	H	Valid	L	Col	
READ with AP (read burst with Auto Precharge)	READA	L	H	L	H	Valid	H	Col	3
WRITE (select bank, column, and start write burst)	WRITE	L	H	L	L	Valid	L	Col	
WRITE with AP (write burst with Auto Precharge)	WRITEA	L	H	L	L	Valid	H	Col	3
BURST TERMINATE or enter Deep Power-Down	BST	L	H	H	L	X	X	X	4,5
PRECHARGE (deactive row in selected bank)	PRE	L	L	H	L	Valid	L	X	6
PRECHARGE ALL (deactive rows in all banks)	PREALL	L	L	H	L	X	H	X	6
AUTO REFRESH or enter SELF REFRESH	REFA / REFS	L	L	L	H	X	X	X	7,8,9
LOAD MODE REGISTER	LMR	L	L	L	L	Valid	Op-code		10

Notes:

1. All states and sequences not shown are illegal or reserved.
2. DESELECT and NOP are functionally interchangeable.
3. Auto-precharge is non-persistent.. A10 High enables Auto Precharge, while A10 Low disables Auto-precharge.
4. Burst Terminate applies to only Read bursts with Auto0precharge disabled. This command is undefined and should not be used for Read with Auto-precharge enable, and for write bursts.
5. This command is BURST TERMINATE if CKE is High, and Deep Power-Down entry is CKE is Low.
6. If A10 is Low, bank address determines which bank is to be precharged. If A10 is High, all banks are precharged and BA0,BA1 are don't care.
7. This command is AUTO REFRESH is CKE is High, and SELF REFRESH if CKE is Low.
8. All address inputs and I/O are 'Don't care', except for CKE. Internal refresh counters control bank and row addressing.
9. All banks must be precharged before issuing an AUTO-REFRESH or SELF REFRESH command.
10. BA0 and BA1 value select between MRS, EMRS and SRR.
11. CKE is High for all commands shown, except SELF REFRESH and Deep Power-Down.

DM Operation Truth Table

Function	DM	DQ	Notes
Write Enable	L	Valid	1,2
Write Inhibit	H	X	1,2

Notes:

1. Used to mask write data, provided coincident with the corresponding data.
2. All states and sequences not shown are reserved and/or illegal.

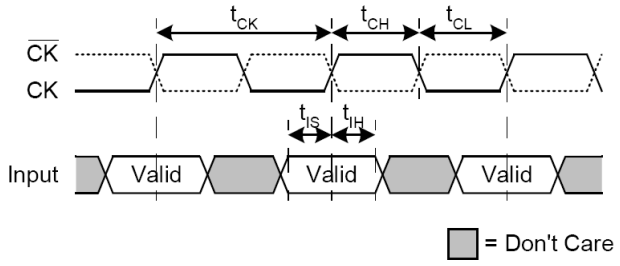
CKE Truth Table

Current State	CKE		Command (n) /RAS, /CAS, /WE, /CS	Action (n) -Result	Notes
	Previous Cycle (n-1)	Current Cycle (n)			
Power Down	L	L	X	Maintain Power Down	
Self Refresh	L	L	X	Maintain Self Refresh	
Deep Power Down	L	L	X	Maintain Deep Power Down	
Power Down	L	H	NOP or DESELECT	Exit Power Down	4,5,8
Self Refresh	L	H	NOP or DESELECT	Exit Self Refresh	4,6,9
Deep Power Down	L	H	NOP or DESELECT	Exit Deep Power Down	4,7
All Banks Idle	H	L	NOP or DESELECT	Precharge Power Down Entry	4
Bank(s) Active	H	L	NOP or DESELECT	Active Power Down Entry	4
All Banks Idle	H	L	AUTO REFRESH	Self Refresh Entry	
All Banks Idle	H	L	BURST TERMINATE	Deep Power Down Entry	
See the other Truth Tables	H	H	See the other Truth Tables		

Notes:

1. Current state is the state of LPDDR immediately prior to clock edge n.
2. Command(n) is the command registered at clock edge n, and Action(n) is the result of Command(n).
3. All states and sequences not shown are illegal or reserved.
4. DESELECT and NOP are functionally interchangeable.
5. Power Down exit time (^{t}XP) should elapse before a command other than NOP or DESELECT is issued.
6. SELF REFRESH exit time (^{t}XSR) should elapse before a command other than NOP or DESELECT is issued.
7. The Deep Power Down exit procedure must be followed as discussed in the Deep Power Down section..
8. The clock must toggle at least once during the ^{t}XP period.
9. The clock must toggle at least once during the ^{t}XSR period.
10. Upon exiting Deep Power Down mode, a full DRAM initialization sequence is required.

Basic Timing Parameters for Commands



Notes:

1. Input = A0 – An, BA0, BA1, CKE, /CS, /RAS, /CAS, /WE; An = Address bus MSB.

Current State Bank n Truth Table (command to Bank n)

Current State	Command					Action (n) -Result	Notes
	/CS	/RAS	/CAS	/WE	Description		
Any	H	X	X	X	DESELECT (NOP)	Continue previous operation	
	L	H	H	H	NOP	Continue previous operation	
Idle	L	L	H	H	ACTIVE	Select and Active row	
	L	L	L	H	AUTO REFRESH	Auto refresh	10
	L	L	L	L	MODE REGISTER SET	Mode register set	10
Row Active	L	H	L	H	READ	Select column & start read burst	
	L	H	L	L	WRITE	Select column & start write burst	
	L	L	H	L	PRECHARGE	Deactive row in bank or banks	4
READ (AP disable)	L	H	L	H	READ	Select column & start new read burst	5,6
	L	H	L	L	WRITE	Select column & start write burst	5,6,13
	L	L	H	L	PRECHARGE	Truncate read burst, start precharge	
	L	H	H	L	BURST TERMINTE	Burst terminate	11
WRITE (AP disable)	L	H	L	H	READ	Select column & start read burst	5,6,12
	L	H	L	L	WRITE	Select column & start new write burst	5,6
	L	L	H	L	PRECHARGE	Truncate write burst, start precharge	12

Notes:

1. The Table applies when both CKEn-1 and CKE are HIGH, and after ^{t}XSR or ^{t}XP has been met if the previous state was self refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
5. A command other than NOP should not be issued to the same bank while a READ or WRITE burst with Auto Precharge is enabled.
6. The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.
7. Current State Definitions:

   Idle: The bank has been precharged, and the ^{t}RP has been met.

   Row Active: A row in the bank has been activated, and ^{t}RCD had been met. No data bursts/accesses, register accesses in progress

   Read: A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
8. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or supported commands to the other bank, should be issued on any clock edge occurring during these states. Supported commands to any other bank are determined by that bank's current state.

   Precharging: Starts with registration of a PRECHARGE command, ends when ^{t}RP is met. Then the bank will be in idle state.

   Row Activating: Starts with registration of an AVTIVE command, ends when ^{t}RCD is met Then the bank will be in row active state

Read w/ AP enabled: Start with registration of a READ command with auto precharge enabled, ends when ^{t}RP has been met. Then the bank will be in the idle state.

Write w/ AP enabled: Start with registration of a WRITE command with auto precharge enabled, ends when ^{t}RP has been met. Then the bank will be in the idle state.

9. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.

   Refreshing: Starts with registration of an AUTO REFRESH command, ends when ^{t}RFC is met. Then all banks will be in idle state.

   Accessing Mode Register: Starts with registration of a LOAD MODE REGISTER command, ends when ^{t}MRD is met. Then all banks will be in idle state.

   Precharging All: Starts with registration of a PRECHARGE ALL command, ends when ^{t}RP is met. Then all banks will be in idle state

10. Not bank-specific; requires that all banks are idle and no bursts are in progress.
11. Not bank-specific; BURST TERMINATE affects the most recent read burst, regardless of bank.
12. Requires appropriate DM masking.
13. A WRITE command may be applied after the READ burst had been completed; otherwise, a BURST TERMINATE must be used to end the READ prior to asserting a WRITE command.

Current State Bank n Truth Table (command to Bank m)

Current State	Command					Action (n) -Result	Notes
	/CS	/RAS	/CAS	/WE	Description		
Any	H	X	X	X	DESELECT (NOP)	Continue previous operation	
	L	H	H	H	NOP	Continue previous operation	
Idle	X	X	X	X	ANY	Any command allowed to bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start read burst	8
	L	H	L	L	WRITE	Select column & start write burst	8
	L	L	H	L	PRECHARGE	Precharge	
READ (AP disable)	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start read burst	8
	L	H	L	L	WRITE	Select column & start write burst	8,10
	L	L	H	L	PRECHARGE	Precharge	
WRITE (AP disable)	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start read burst	8,9
	L	H	L	L	WRITE	Select column & start write burst	8
	L	L	H	L	PRECHARGE	Precharge	
Read (AP enabled)	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start read burst	5,8
	L	H	L	L	WRITE	Select column & start write burst	5,8,10
	L	L	H	L	PRECHARGE	Precharge	
Write (AP enabled)	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start read burst	5,8
	L	H	L	L	WRITE	Select column & start write burst	5,8
	L	L	H	L	PRECHARGE	Precharge	

Notes:

1. The Table applies when both CKEn-1 and CKE are HIGH, and after ^{t}XSR or ^{t}XP has been met if the previous state was self refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. Current State Definitions:

   Idle: The bank has been precharged, and the ^{t}RP has been met.

   Row Active: A row in the bank has been activated, and ^{t}RCD had been met. No data bursts/accesses, register accesses in progress

   Read: A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

5. The read with auto precharge enabled or write with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when ^{t}WR ends, with ^{t}WR measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or ^{t}RP) begins. The devices supports concurrent auto precharge such that when a read with auto precharge is enabled or a write with auto precharge is enabled, any command to other banks is supported, as long as that command does not interrupt the read or write data transfer already in progress. In either case, all other related limitations apply (for example, contention between read data and write data must be avoided). The minimum delay from a READ or WRITE command with auto precharge enabled to a command to a different bank is summarized below.

From Command	To Command	Min. delay (w/ concurrent Auto Precharge)
Write w/ AP	READ or READ w/ AP WRITE or WRITE w/ AP PRECHARGE ACTIVE	[1 + (BL/2)] ^{t}CK + ^{t}WTR (BL/2) ^{t}CK 1 ^{t}CK 1 ^{t}CK
READ w/ AP	READ or READ w/ AP WRITE or WRITE w/ AP PRECHARGE ACTIVE	(BL/2) ^{t}CK [CL + (BL/2)] ^{t}CK 1 ^{t}CK 1 ^{t}CK

6. AUTO REFRESH, SELF REFRESH, and LOAD MODE REGISTER commands may only be issued when all banks are idle.

7. A BURST TERMINATE command can not be issued to another bank; it applies to the bank represented by the current state only.

8. READs or WRITEs listed in the Command column include READs and WRITEs with Auto Precharge enabled and READs and WRITEs with Auto Precharge disabled.

9. Requires appropriate DM masking.

10. A WRITE command may be only be applied after the completion of data output, otherwise a BURST TERMINATE command must be issued to end the READ prior to asserting a WRITE command.

COMMAND

NO OPERATION (NOP)

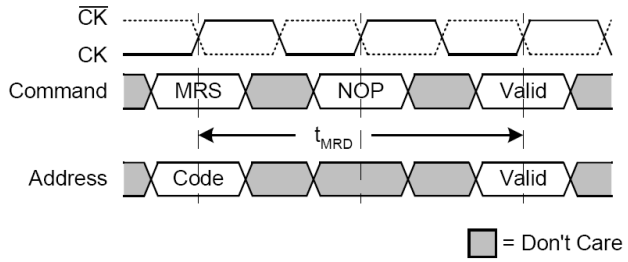
The No operation (NOP) command is used to instruct the selected LPDDR SDRAM to perform a NOP. This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

DESELECT

The Deselect function (/CS=HIGH) prevents new commands from being executed by the LPDDR SDRAM. Operations already in progress are not affected.

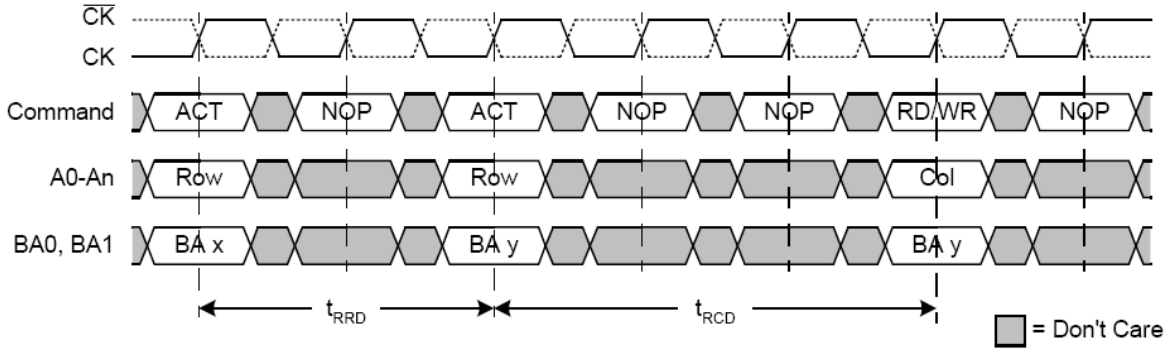
LOAD MODE REGISTER

The mode registers are loaded via the address inputs and can only be issued when all banks are idle, no bursts are in progress. The subsequent executable command can not be issued until ^{t}MRD is met.



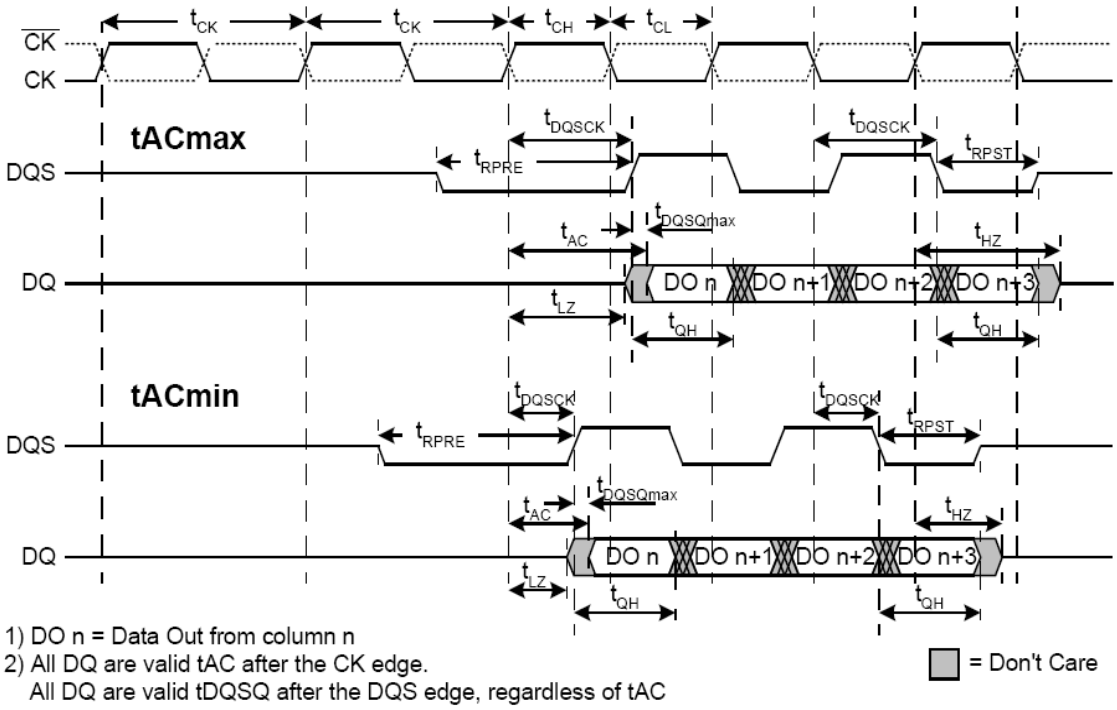
ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for subsequent access. The values on the BA0 and BA1 inputs select the bank, and the addresses provided on inputs A0-A13 selects the row. Once a row is open, a READ or WRITE command could be issued to that row, subject to the ^{t}RCD specification. A subsequent ACTIVE command to another row in the same bank can only be issued after the previous row has been closed. The minimum time interval between two successive ACTIVE commands on the same bank is defined by ^{t}RC. The subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between two successive ACTIVE commands on different banks is defined by ^{t}RRD. These rows remain active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.



READ

The READ command is used to initiate a burst read access to an active row, with a burst length as set in the Mode Register. BA0 and BA1 select the bank, and the address inputs select the starting column location. The value of A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses. During Read bursts, DQS is driven by the LPDDR SDRAM along with the output data. The initial Low state of the DQS is known as the read preamble; the Low state coincident with last data-out element is known as the read postamble. The first data-out element is edge aligned with the first rising edge of DQS and the successive data-out elements are edge aligned to successive edges of DQS.

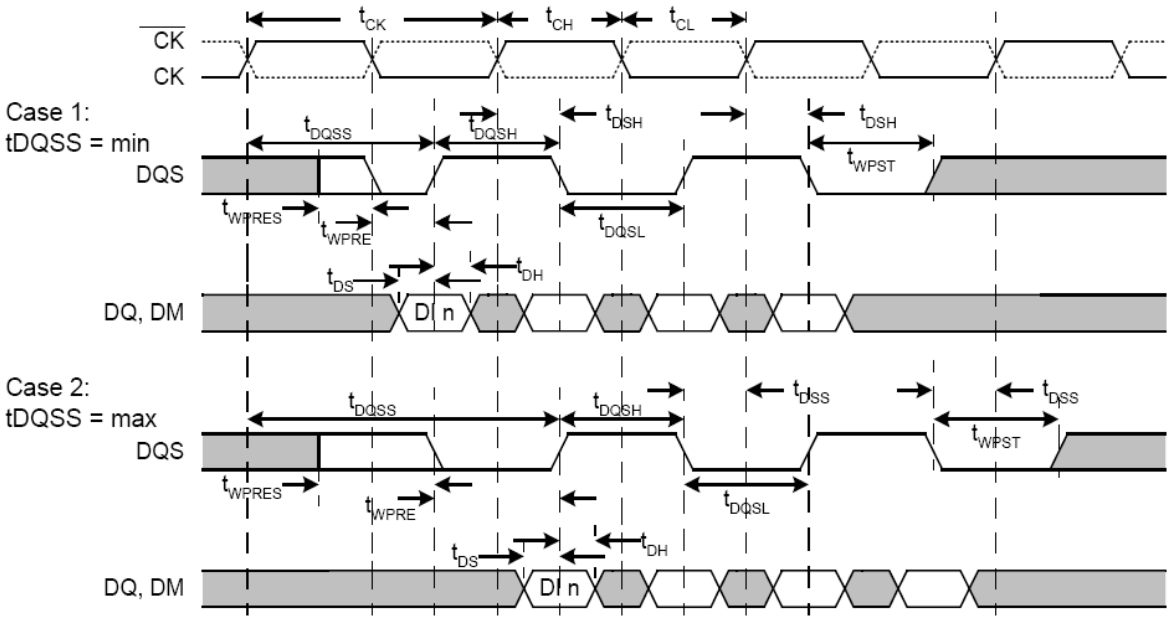


1) DO n = Data Out from column n
2) All DQ are valid tAC after the CK edge.
All DQ are valid tDQSQ after the DQS edge, regardless of tAC

= Don't Care

WRITE

The WRITE command is used to initiate a burst write access to an active row, with a burst length as set in the Mode Register. BA0 and BA1 select the bank, and the address inputs select the starting column location. The value of A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location. During Write bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and the subsequent data elements will be registered on successive edges of DQS. The Low state of DQS between the WRITE command and the first rising edge is called the write preamble; the Low state on DQS following the last data-in element is called write postamble.



1) DI n = Data In for column n
2) 3 subsequent elements of Data In are applied in the programmed order following DI n.
3) tDQSS: each rising edge of DQS must fall within the ± 25% window of the corresponding positive clock edge.

= Don't Care

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged. In case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care”. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

AUTO PRECHARGE

Auto Precharge is a feature which performs the same individual bank precharge function, but without requiring an explicit command. This is accomplished by using A10 (A10=High), to enable Auto Precharge in conjunction with a specific READ or WRITE command. A precharge of the bank / row that is addressed with the READ or WRITE command is automatically performed upon completion of the read or write burst. Auto precharge is non persistent in that it is either enabled or disabled for each individual READ or WRITE command. Auto precharge ensures that a precharge is initiated at the earliest valid stage within a burst.

BURST TERMINATE

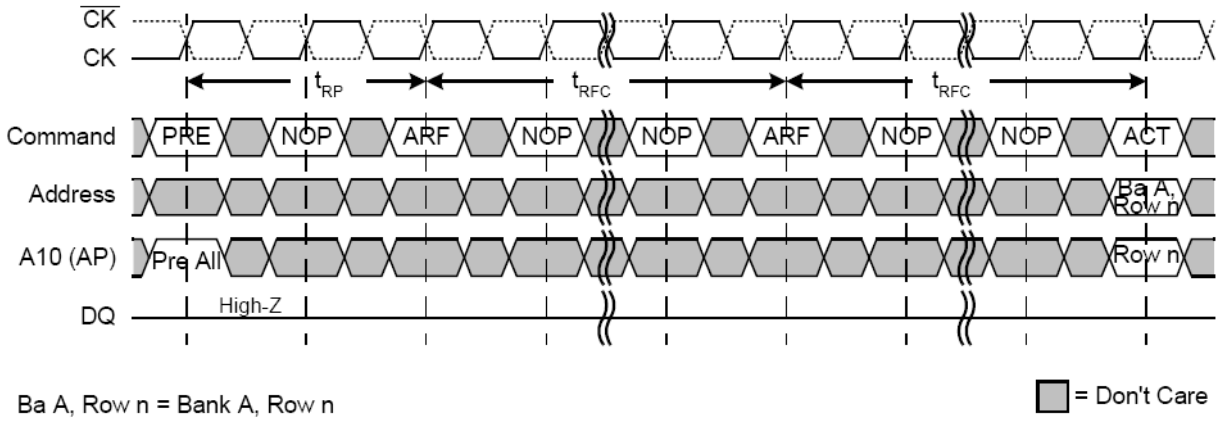
The BURST TERMINATE command is used to truncate read bursts with auto precharge disabled. The most recently registered READ command prior to the BURST TERMINATE command will be truncated. The BURST TERMINATE command is not bank specific, and should not be used to terminate write bursts.

REFRESH

LPDDR SDRAM devices require a refresh of all rows in any rolling 64ms interval. Each refresh is generated in one of two ways: by an explicit AUTO REFRESH command, or by an internally timed event in SELF REFRESH mode:

- AUTO REFRESH

AUTO REFRESH command is used during normal operation of the LPDDR SDRAM, and it's non-persistent, so it must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller. The address bits become "Don't Care" during AUTO REFRESH. The LPDDR SDRAM requires AUTO REFRESH commands at an average periodic interval of ^{t}REFI. To provide improved efficiency in scheduling and switching between tasks, some flexibility in the absolute interval is provided. The auto refresh period begins when the AUTO REFRESH command is registered and ends ^{t}RFC later.

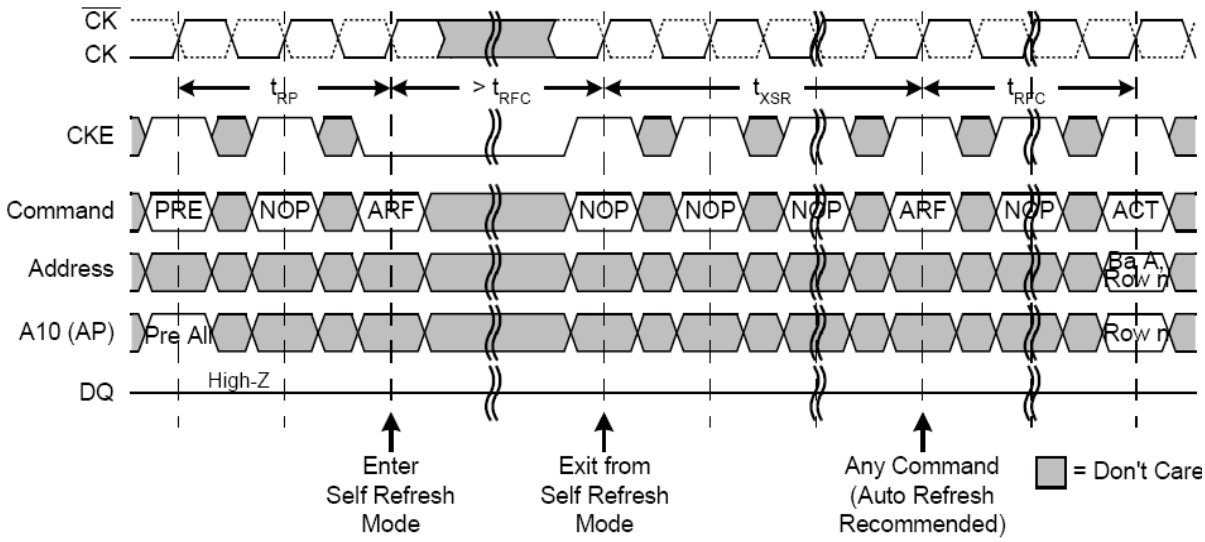


- SELF REFRESH

SELF REFRESH command can be used to retain data in the LPDDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the LPDDR SDRAM retains data without external clocking. The LPDDR SDRAM device has a built-in timer to accommodate Self Refresh operation. The SELF REFRESH command is initiated like an AUTO REFRESH command, except CKE is LOW. Input signals except CKE are "Don't Care" during Self Refresh. Once the SELF REFRESH command is registered, the external clock can be halted after one clock later. CKE must be held low to keep the device in Self Refresh mode, and internal clock also disabled to save power. The minimum time that the device must remain in Self Refresh mode is ^{t}RFC.

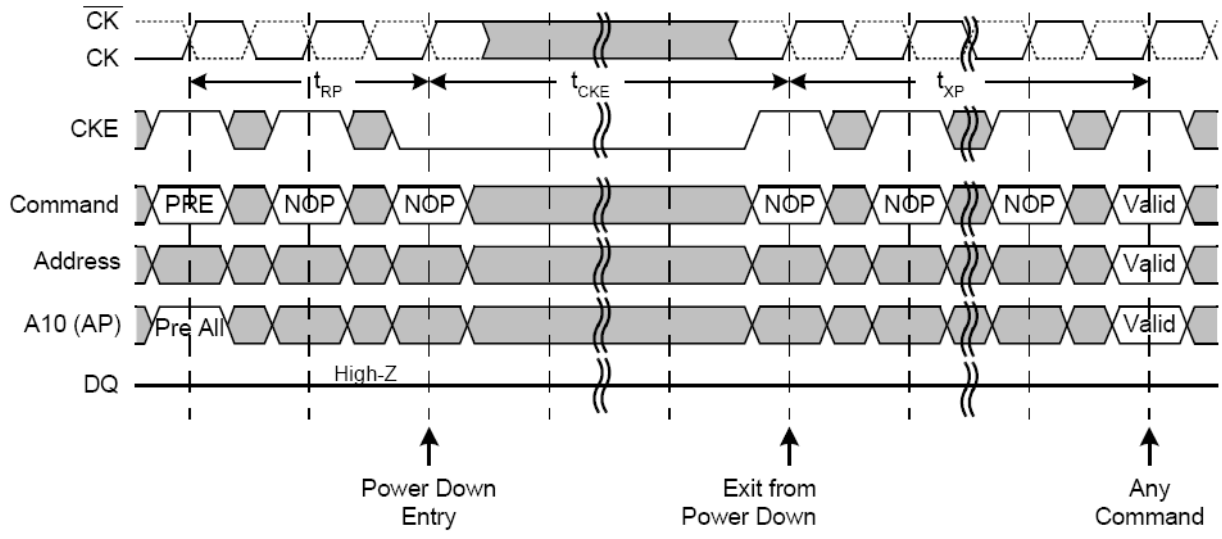
In the Self Refresh mode, two additional power-saving options exist: Temperature Compensated Self Refresh and Partial Array Self Refresh. During this mode, the device is refreshed as identified in the extended mode register. An internal temperature sensor will adjust the refresh rate to optimize device power consumption while ensuring data integrity. During SELF REFRESH operation, refresh intervals are scheduled internally and may vary. These refresh intervals may be different then the specified ^{t}REFI time. For this reason, the SELF REFRESH command must not be used as a substitute for the AUTO REFRESH command.

The procedure for exiting SELF REFRESH requires a sequence of commands. First, CK must be stable prior to CKE going back HIGH. When CKE is HIGH, the LPDDR SDRAM must have NOP commands issued for ^{t}XSR time.



Power-Down

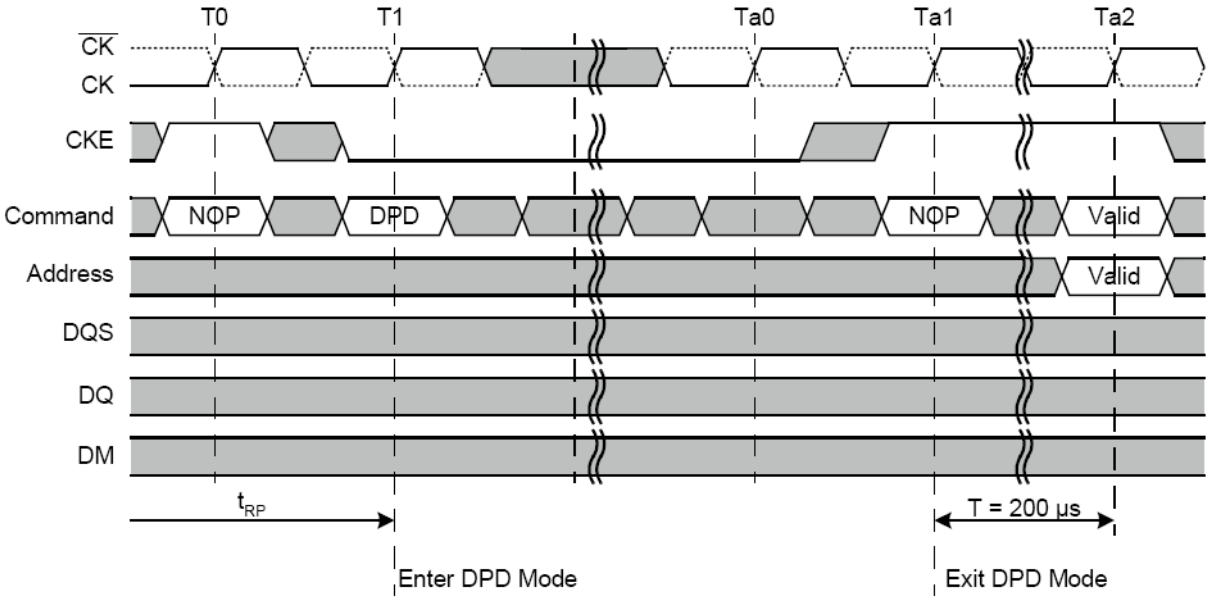
Power-down is entered when CKE is registered Low (no accesses can be in progress). If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Power-down mode deactivates the input and output buffers, excluding CK, /CK and CKE. CKE keep Low to maintain device in the power-down mode, and all other inputs signals are “Don’t Care”. The minimum power-down duration is specified by ^{t}CKE. The device can not stay in this mode for longer than the refresh requirements of the device, without losing data. The power-down state is synchronously existed when CKE is registered High (along with a NOP or DESELECT command). A valid command can be issued after ^{t}XP after exist from power-down.



Precharge Power-Down mode shown: all banks are idle and t_{RP} is met when Power-Down Entry command is issued

Deep-Power-Down

The Deep Power-Down (DPD) mode enables very low standby currents. All internal voltage generators inside the LPDDR SDRAM are stopped and all memory data, MRS and EMRS information is lost in this mode. The DPD command is the same as a BURST TERMINATE command with CKE LOW. All banks must be in idle state with no activity on the data bus prior to entering the DPD mode. While in this mode, CKE must be held in a constant Low state. To exit the DPD mode, CKE is taken high after the clock is stable and NOP commands must be maintained for at least 200us. After 200us a complete re-initialization is required.



1) Clock must be stable before exiting Deep Power-Down mode. That is, the clock must be cycling within specifications by Ta0
2) Device must be in the all banks idle state prior to entering Deep Power-Down mode
3) 200µs is required before any command can be applied upon exiting Deep Power-Down mode
4) Upon exiting Deep Power-Down mode a PRECHARGE ALL command must be issued, followed by two AUTO REFRESH commands and a load mode register sequence

= Don't Care

Clock Stop

Stopping a clock during idle periods is an effective method of reducing power consumption. The LPDDR SDRAM supports clock stop mode under the following conditions:

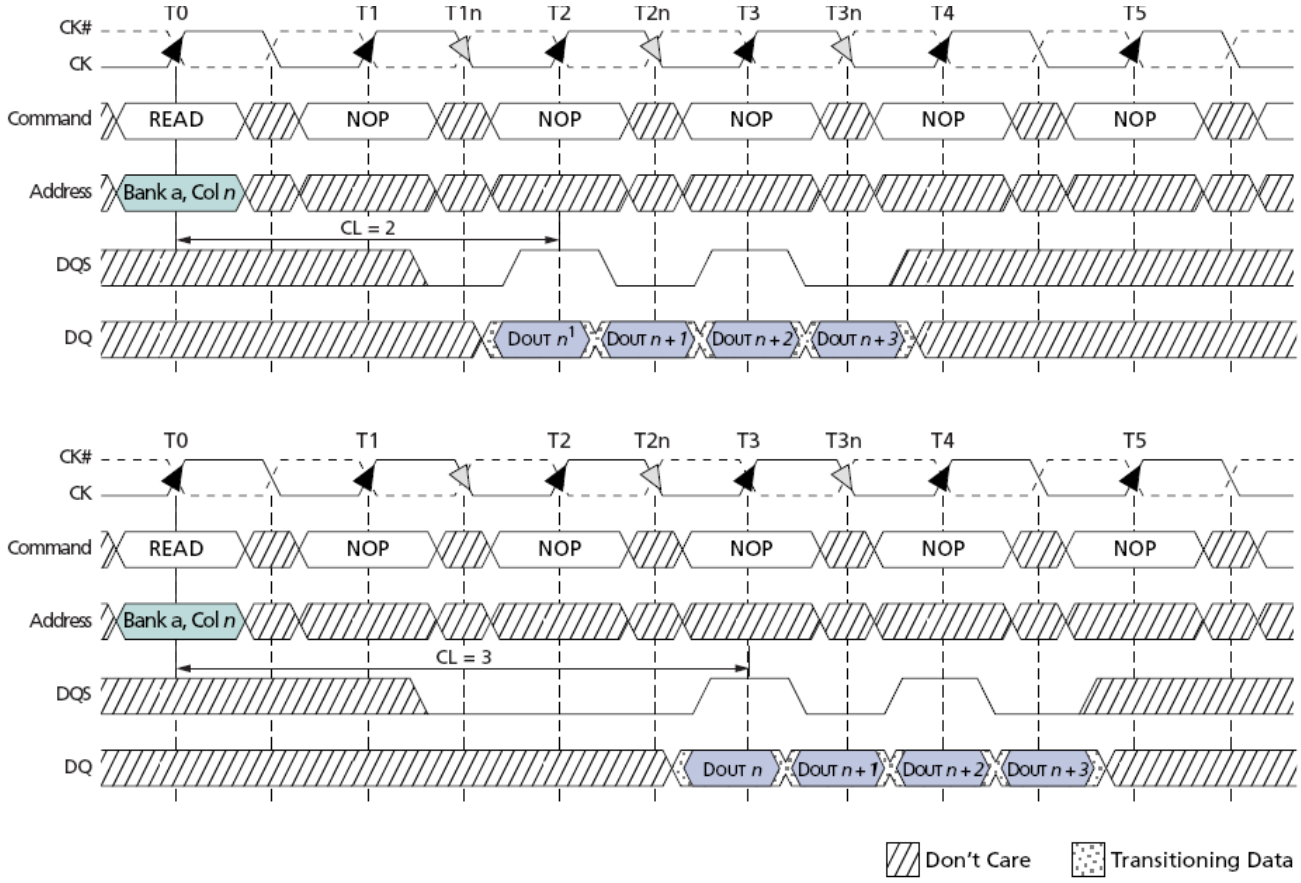
- The last command (ACTIVE, READ, WRITE, PRECHARGE, AUTO REFRESH or MODE REGISTER SET) has executed to completion, including any data-out during read bursts; the number of clock pluses per access command depends on the device's AC timing parameters and the clock frequency;
- The related timing condition (^{t}RCD, ^{t}WR, ^{t}RP, ^{t}RFC, ^{t}MRD) has been met;
- CKE is held High.

When all conditions have been met, the device is either in "idle state" or "row active state", and clock stop may be entered with CK held Low and /CK held High. Clock Stop mode is exited by restarting the clock. At least one NOP command has to be issued before the next access command may be applied. Additional clock pulses might be required depending on the system characteristics.

Timing

READs

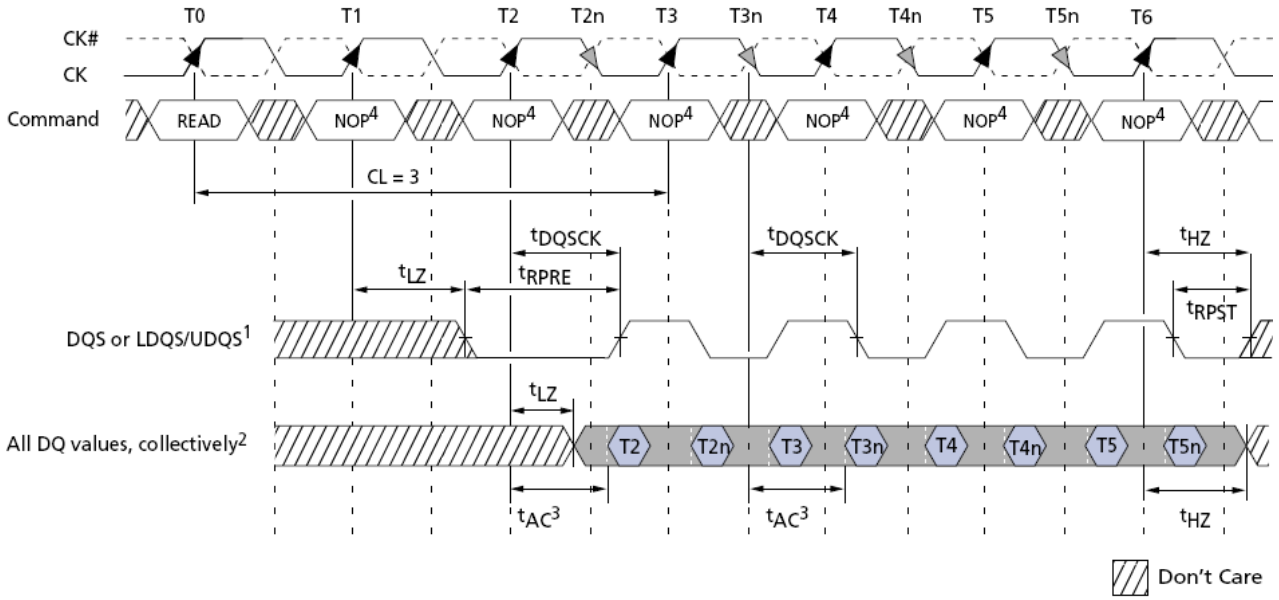
READ burst operations are initiated with a READ command. The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. The first data-out element is edge aligned with the first rising edge of DQS and the successive data-out elements are edge aligned to successive edges of DQS. DQS is driven by LPDDR SDRAM along with output data. Upon completion of a read burst, assuming no other READ command has been initiated, the DQ will go to High-Z.



Read Burst Operation (BL=4, and CL=2, CL=3)

Notes:

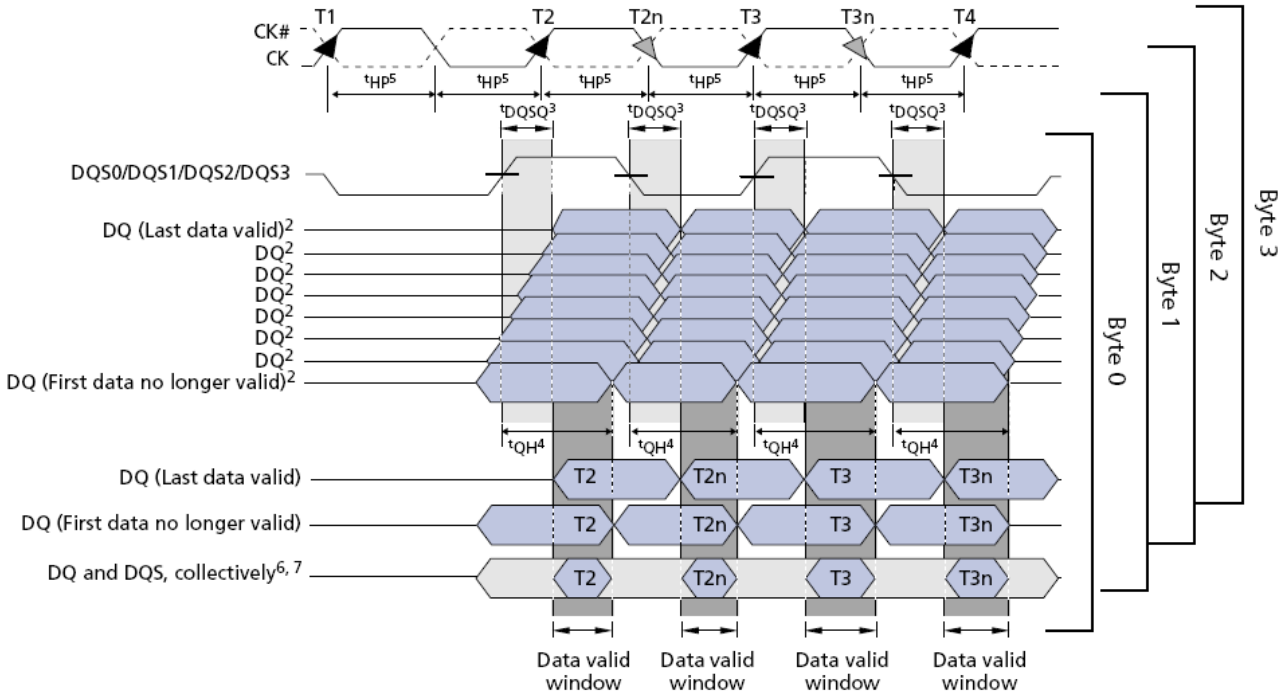
1. Dout n = data-out from column n.
2. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.



Data Output Timing – ^{t}AC and ^{t}DQSCK

Notes:

1. DQ transitioning after DQS transitions define ^{t}DQSQ window.
2. All DQ must transition by ^{t}DQSQ after DQS transitions, regardless of ^{t}AC.
3. ^{t}AC is the DQ output window relative to CK and is the "long-term" component of DQ skew.
4. Commands other than NOP may be valid during this cycle.

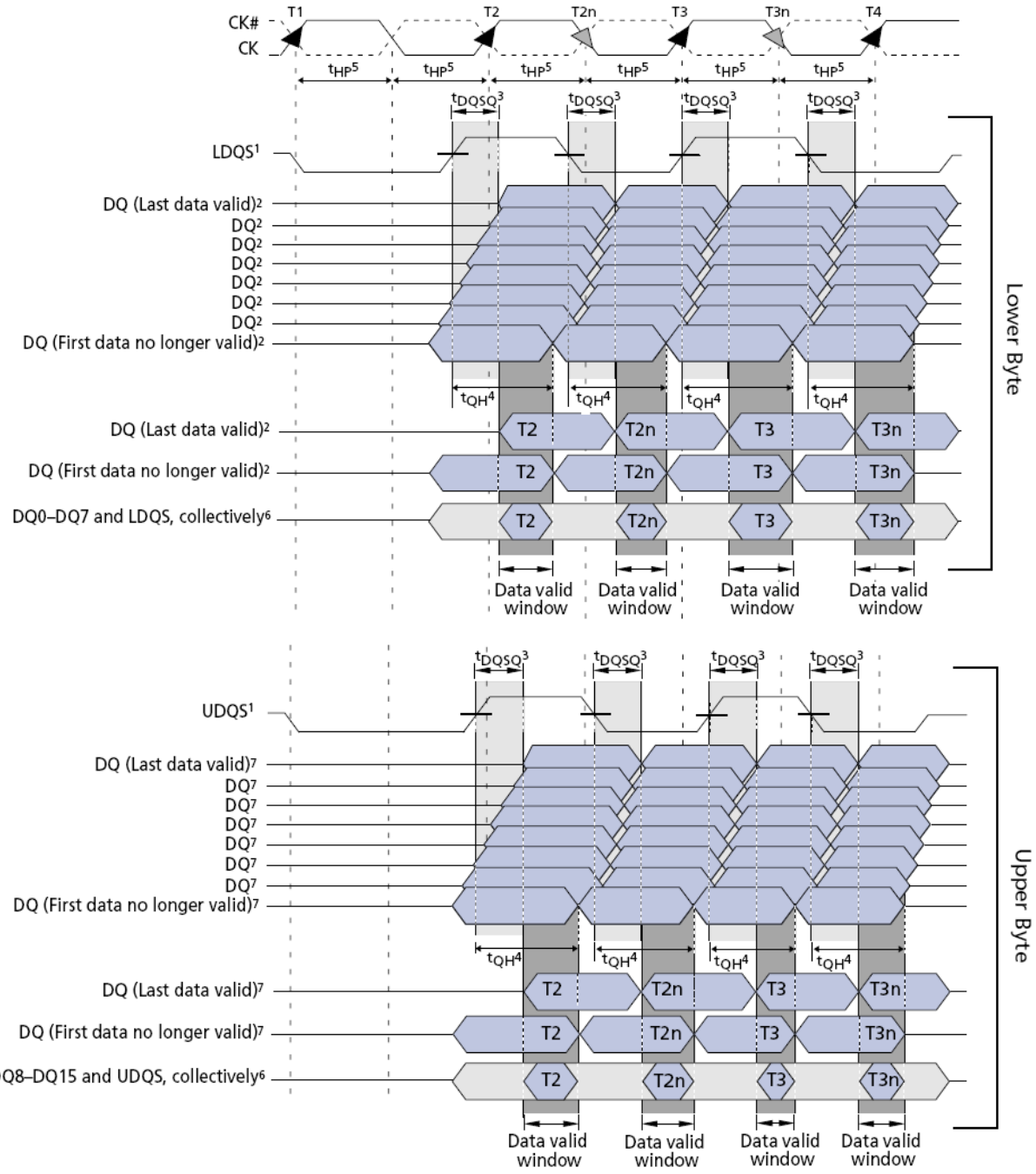


Data Output Timing – ^{t}DQSQ, ^{t}QH and Data Valid Window (x32)

Notes:

1. DQ transitioning after DQS transitions define ^{t}DQSQ window.

2. Byte 0 is DQ0-DQ7, Byte 1 is DQ8-DQ15, Byte 2 is DQ16-DQ23, and Byte 3 is DQ24-DQ31.
3. ^{t}DQSQ is derived at each DQS clock edge and is not cumulative over time and begins with DQS transition and ends with the last valid DQ transition .
4. ^{t}OH is derived from ^{t}HP, ^{t}OH = ^{t}HP - ^{t}OHS.
5. ^{t}OH is the lesser of ^{t}CL or ^{t}CH clock transition collectively when a bank is active.
6. The data valid window is derived from each DQS transition and is ^{t}OH – ^{t}DQSQ.
7. DQ[7:0] and DQS0 for byte 0; DQ[15:8] and DQS1 for byte 1; DQ[23:16] and DQS2 for byte 2; DQ[31:24] and DQS3 for byte 3.



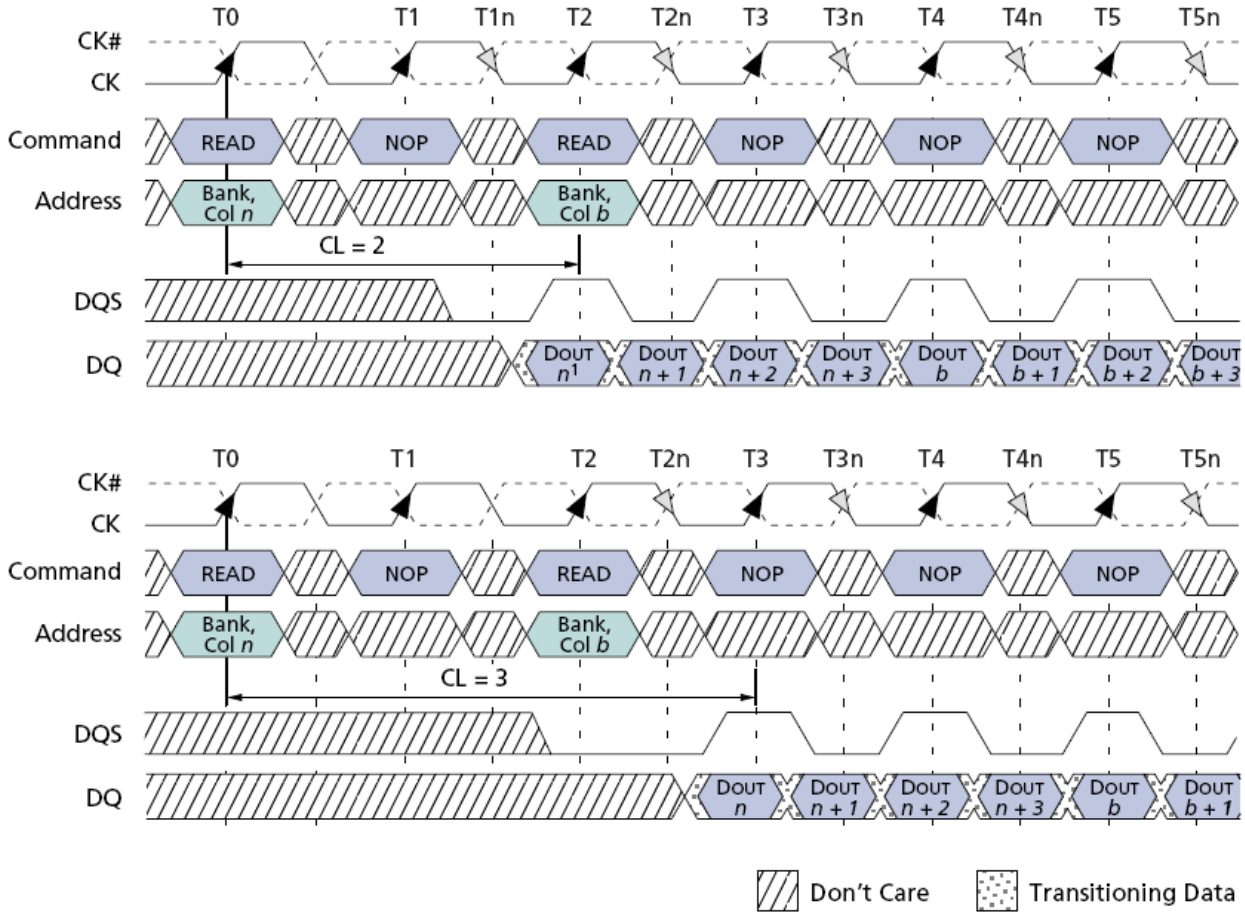
Data Output Timing – ^{t}DQSQ, ^{t}QH and Data Valid Window (x16)

Notes:

1. DQ transitioning after DQS transitions define ^{t}DQSQ window. LDQS defines the lower byte and UDQS defines the upper byte.
2. DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, or DQ7.
3. ^{t}DQSQ is derived at each DQS clock edge and is not cumulative over time and begins with DQS transition and ends with the last valid DQ transition .
4. ^{t}OH is derived from ^{t}HP, ^{t}OH = ^{t}HP - ^{t}OHS.
5. ^{t}OH is the lesser of ^{t}CL or ^{t}CH clock transition collectively when a bank is active.
6. The data valid window is derived from each DQS transition and is ^{t}OH – ^{t}DQSQ.
7. DQ9, DQ9, DQ10, DQ11, DQ12, DQ13, DQ14, or DQ15.

READ to READ

Data from a read burst may be concatenated or truncated by a subsequent READ command. The first data from the new burst follows either the last element of a completed burst or the last desired element of a longer burst that is being truncated. The new READ command should be issued X cycles after the first READ command, where X equals the number of desired data-out element pairs (pairs are required by the 2n prefetch architecture).

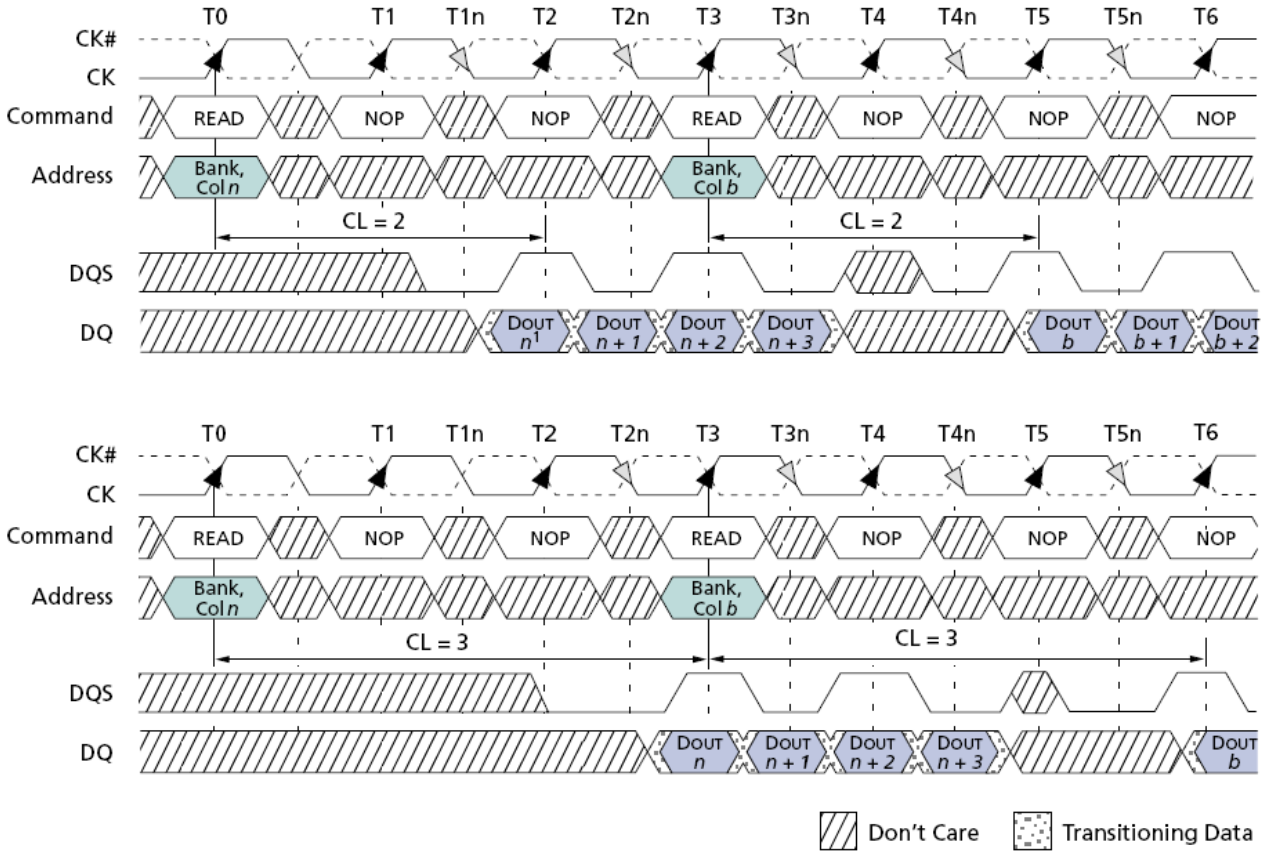


Consecutive Read Bursts (CL=2 and CL=3)

Notes:

1. Dout n (or b) = data-out from column n (or column b).

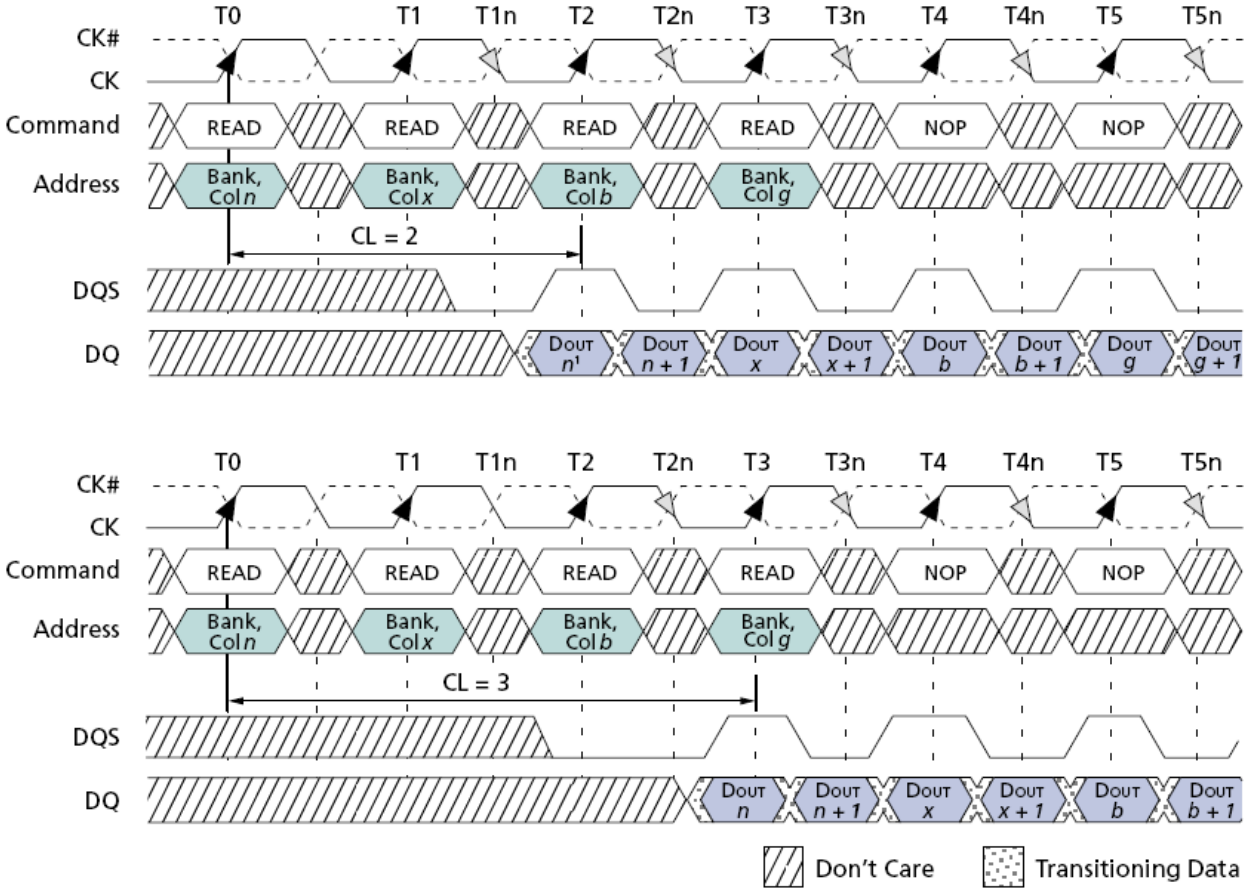
2. BL = 4, 8, or 16 (if 4, the bursts are concatenated; if 8 or 16, the second burst interrupts the first).
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.



Nonconsecutive Read Bursts (CL=2 and CL=3)

Notes:

1. Dout n (or b) = data-out from column n (or column b).
2. BL = 4, 8, or 16 (if 4, the bursts are concatenated; if 8 or 16, the second burst interrupts the first).
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.



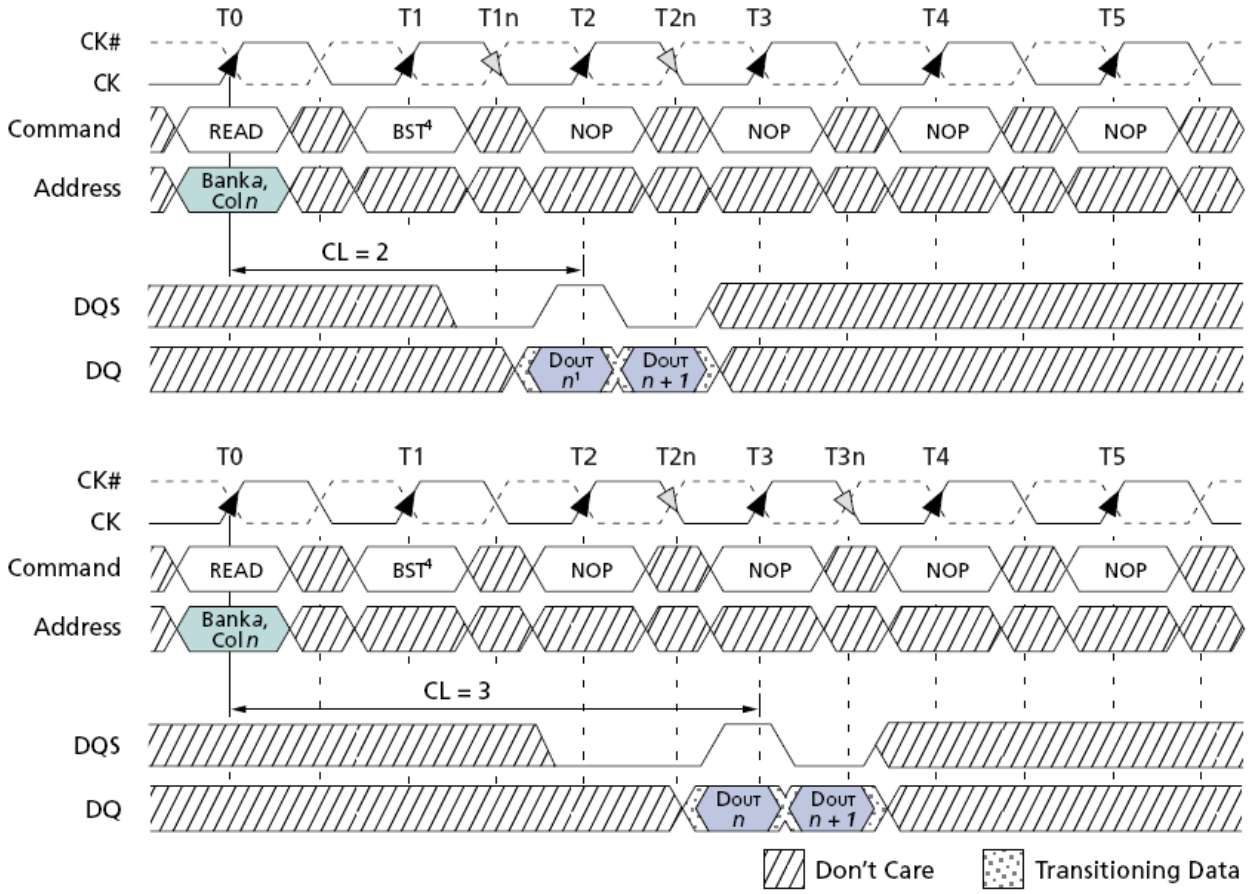
Random Read Bursts (CL=2 and CL=3)

Notes:

1. Dout n (or x, b, g) = data-out from column n (or column x, column b, column g).
2. BL = 2, 4, 8, or 16 (if 4, 8 or 16, the following burst interrupts the previous).
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

READ BURST TERMINATE

Data from any READ burst may be truncated with a BURST TERMINATE command. The BURST TERMINATE latency is equal to read (CAS) latency, i.e., the BURST TERMINATE command should be issued X cycles after the READ command where X equals the desired data-out element pairs (pairs are required by the 2n-prefetech architecture).



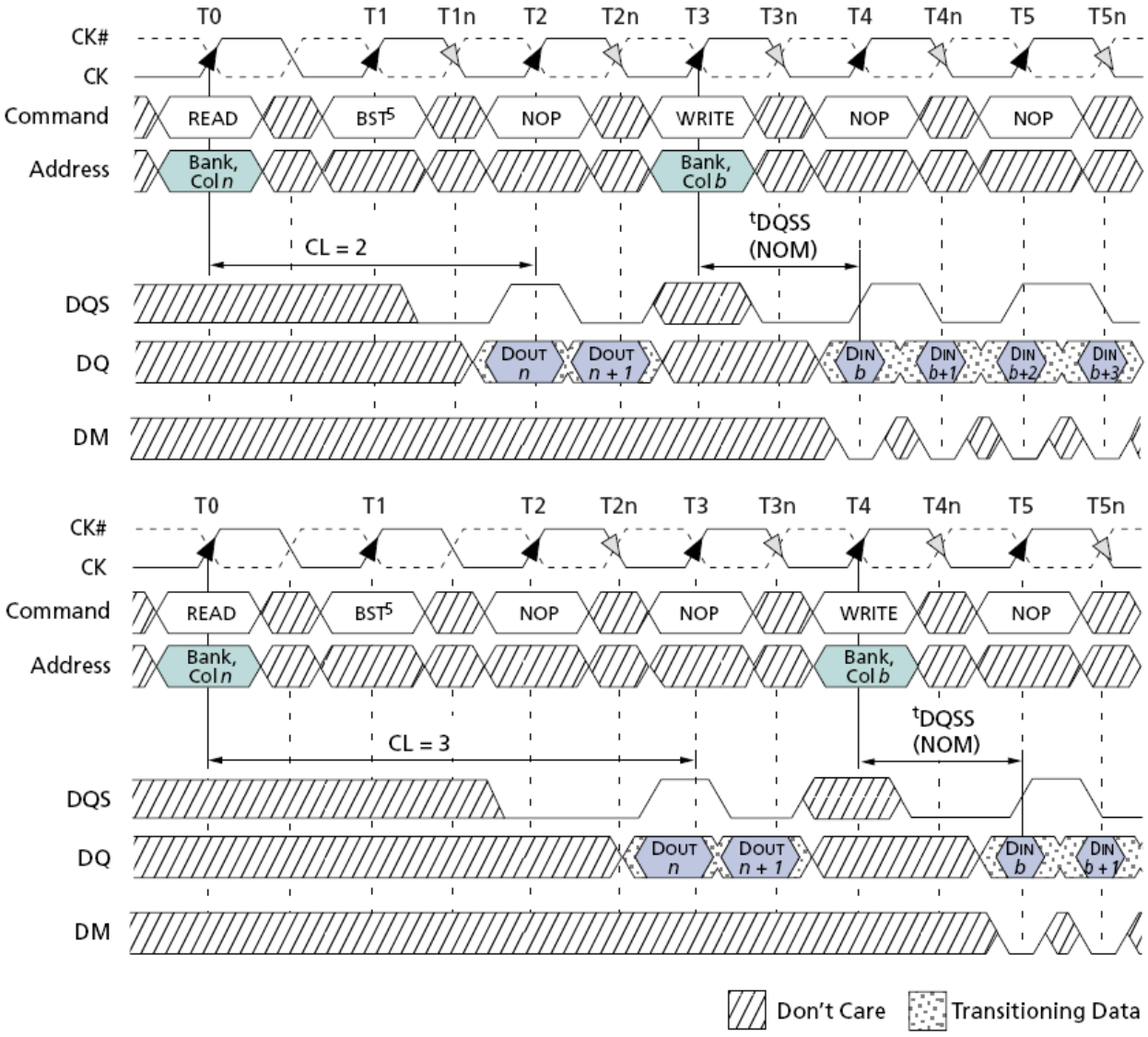
Terminating a Read Bursts (CL=2 and CL=3)

Notes:

1. Dout n = data-out from column n.
2. BL = 4, 8, or 16.
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
4. BST = BURST TERMINATE command; page remains open.
5. CKE = HIGH.

READ to WRITE

Data from READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used.



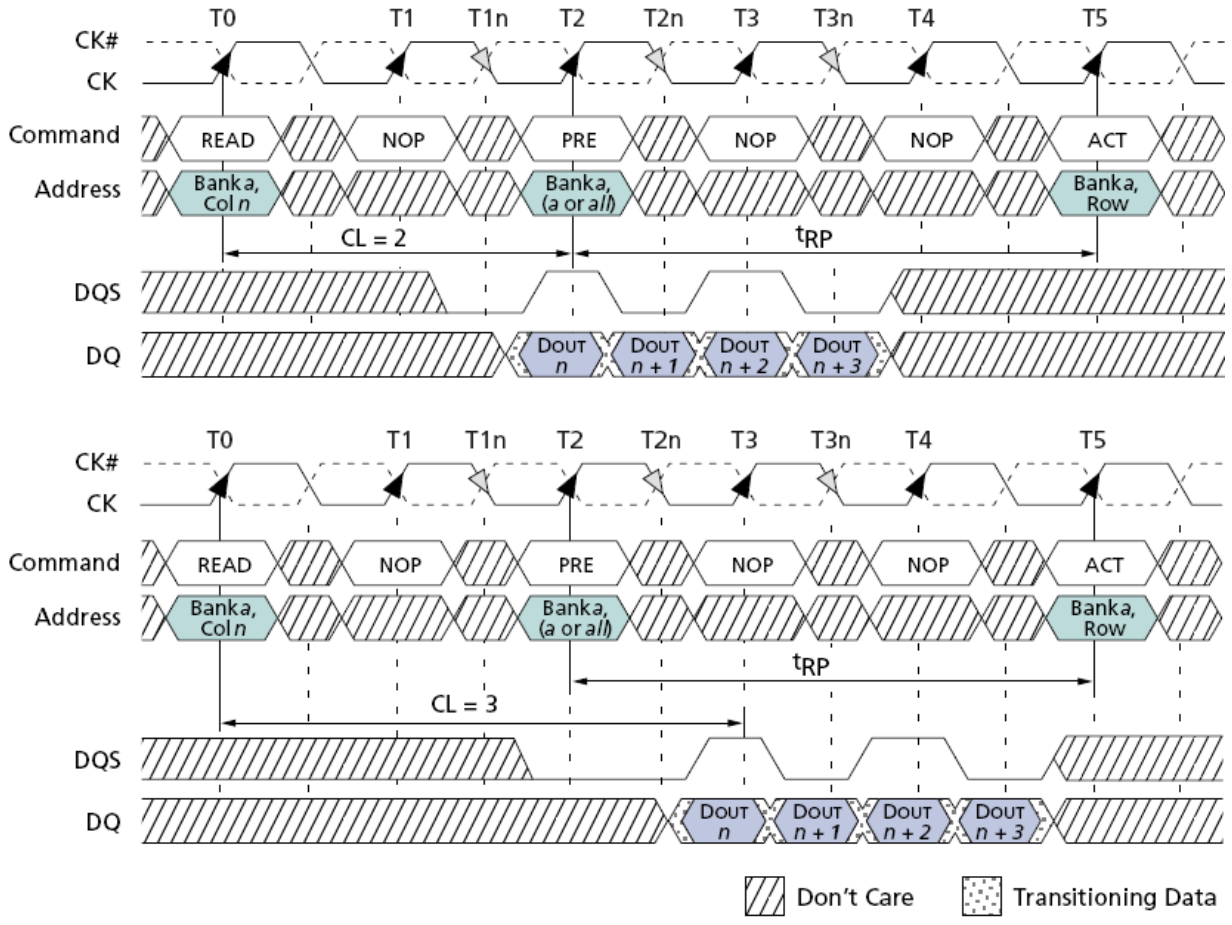
Read to Write (CL=2 and CL=3)

Notes:

1. Dout n = data-out from column n.
2. BL = 4, 8, or 16.
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
4. BST = BURST TERMINATE command; page remains open.
5. CKE = HIGH.

READ to Precharge

A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank. The PRECHARGE command should be issued X cycles after the READ command, where X equals the number of desired data element pairs. Following the PRECHARGE command, a subsequent command to the same bank can not be issued until ^{t}RP is met. Part of the row precharge time is hidden during the access of the last data element. In the case of a READ being executed to completion, a PRECHARGE command issued at optimum time provides the same operation as READ with AP. The disadvantage of PRECHARGE command is that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that can be used to truncate bursts.



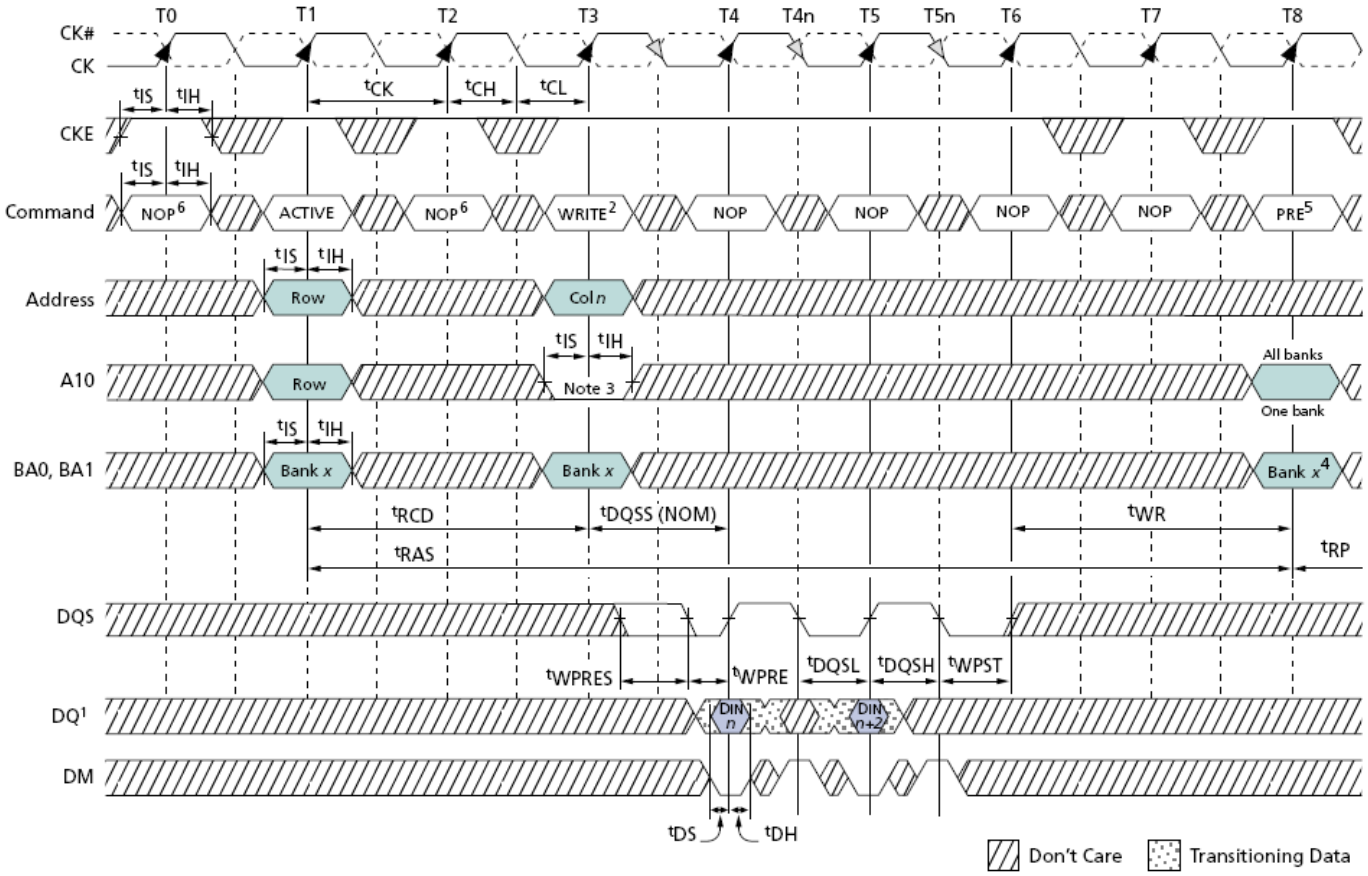
Read to Precharge (CL=2 and CL=3)

Notes:

1. Dout n = data-out from column n.
2. BL = 4, or an interrupted burst 8 or 16.
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
4. READ-to-PRECHARGE equals 2 clocks, which enables 2 data pairs of data-out. A READ command with auto precharge enabled, provided ^{t}RAS (min) is met, would cause a precharge to be performed at X number of clock cycles after the READ command, where x = BL/2.
5. PRE = PRECHARGE command; ACT = ACTIVE command.

WRITEs

WRITE burst operations are initiated with a WRITE command. The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and subsequent data elements will be registered on successive edges of DQS. Input data appearing on the data bus is written to the memory array subject to the state of the data mask DM inputs coincident with the data.



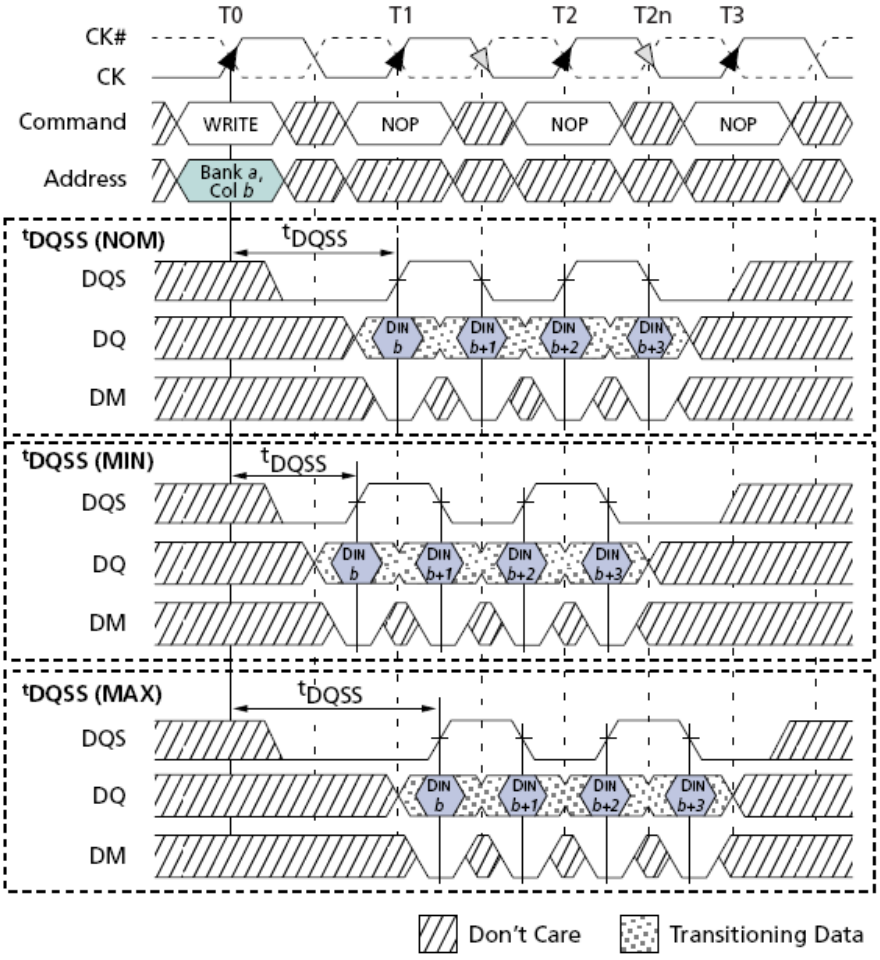
Write – DM Operation (CL=2 and CL=3)

Notes:

1. Din n = data-in from column n.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. Bank x at T8 is "Don't Care", if A10 is HIGH at T8.
5. PRE = PRECHARGE command.
6. NOP commands are shown for ease of illustration; other commands may be valid at these time.

WRITE Burst

The time between the WRITE command and the first corresponding rising edge of DQS (^{t}DQSS) is specified with a relatively wide range (from 75% to 125% of one clock cycle). All of the WRITE diagrams show the nominal case, and where the two extreme cases (that is, ^{t}DQSS(min) and ^{t}DQSS(max)) might not be intuitive, they have also been included. Upon completion of the burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored.



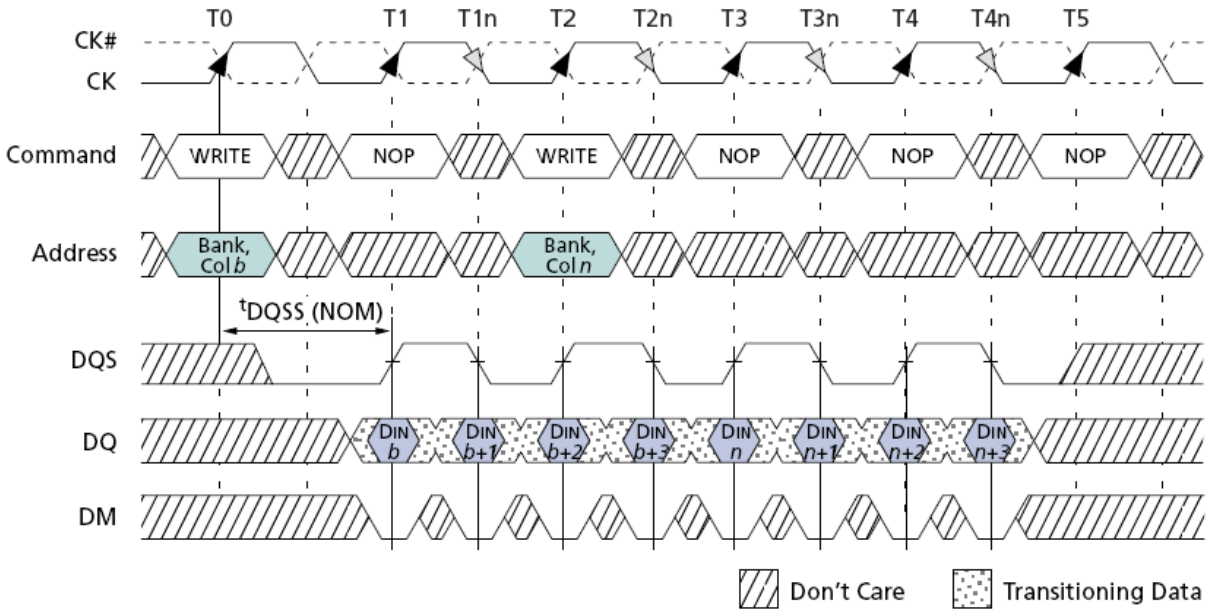
Write burst (nominal, ^{t}DQSS(min)/(max), BL=4)

Notes:

1. Din b = data-in from column b.
2. An uninterrupted burst of 4 is shown.
3. A10 is LOW with the WRITE command (Auto Precharge is disabled).

WRITE to WRITE

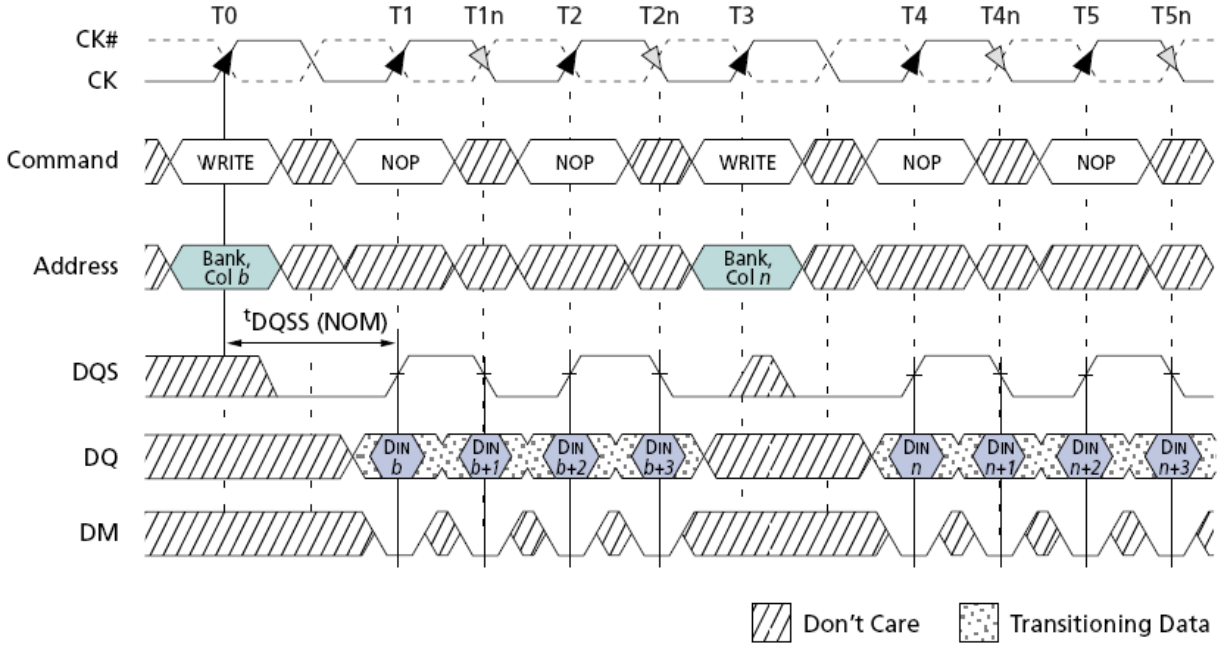
Data for any WRITE burst may be concatenated with or truncated by a subsequent WRITE command. In either case, a continuous flow input data can be maintained. The new WRITE command can be issued on any positive edge of the clock following the previous WRITE command. The first data-in element from the new burst is applied after either the last element of a completed burst or the last desired data element of the longer burst which is being truncated. The new WRITE command should be issued X cycles after the first WRITE command, where X equals the number of desired data-in element pairs (pairs are required by the 2n-prefetch architecture).



Consecutive WRITE-to-WRITE (BL=4)

Notes:

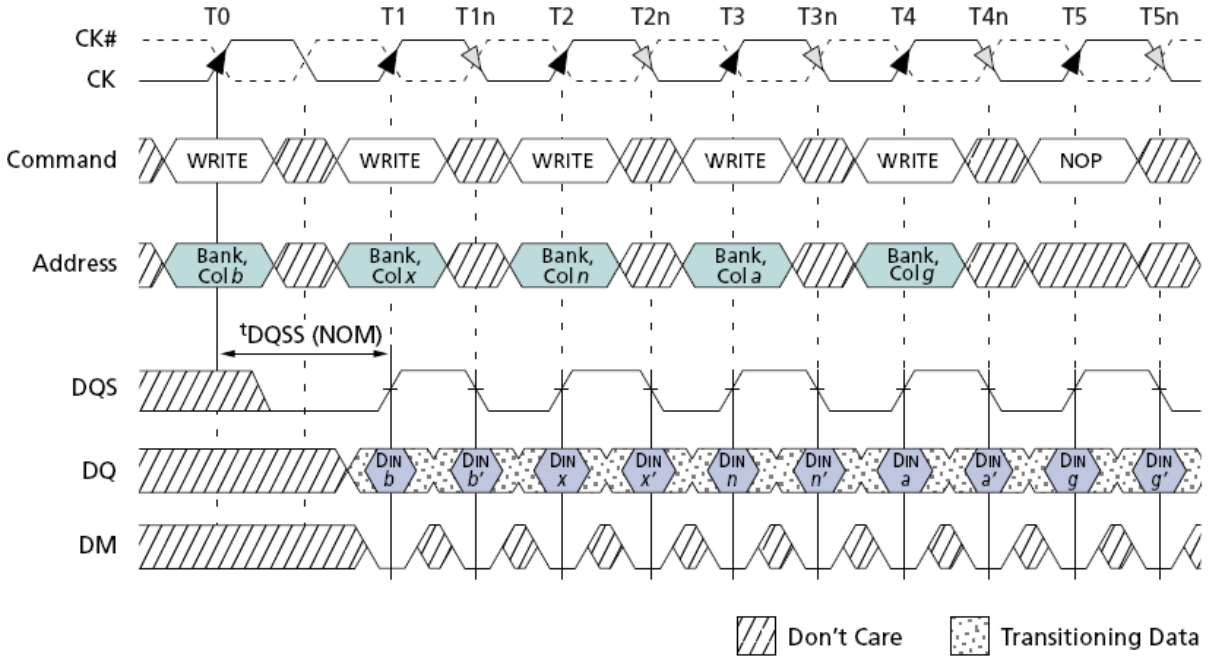
1. Din b (n) = data-in from column b (n).
2. An uninterrupted burst of 4 is shown.
3. Each WRITE command may be to any bank.



Nonconsecutive WRITE-to-WRITE (BL=4)

Notes:

1. Din b (n) = data-in from column b (n).
2. An uninterrupted burst of 4 is shown.
3. Each WRITE command may be to any bank.



Random Write Cycles

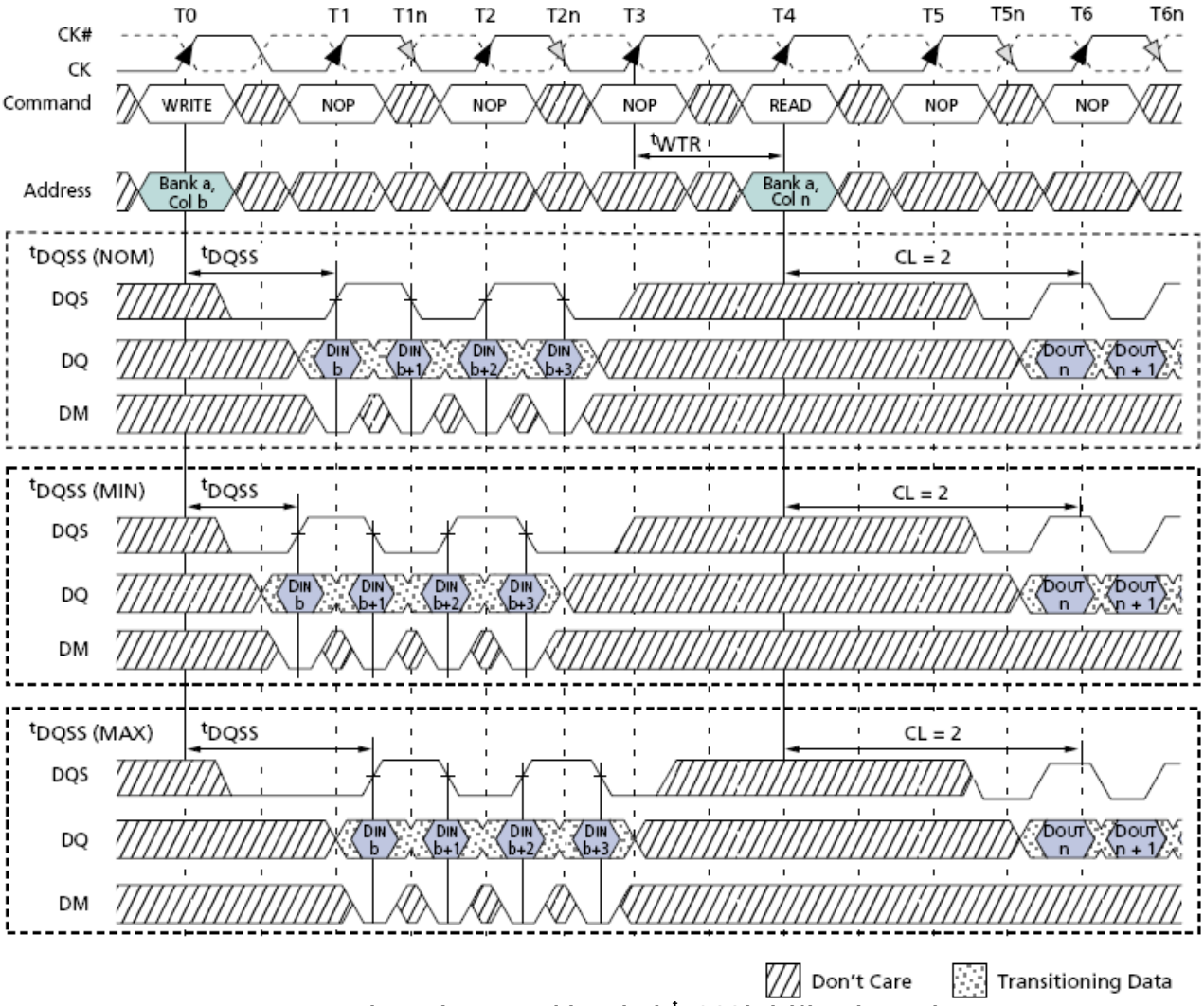
Notes:

1. Din b (or x, n, a, g) = data-in from column b (or x, n, a, g).
2. b' (or x', n', a', g') = the next data-in following Din b (x, n, a, g) according to the programmed burst order.

3. Programmed BL = 2, 4, 8, or 16 in cases shown.
4. Each WRITE command may be to any bank.

WRITE to READ

Data for any Write burst may be followed by a subsequent READ command. To follow a Write without truncating the write burst, ^{t}WTR should be met as shown in Figure.

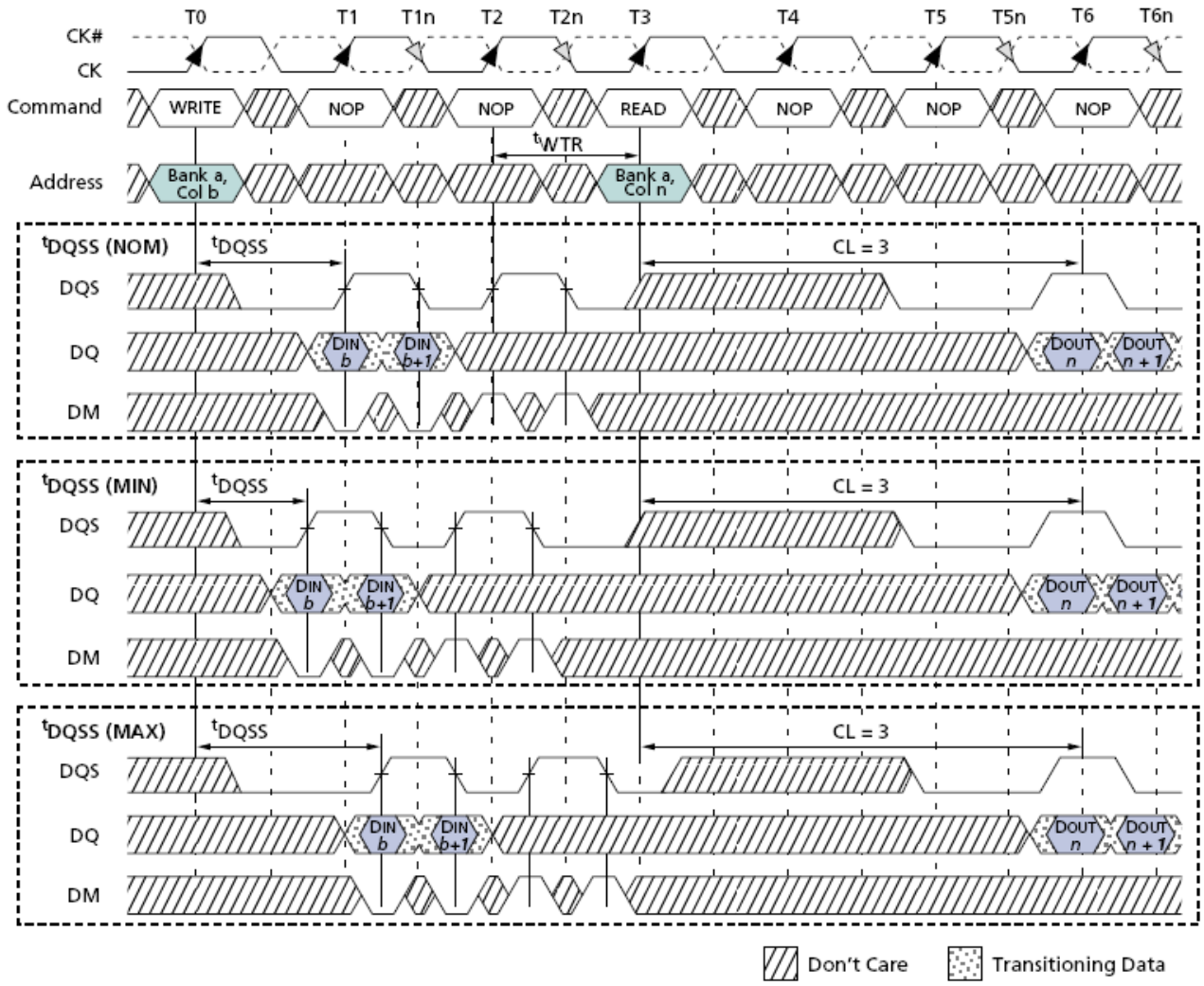


Non-Interrupting Write-to-Read (nominal, ^{t}DQSS(min)/(max), BL=4)

Notes:

1. Din b = data-in from column b; Dout n = data-out for column n.
2. An uninterrupted burst of 4 is shown.
3. ^{t}WTR is referenced from the first positive CK edge after the last data-in pair.
4. The READ and WRITE commands are to the same device. However, the READ and WRITE commands may be to different devices. In which case ^{t}WTR is not required and the READ command could be applied earlier.
5. A10 is LOW with the WRITE command (auto precharge is disabled).

Data for any Write burst may be truncated by a subsequent READ command as shown in Figure. Note that the only data-in pairs that are registered prior to the ^{t}WTR period are written to the internal array, and any subsequent data-in must be masked with DM.



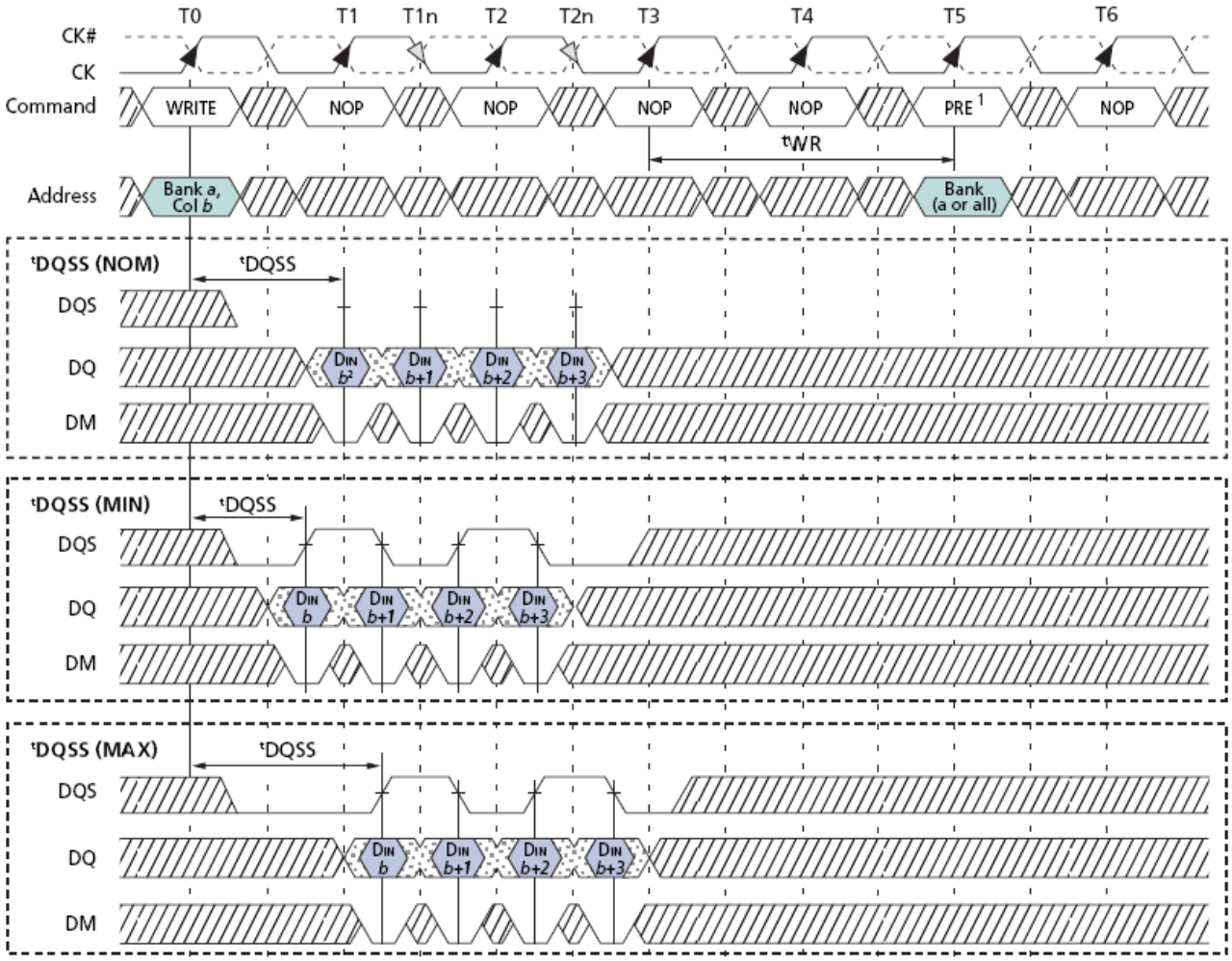
Interrupting Write-to-Read (nominal, ^{t}DQSS(min)/(max), BL=4)

Notes:

1. Din b = data-in from column b; Dout n = data-out for column n.
2. An uninterrupted burst of 4 is shown; two data elements are written.
3. ^{t}WTR is referenced from the first positive CK edge after the last data-in pair.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. DQS is required at T2 and T2n (nominal case) to register DM.

WRITE to PRECHARGE

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE without truncating the WRITE burst, tWR should be met as shown in the Figure.

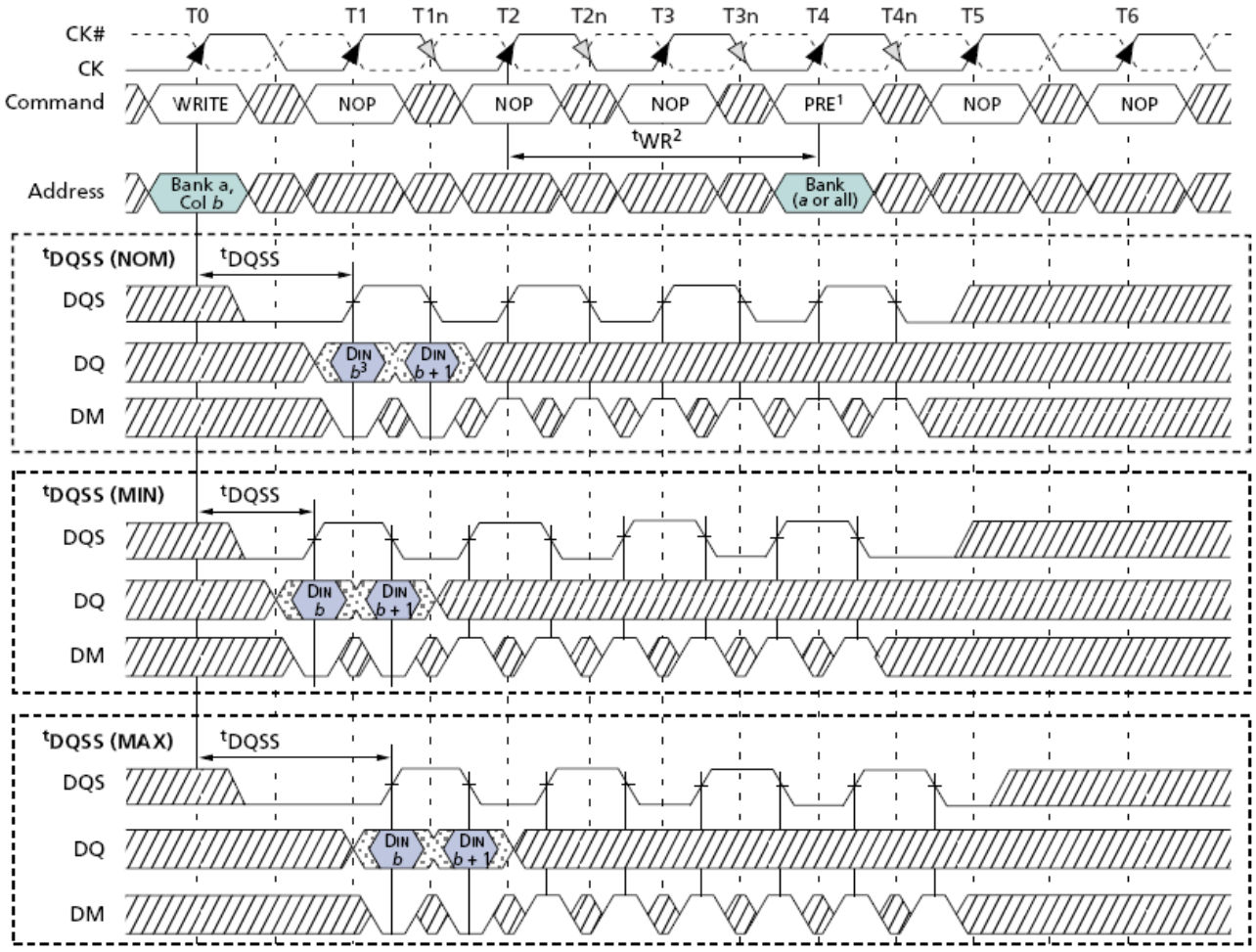


Non-Interrupting Write-to-Precharge (nominal, ^{t}DQSS(min)/(max), BL=4)

Notes:

1. PRE = PRECHARGE.
2. Din b = data-in from column b.
3. An uninterrupted burst of 4 is shown.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. ^{t}WTR is referenced from the first positive CK edge after the last data-in pair.
6. The PRECHARGE and WRITE commands are to the same device. However, the PRECHARGE and WRITE commands can be to different devices; in this case, ^{t}WR is not required and the PRECHARGE command can be applied earlier.

Data for any Write burst may be truncated by a subsequent PRECHARGE command as shown in Figure. Note that the only data-in pairs that are registered prior to the ^{t}WR period are written to the internal array, and any subsequent data-in must be masked with DM. After the PRECHARGE command, a subsequent command to the same bank can not be issued until ^{t}RP is met.



Interrupting Write-to-Precharge (nominal, ^{t}DQSS(min)/(max), BL=8)

Notes:

1. PRE = PRECHARGE.
2. ^{t}WR is referenced from the first positive CK edge after the last data-in pair.
3. Din b = data-in from column b.
4. An interrupted burst of 8 is shown; two data elements are written.
5. A10 is LOW with the WRITE command (auto precharge is disabled).
6. DQS is required at T4 and T4n to register DM.

PRECHARGE

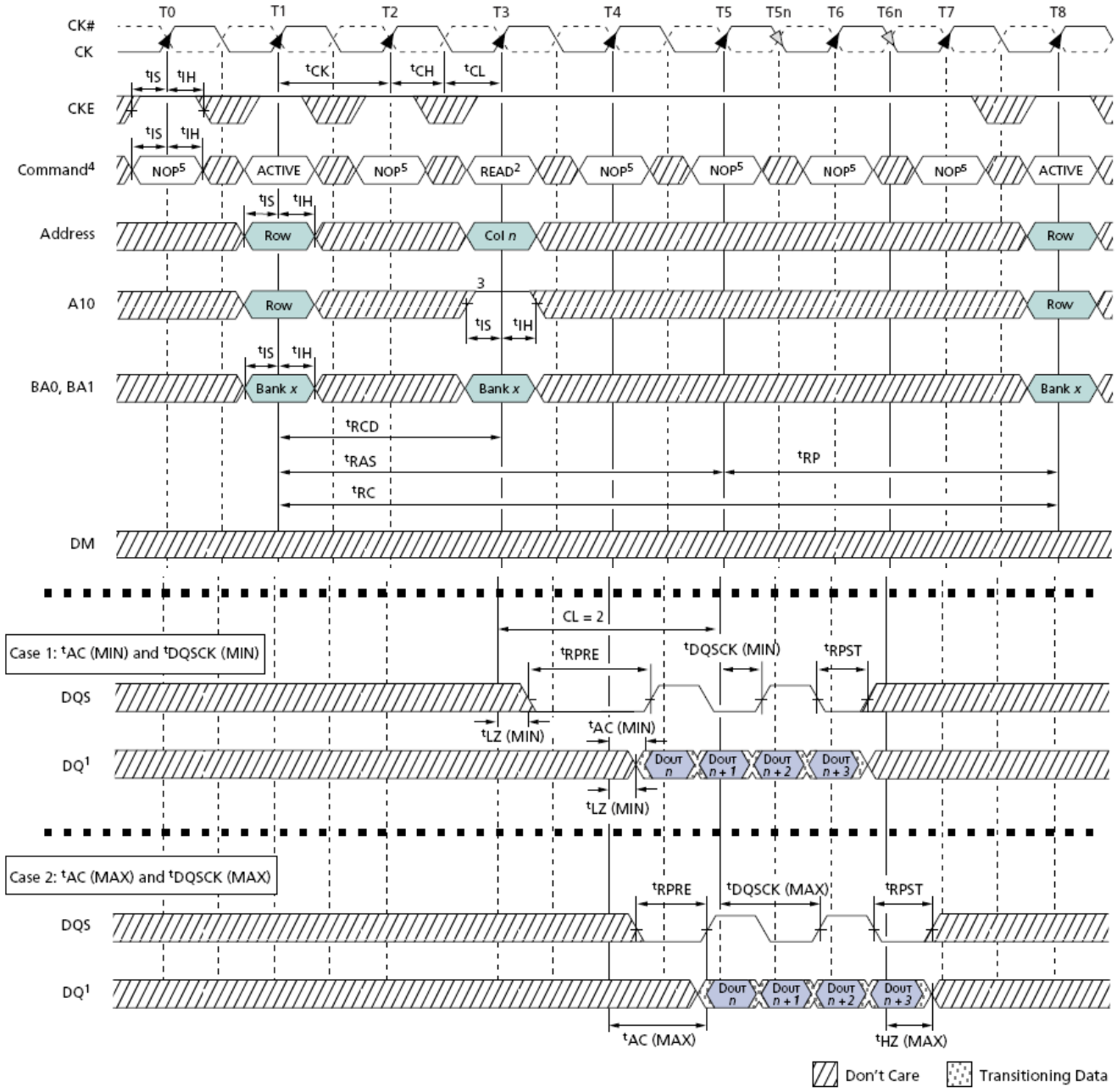
The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (^{t}RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged. In case where only one bank is to be precharged (A10=LOW), inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care”. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging.

AUTO PRECHARGE

Auto Precharge is a feature which performs the same individual bank precharge function described previously, but without requiring an explicit command. This is accomplished by using A10 (A10=High), to enable Auto Precharge in conjunction with a specific READ or WRITE command. A precharge of the bank / row that is addressed with the READ or WRITE command is automatically performed upon completion of the read or write burst. Auto precharge is non-persistent in that it is either enabled or disabled for each individual READ or WRITE command. Auto precharge ensures that a precharge is initiated at the earliest valid stage within a burst. The “earliest valid stage” is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating ^{t}RAS(min). The READ with auto precharge enabled or WRITE with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. The access period starts with registration of the command and ends where the precharge period (or ^{t}RP) begins. For READ with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all the data in the burst. For WRITE with auto precharge, the precharge period begins when ^{t}WR ends, with ^{t}WR measured as if auto precharge was disabled. In addition, during a WRITE with auto precharge, at least one clockis required during ^{t}WR time. During the prechare period, the user must not issue another command to the same bank until ^{t}RP is satisfied. This device supports ^{t}RAS lock-out. In the case of a single READ with auto-precharge or a single WRITE with auto-precharge issued at ^{t}RCD(min), the internal precharge will be delayed until ^{t}RAS(min) has been satisfied.

Concurrent AUTO PRECHARGE

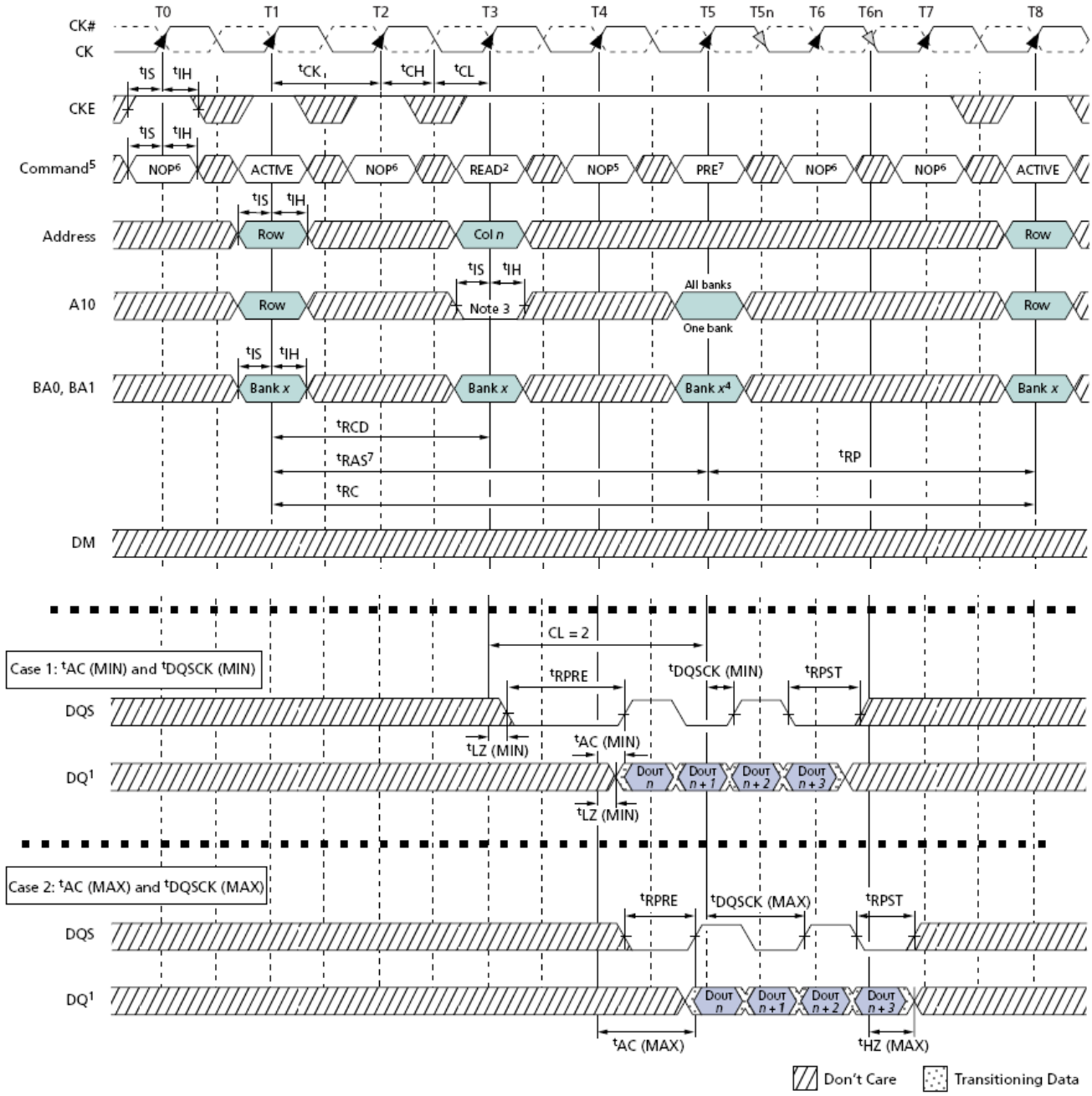
This device supports concurrent auto precharge such that when a READ with auto precharge is enabled or a WRITE with auto precharge is enabled, any command to another bank is supported, as long as that command does not interrupt the read or write data transfer already in process. This feature enables the precharge to complete in the bank in which the READ or WRITE with auto precharge was executed, without requiring an explicit PREACHRGE command, thus freeing the command bus for operations in other banks. During the access period of a READ or a WRITE with auto precharge, only ACTIVE and PRECHARGE commands may be applied to other banks. During the precharge period, ACTIVE, PRECHARGE, READ, and WRITE commands may be applied to other banks. In either situation, all other related limitations apply.



Bank Read with Auto precharge (^{t}AC, ^{t}DQSCK(min)/(max), BL=4)

Notes:

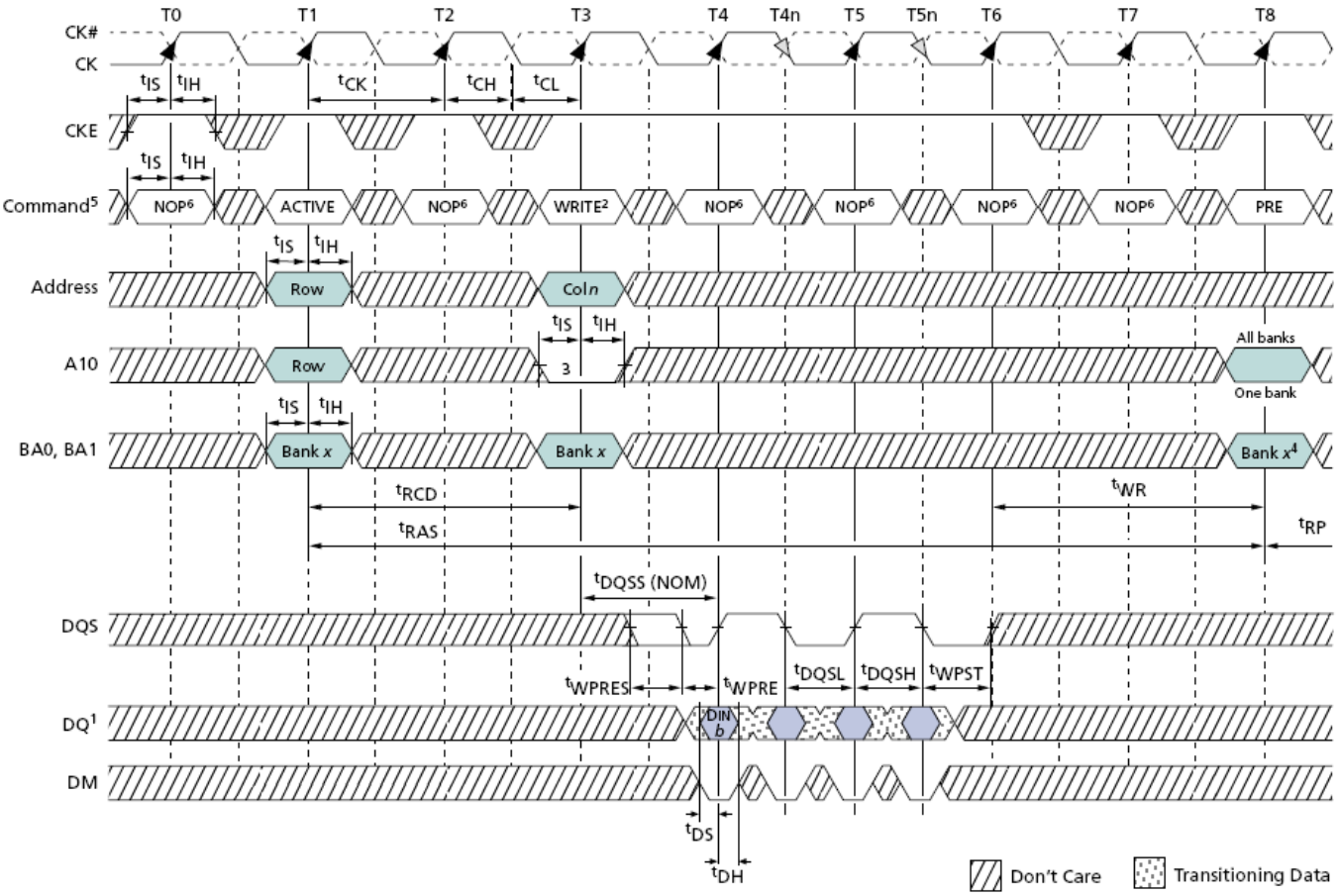
1. Din n = data-out from column n.
2. BL =4 in the case shown.
3. Enable auto precharge.
4. NOP commands are shown for ease of illustration; other commands may be valid at these times.



Bank Read without Auto precharge (^{t}AC, ^{t}DQSCK(min)/(max), BL=4)

Notes:

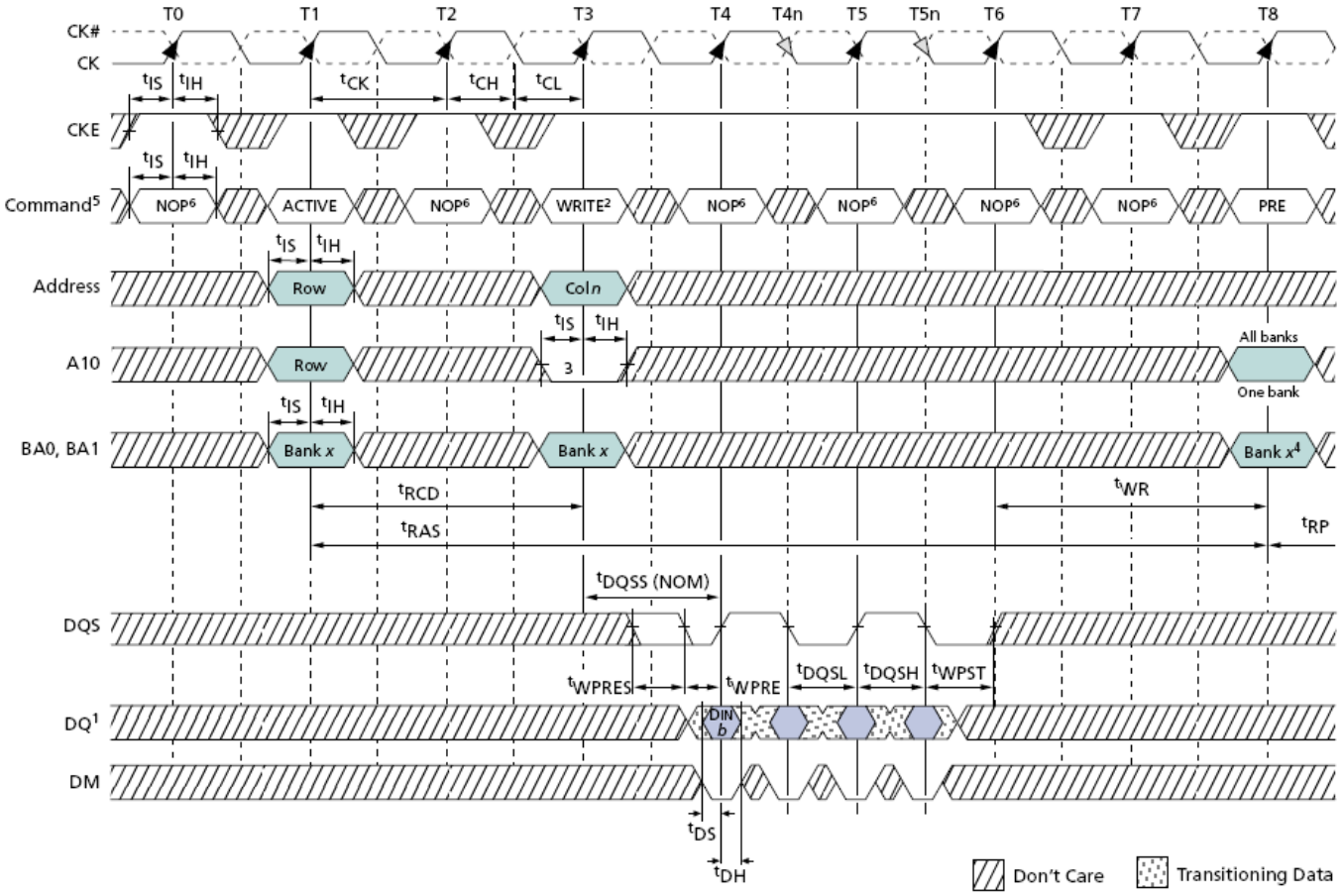
1. Din n = data-out from column n.
2. BL =4 in the case shown.
3. Disable auto precharge.
4. BANK x at T5 is "Don't Care", if A10 is HIGH at T5.
5. PRE = PRECHARGE.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. The PRECHARGE command can only be applied at T5, if ^{t}RAS(min) is met.



Bank Write with Auto precharge (BL=4)

Notes:

1. Din n = data-out from column n.
2. BL =4 in the case shown.
3. Enable auto precharge.
4. NOP commands are shown for ease of illustration; other commands may be valid at these times.



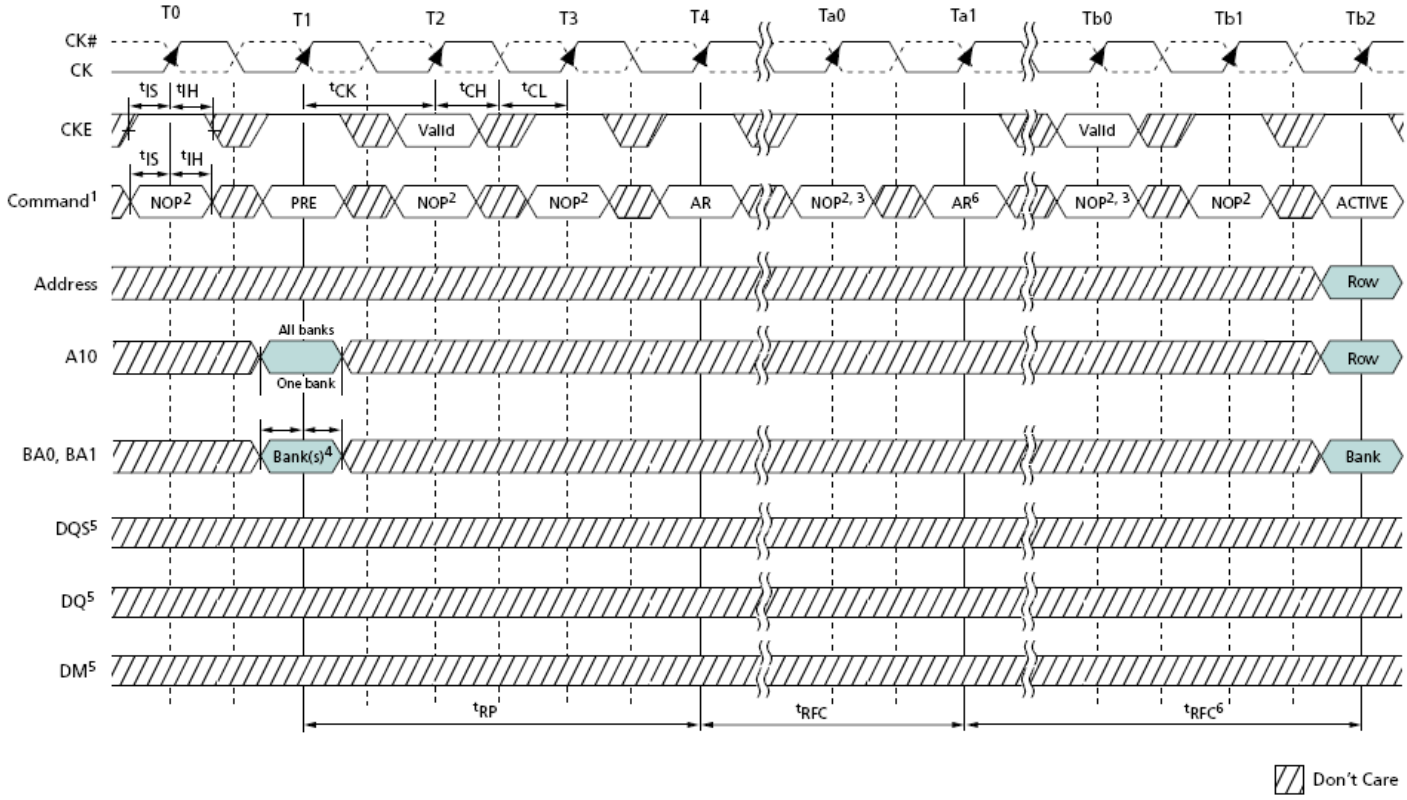
Bank Write without Auto precharge (BL=4)

Notes:

1. Din n = data-out from column n.
2. BL =4 in the case shown.
3. Disable auto precharge.
4. Bank x at T8 is "Don't Care", if A10 is HIGH at T8.
5. PRE = PRECHARGE.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.

AUTO REFRESH

AUTO REFRESH command is used during normal operation of the LPDDR SDRAM, and is analogous to /CAS-BEFORE-/RAS (CBR) Refresh in the FPM/EDO DRAMs. The Auto Refresh is non-persistent, so it must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller. The address bits become “Don’t Care” during AUTO REFRESH. The LPDDR SDRAM requires AUTO REFRESH commands at an average periodic interval of ^{t}REFI. To provide improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. Although it is not a JEDEC requirement, CKE must be active (HIGH) during the auto refresh period to provide support for future functional features. The auto refresh period begins when the AUTO REFRESH command is registered and ends ^{t}RFC later.



Notes:

1. PRE = PRECHARGE; AR = AUTO REFRESH.
2. NOP commands are shown for ease of illustration; other commands may be valid at these times. CKE must be active during clock positive transitions.
3. NOP or COMMAND INHIBIT are the only commands supported until after ^{t}RFC time; CKE must be active during clock positive transitions.
4. Bank x at T1 is “Don’t Care”, if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active.
5. DM, DQ, and DQS signals are all “Don’t Care”, High-Z for operations shown.
6. The second AUTO PRECHARGE is not required and is only shown as an example of two back-to-back AUTO REFRESH commands.

DIRECTED AUTO REFRESH (DARF)

Directed auto refresh (DARF) allows the memory controller to refresh one bank while accessing the other banks. DARF is enabled with bit[9] of the Extended Mode Register, EMR[9]:

EMR[9] = 0b: DARF operation is disabled.

EMR[9] = 1b: DARF command replaces AUTO REFRESH command.

W When EMR[9] toggles from 0 to 1 the internal bank register counter, DARF_BANK., will be reset to bank 0 so that the first DARF refresh will address bank 0. DARF should only be entered during device initialization. Once DARF is enabled, in order to switch back to normal operation, the user will be required to re-initialize the device and select normal device operation during the initialization sequence. Data in the array will not be guaranteed when switching from DARF to normal operation. DARF is similar to the AUTO REFRESH command with the exception that DARF only executes the refresh operation in a single bank. Table 25 identifies the command truth table for the available refresh commands.

DARF, Auto Refresh, and Self Refresh Commands

Name (Function)	/CS	/RAS	/CAS	/WE	CKE	EMR[9]	Address	Notes
AUTO REFRESH	L	L	L	H	H	0	X	
SELF REFRESH	L	L	L	H	L	X	X	
Directed Auto Refresh (DARF)	L	L	L	H	H	1	X	1

Notes:

1. Bank is specified by an internal register referred to as DARF_BANK. The bank for the DARF command is specified with a DARF_BANK register. During DARF the ADDR, BA are unspecified and do not impact the operation of the command.

DARF_BANK Register Control – Pointer for the DARF command identifies which bank is receiving the command. Note this register is not accessible outside the device.

Reset: DARF_BANK[1:0] 00b: Any of the following conditions cause a reset of the DARF_BANK Register:
Rising edge transition in EMR[9]: 0b 1b & Exit SELF REFRESH operation.

Increment: DARF_BANK[1:0] DARF_BANK[1:0] + 1: the counting order for the register is: 00b 01b 10b 11b 00b.... The counter is incremented by the execution of a DARF command. When the DARF command is active in one bank, other banks are available for the commands specified in Table 26. Receipt of commands not specified in the table is illegal and results in unpredictable operation.

Truth Table of Legal Commands During DARF

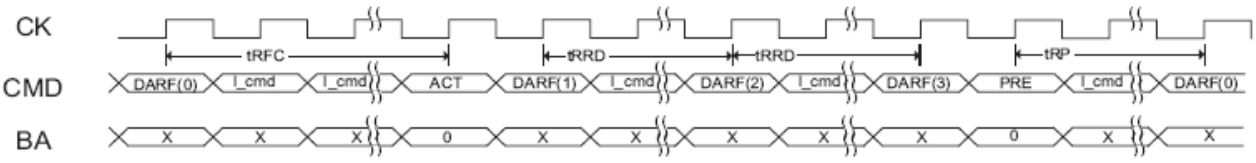
Name (Function)	/CS	/RAS	/CAS	/WE	Address	Notes
DESELECT (NOP)	H	X	X	X	X	2
NO OPERATION (NOP)	L	H	H	H	X	2
ACTIVE	L	L	H	H	BANK/ROW	1,2
READ	L	H	L	H	BANK/COL	1,2
WRITE	L	H	L	L	BANK/COL	1,2
BURST TERMINATE OR DEEP POWER DOWN	L	H	H	L	X	2
PRECHARGE	L	L	H	L	BANK	1,2
LOAD MODE REGISTER	L	L	L	L	Op-Code	2,3

Notes:

1. Only for the bank not executing the directed auto-refresh. Initiating a command to the bank with the active DARF operation is illegal and will corrupt either the DARF operation, the initiated command, or both.
2. Restrictions as specified in the device data sheet.
3. EMR[9] must remain '1b'

During DARF operation, ^{t}REF is reduced to 16ms. None of the other AC or DC specifications, including ^{t}RFC, ^{t}RRD, and ^{t}XSR, are affected by the DARF command.

DARF Commands Sequences



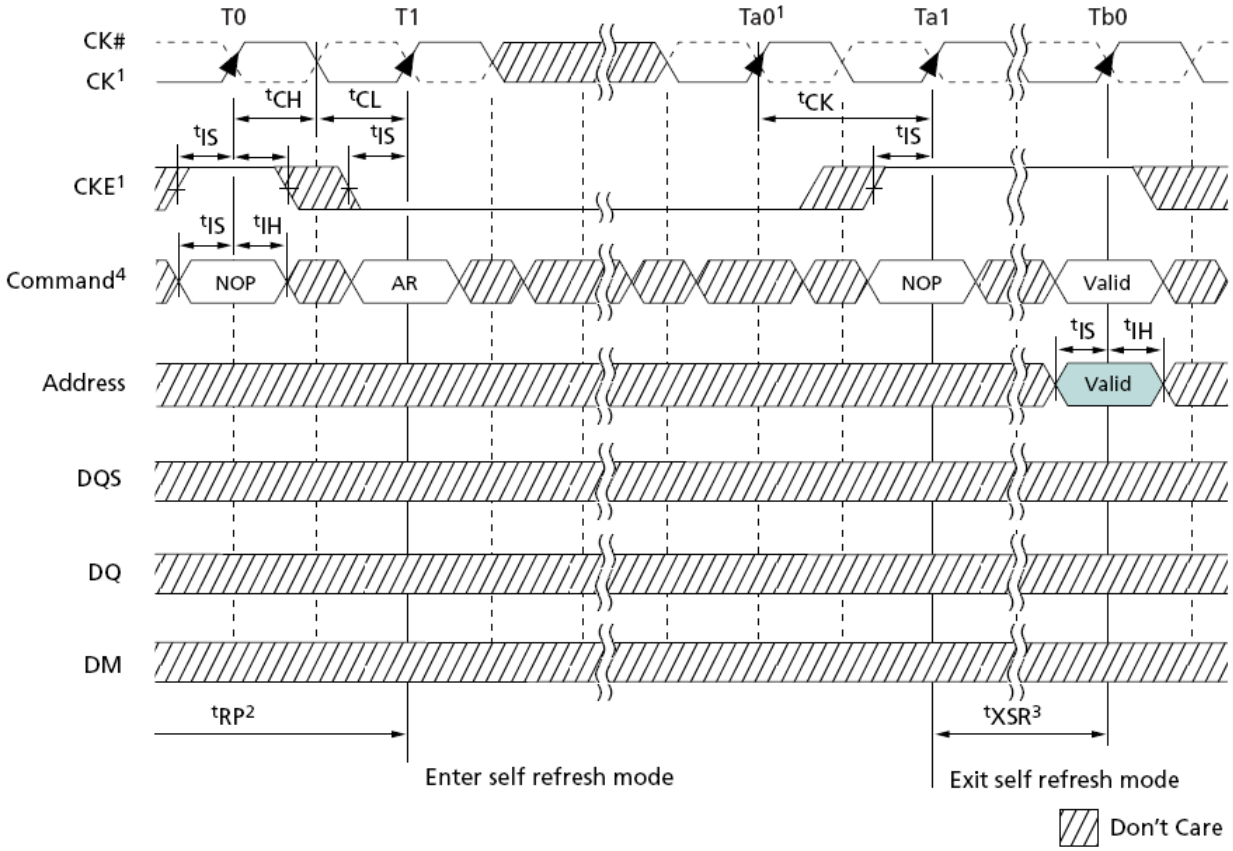
Notes: 1. DARF(n): "n" value in DARF_BANK register. Represents the bank being refreshed I_cmd: Any command.

SELF REFRESH

SELF REFRESH command can be used to retain data in the LPDDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the LPDDR SDRAM retains data without external clocking. The LPDDR SDRAM device has a built-in timer to accommodate Self Refresh operation. The SELF REFRESH command is initiated like an AUTO REFRESH command, except CKE is LOW. Input signals except CKE are "Don't Care" during Self Refresh. During SELF REFRESH, the device is refreshed as identified in the extended mode register. Once the SELF REFRESH command is registered, the external clock can be halted after one clock later. CKE must be held low to keep the device in Self Refresh mode, and internal clock also disabled to save power. The minimum time that the device must remain in Self Refresh mode is ^{t}RFC.

In the Self Refresh mode, two additional power-saving options exist: Temperature Compensated Self Refresh and Partial Array Self Refresh. During this mode, the device is refreshed as identified in the extended mode register. An internal temperature sensor will adjust the refresh rate to optimize device power consumption while ensuring data integrity. During SELF REFRESH operation, refresh intervals are scheduled internally and may vary. These refresh intervals may be different then the specified ^{t}REFI time. For this reason, the SELF REFRESH command must not be used as a substitute for the AUTO REFRESH command.

The procedure for exiting SELF REFRESH requires a sequence of commands. First, CK must be stable prior to CKE going back HIGH. When CKE is HIGH, the LPDDR SDRAM must have NOP commands issued for ^{t}XSR time to complete any internal refresh already in progress. Self Refresh is to be supported for full AT temperature range up to 105C. A temperature trip point should be provided to achieve 4x refresh rate above 85C.

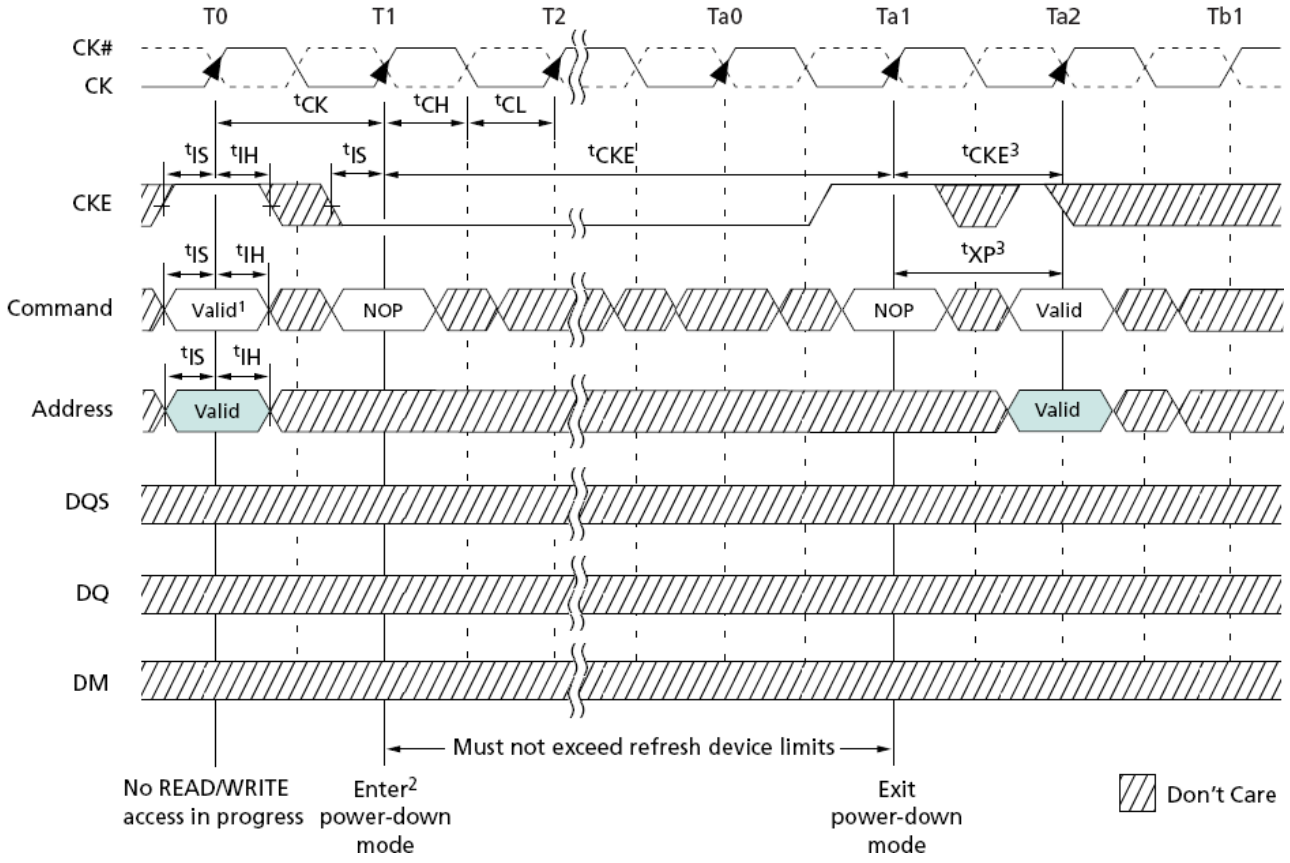


Notes:

1. Clock must be stable, cycling within specifications by Ta0, before exiting self refresh mode.
2. Device must be in the all banks idle state prior to entering self refresh mode.
3. NOPs or DESELECTs is required for ^{t}XSR time with at least two clock pulses.
4. AR = AUTO REFRESH.
5. CKE must remain LOW to remain in self refresh.

Power-Down

Power-down is entered when CKE is registered Low (no accesses can be in progress). If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Power-down mode deactivates all input and output buffers, excluding CK, /CK and CKE. CKE keep Low to maintain device in the power-down mode, and all other inputs signals are “Don’t Care”. The minimum power-down duration is specified by ^{t}CKE. The device can not stay in this mode for longer than the refresh requirements of the device, without losing data. The power-down state is synchronously existed when CKE is registered High (along with a NOP or DESELECT command). A valid command can be issued after ^{t}XP after exist from power-down.

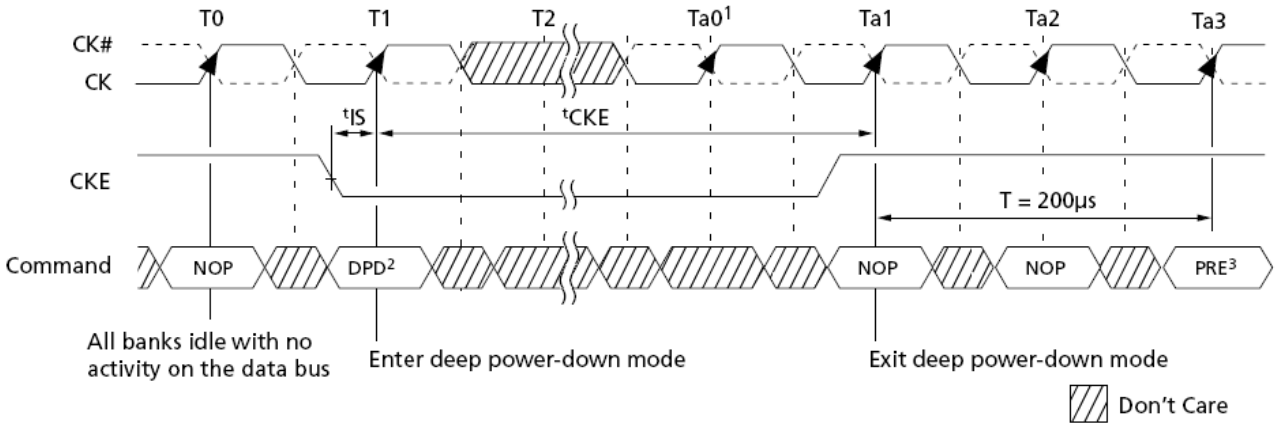


Notes:

1. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down. If this command is an ACTIVE (or if at least one row is already active), then the power-down mode is active power-down.
2. No column accesses can be in progress, when power-down is entered.
3. ^{t}CKE applies if CKE goes LOW at Ta2 (entering power-down); ^{t}XP applies if CKE remains HIGH at Ta2 (exit power-down).

Deep-Power-Down

The Deep Power-Down (DPD) mode is an operating mode used to achieve maximum power reduction by eliminating the power of the memory array. All internal voltage generators inside the LPDDR SDRAM are stopped and all memory data, MRS and EMRS information is lost in this mode. The DPD command is the same as a BURST TERMINATE command with CKE LOW. All banks must be in idle state with no activity on the data bus prior to entering the DPD mode. While in this mode, CKE must be held in a constant Low state. To exit the DPD mode, CKE is taken high after the clock is stable and NOP commands must be maintained for at least 200us. After 200us a complete re-initialization is required.



Notes:

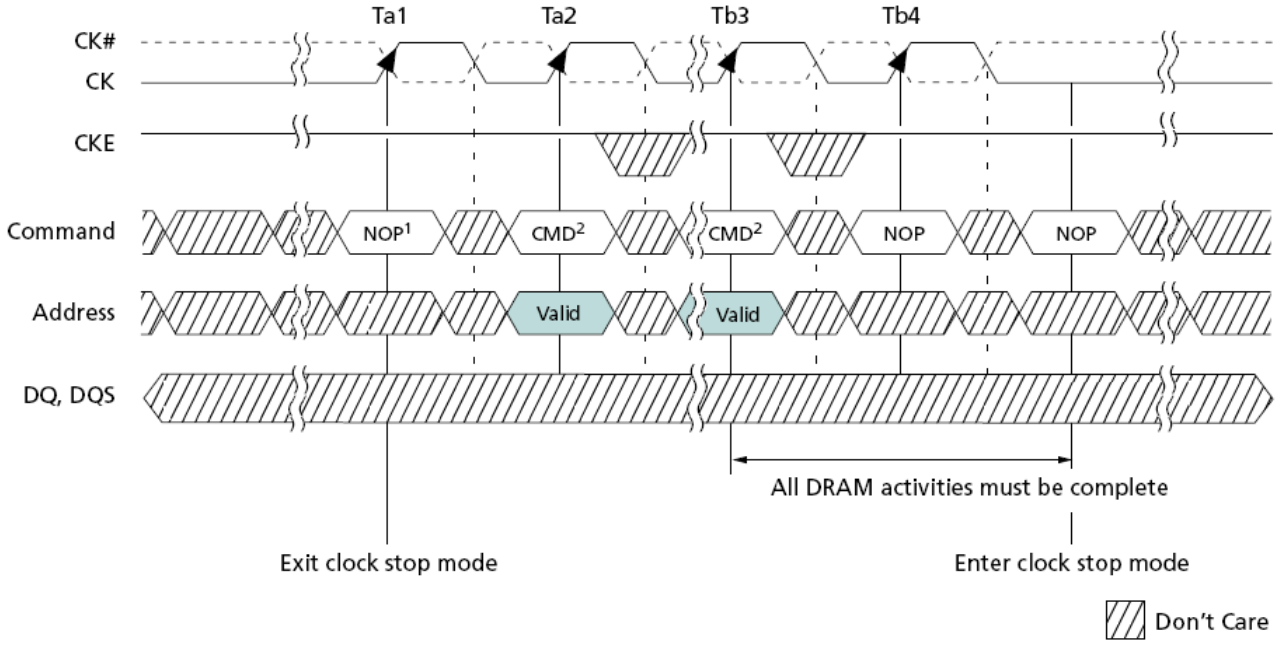
1. Clock must be stable prior to CKE going HIGH.
2. DPD = Deep Power-Down.
3. Upon exit of power-down mode, a full DRAM initialization sequence is required.

Clock Stop

One method of controlling the power efficiency in applications is to throttle the clock that controls the LPDDR SDRAM. The clock may be controlled in two ways:

- Change the clock frequency.
- Stop the clock.

The LPDDR SDRAM enables the clock to change frequency during operation only if all the timing parameters are met, and all refresh requirements are satisfied. The clock can be stopped altogether if there are no DRAM operations in progress that would be affected by this change. Any DRAM operation already in process must be completed before entering clock stop mode; this includes the following timings: ^{t}RCD, ^{t}RP, ^{t}RFC, ^{t}MRD, ^{t}WR, and ^{t}RPST. In addition, any READ or WRITE burst in progress must complete. CKE must be held HIGH, with CK=LOW and /CK=HIGH, for the full duration of the clock stop mode. One clock cycle and at least one NOP or DESELECT is required after the clock is restarted before a valid command can be issued.



Notes:

1. Prior to Ta1, the device is in clock stop mode. To exit, at least one NOP is required before any valid command.
2. Any valid command is supported; device is not in clock suspend mode.

Revision Log

Rev	Date	Modification
0.1	11/2009	Preliminary Release
0.2	10/2010	Update the AC/DC data base on real silicon characterization performance
0.9	07/2011	Errors correction
1.0	08/2011	For Web Release
1.1	10/2011	Error correction

NANYA TECHNOLOGY CORPORATION

HWA YA Technology Park

669, FU HSING 3rd Rd., Kueishan,

Taoyuan, Taiwan, R.O.C.

The NANYA TECHNOLOGY CORPORATION

Home page can be found at http:\\www.nanya.com