Feature

- Double-data rate architecture; two data transfer per clock cycle
- Bidirectional, data strobe (DQS, $\overline{DQS}$) is transmitted/received with data, to be used in capturing data at the receiver
- Differential clock inputs (CK and $\overline{CK}$)
- Differential data strobe (DQS and $\overline{DQS}$)
- Commands & addresses entered on both positive & negative CK edge; data and data mask referenced to both edges of DQS
- Eight internal banks for concurrent operation
- Data mask (DM) for write data
- Programmable Burst Lengths: 4 ,8 or 16
- Burst type: Sequential or interleave
- Programmable RL (Read latency) & WL (Write latency)
- Clock Stop capability during idle period
- Auto Pre-charge for each burst access
- Configurable Drive Strength (DS)
- Auto Refresh and Self Refresh Modes
- Optional Partial Array Self Refresh (PASR) and Temperature Compensated Self Refresh (TCSR)
- Deep Power Down Mode (DPD)
- HSUL_12 compatible inputs (High Speed Undermanaged Logic 1.2V)
- VDD2/VDDCA/VDDQ= 1.14~1.3V; VDD1= 1.70~1.95V
- Configuration and Addressing

Items		4Gb	8Gb
Device Type		S4	S4
Number of Banks		8	8
Bank Addresses		BA0-BA2	BA0-BA2
x32	Row	R0-R13	R0-R13
	Column	C0-C9	C0-C9

Options

VDD1/VDD2/VDDQ/VDDCA

- -1.8V/1.2V/1.2V/1.2V (S4B)

RoHS compliance and Halogen free

Package

- -134-Ball BGA 11.5mm x 11.5mm 0.65mm pitch
- -168-Ball PoP 12mm x 12mm 0.5mm pitch
- -216-Ball PoP 12mm x 12mm 0.4mm pitch
- -220-Ball PoP 14mm x 14mm 0.5mml pitch
- -240-Ball PoP 14mm x 14 mm 0.5mm pitch

Timing – cycle time

- -1.875ns @ RL=8(533MHz – DDR1066)
- -2.5ns @ RL=6 (400MHz – DDR800)
- -3.0ns @ RL=5 (333MHz – DDR667)

Operating temperature range

- -Commercial (-25℃ to +85℃)
- -Industrial (-40℃ to +85℃)

Description

LPDDR2-S4 uses the double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank/Row Buffer information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

To achieve high-speed operation, our LPDDR2-S4 SDRAM uses the double data rate architecture and adopt 4n-prefetch interface designed to transfer two data per clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single 4n-bit wide, one clock cycle data transfer at the internal SDRAM core and four corresponding n-bit wide, one-half-clock-cycle data transfer at the I/O pins. Read and write accesses to the LPDDR2-S4 are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

For LPDDR2-S4 devices, accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Active command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

Ordering Information

Density	Organization	Part Number	Package	Speed			
				^{t}CK (ns)	Clock (MHz)	Data Rate (Mb/s/pin)	RL
4Gb	128M x 32	NT6TL128M32AI-G0	134-Ball BGA 11.5mm x 11.5mm 0.65mm pitch	1.875	533	1066	8
		NT6TL128M32AI-G1		2.5	400	800	6
		NT6TL128M32AI-G2		3.0	333	667	5
		NT6TL128M32AQ-G0	168-Ball PoP 12mm x 12mm 0.5mm pitch	1.875	533	1066	8
		NT6TL128M32AQ-G1		2.5	400	800	6
		NT6TL128M32AQ-G2		3.0	333	667	5
8Gb	256M x 32	NT6TL256T32AQ-G0	168-Ball PoP 12mm x 12mm 0.5mm pitch	1.875	533	1066	8
		NT6TL256T32AQ-G1		2.5	400	800	6
		NT6TL256T32AQ-G2		3.0	333	667	5
8Gb	256M x 32	NT6TL256T32AS-G0	216-Ball PoP 12mm x 12mm 0.4mm pitch	1.875	533	1066	8
		NT6TL256T32AS-G1		2.5	400	800	6
8Gb	128M x 64	NT6TL128T64AR-G0	216-Ball PoP 12mm x 12mm 0.4mm pitch	1.875	533	1066	8
		NT6TL128T64AR-G1		2.5	400	800	6
		NT6TL128T64AR-G2		3.0	333	667	5
		NT6TL128T64A5-G0	220-Ball PoP 14mm x 14mm 0.5mml pitch	1.875	533	1066	8
		NT6TL128T64A5-G1		2.5	400	800	6
		NT6TL128T64A5-G2		3.0	333	667	5
8Gb	256M x 64	NT6TL256F64A3-G0	240-Ball PoP 14mm x 14 mm 0.5mm pitch	1.875	533	1066	8
Industrial							
8Gb	128M x 64	NT6TL128T64AR-G0I	216-Ball PoP 12mm x 12mm 0.4mm pitch	1.875	533	1066	8
		NT6TL128T64AR-G1I		2.5	400	800	6
		NT6TL128T64AR-G2I		3.0	333	667	5

NANYA Mobile Component/Wafer Part Numbering Guide

NT 6T L 128M32 A I — G1

NANYA
Technology

Product Family

6S =LPSDR SDRAM

6D =LPDDR SDRAM

6V =LPDDR2-S2 SDRAM

6T = LPDDR2-S4 SDRAM

6X = LPSDR/DDR comb

6Y = LPDDR2-S2/S4 comb

Interface & Power (V_{DD} & V_{DDQ})

M = LVCMOS (1.8V, 1.8V)

N = LVCMOS (1.8V, 1.2V)

Interface & Power (V_{DD1} , V_{DD2} , V_{DDQ} , V_{DDCA})

L = HSUL_12 (1.8V, 1.2V, 1.2V, 1.2V)

H = HSUL_12 (1.8V, 1.35V, 1.2V, 1.2V)

Organization (Depth, Width): M=Mono; T=DDP[1] ; F=QDP[2]

256Mb = 16M16 = 8M32 = 8M32R[3]

512Mb = 32M16 = 16M32 = 16M32R

1Gb = 64M16 = 32M32 = 32M32R

2Gb = 256M8 = 128M16 = 64M32 = 64M32R

4Gb = 256M16 = 128M32 = 64T64

8Gb = 128F64 = 256F32 = 128T64 = 256T32

Device Version

A = 1st version

B = 2nd version

C = 3rd version

Package Code

G = 54-Ball BGA (LPSDR, x16)

D = 60-Ball BGA (LPDDR, x16)

K = 90-Ball BGA (LPSDR, x32)

C = 90-Ball BGA (LPDDR, x32)

A = 79-Ball BGA (LPDDR2, x16)

I = 134-Ball BGA (LPDDR2, x32)

Q = 168-Ball PoP-VFBGA (LPDDR2)

R = 216-Ball PoP-VFBGA (LPDDR2)

3 = 240-Ball PoP-VFBGA (LPDDR2)

5= 220-Ball PoP-VFBGA (LPDDR2)

0 = Wafer (KGD)

Speed

LPSDR

S1 = 166MHz @ CL=3

S2 = 133MHz @ CL=3

LPDDR

T1 = 5.0ns @ CL=3

T2 = 5.4ns @ CL=3

T3 = 6.0ns @ CL=3

T4 = 7.5ns @ CL=3

T5 = T3 & S2

T6 = T1 & S1

LPDDR2-S2

T1 = 5.0ns @ RL=3

T3 = 6.0ns @ RL=3

LPDDR2-S4

G0 = 1.875ns @ RL=8

G1 = 2.5ns @ RL=6

G2 = 3.0ns @ RL=5

G3 = 3.7ns @ RL=4

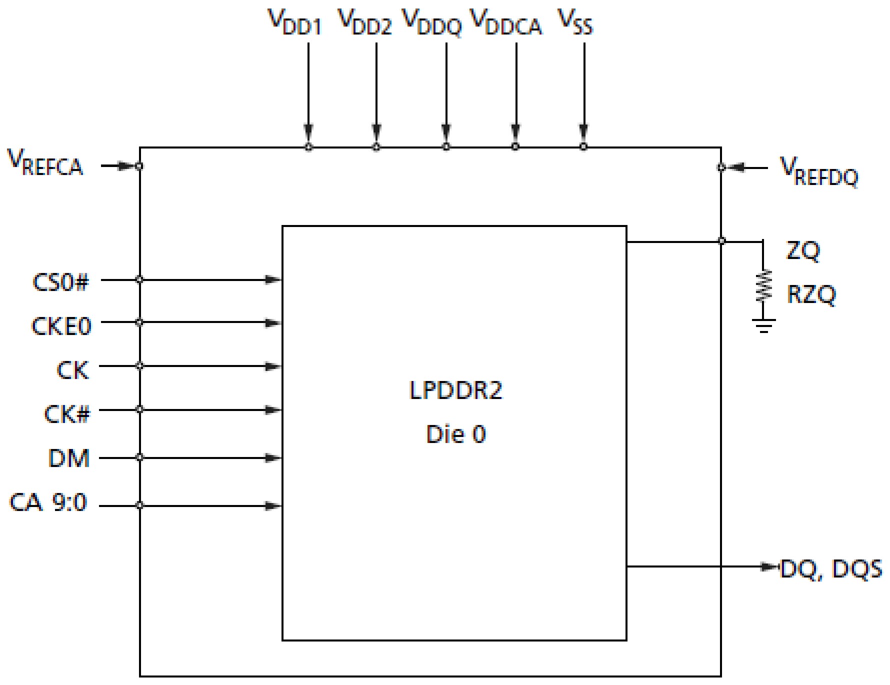
G4 = 5.0ns @ RL=3

Grade

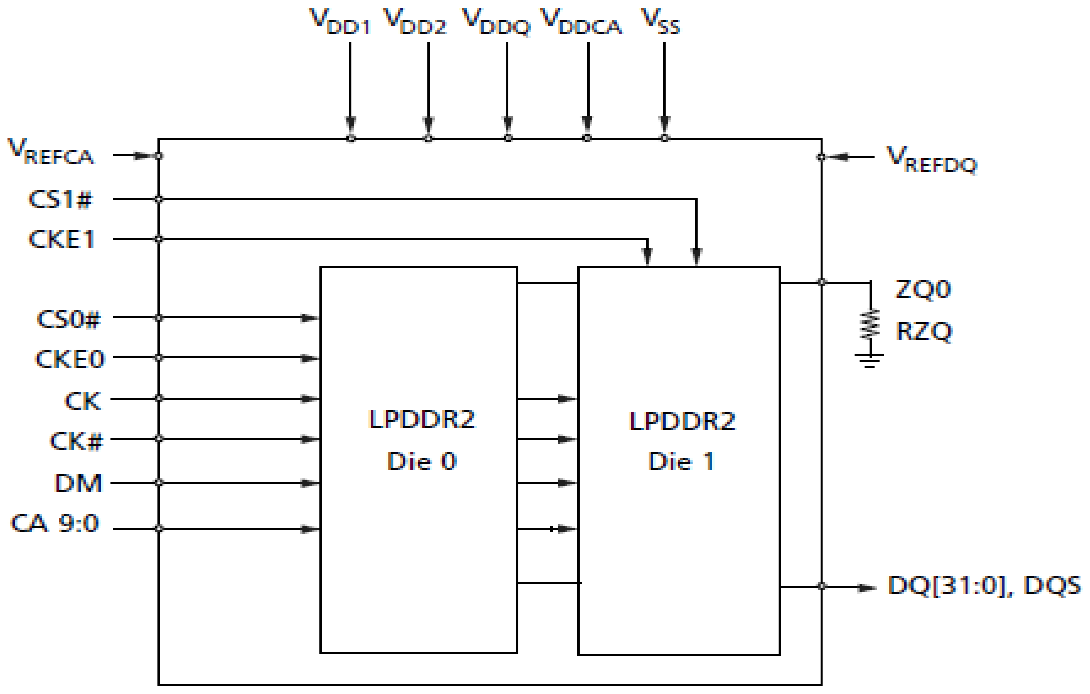
I =Industrial Grade

N/A =Commercial Grade

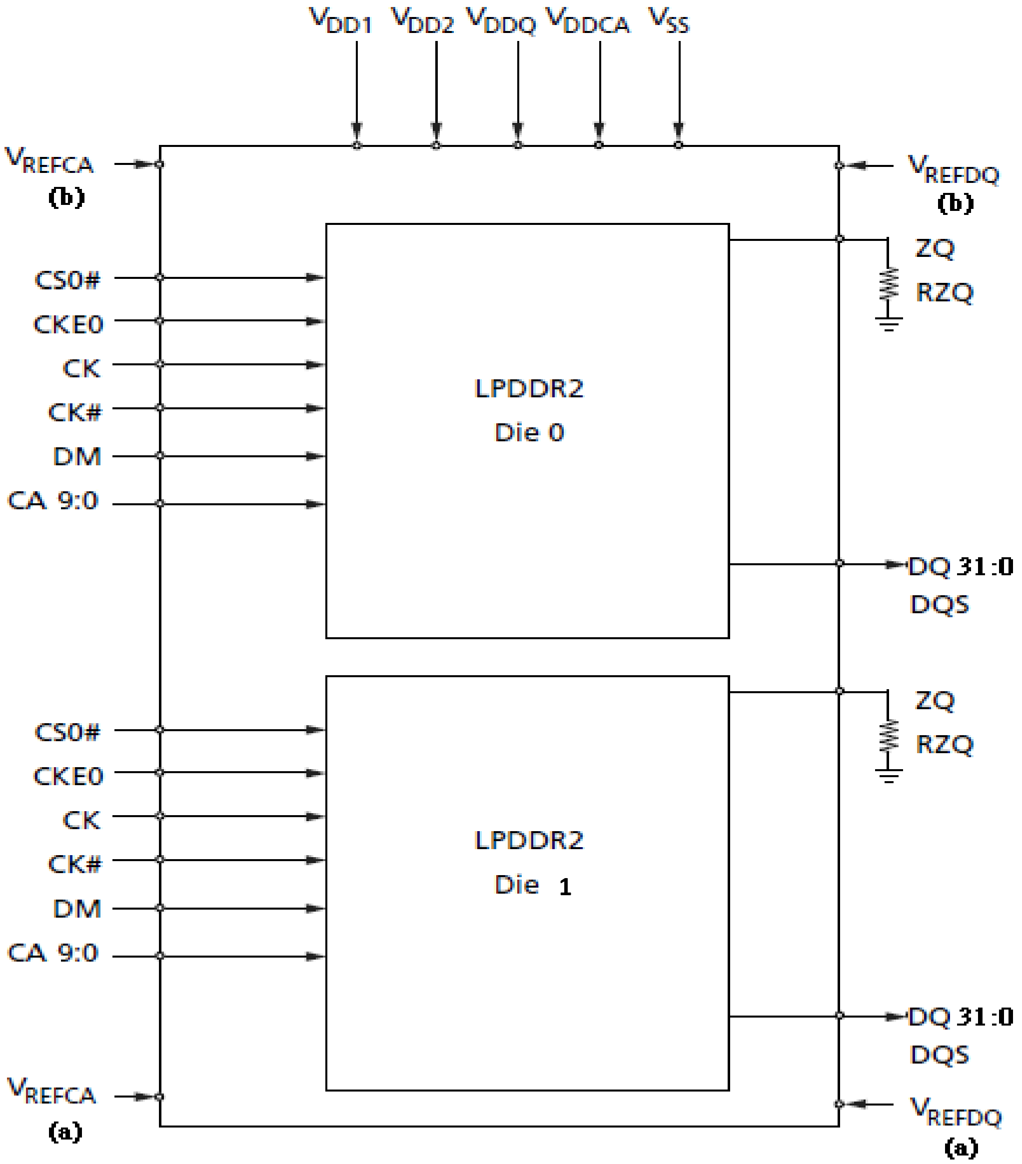
Block Diagram – Single Die, Single Channel Package



Block Diagram — Dual Die, Single Channel Package



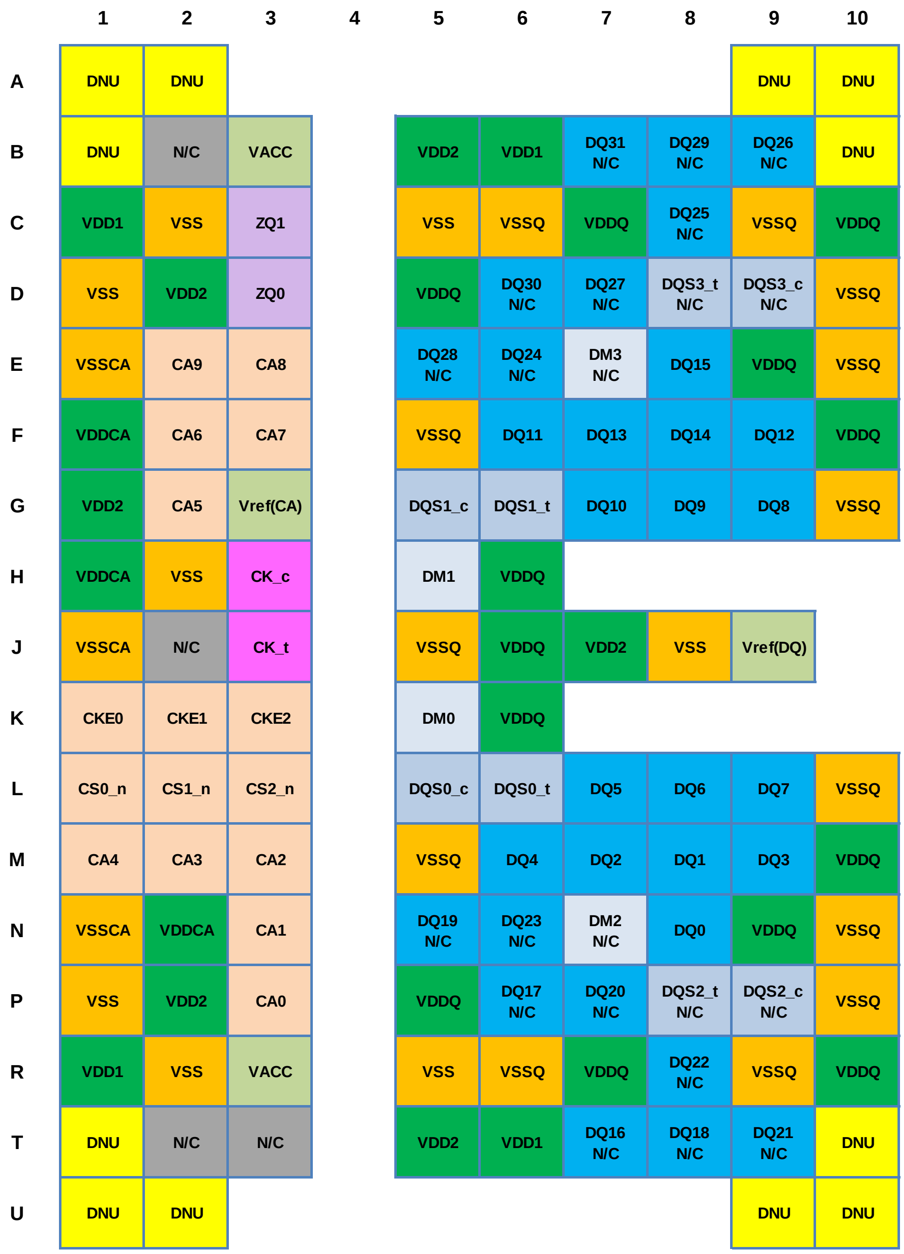
Block Diagram – Dual Die, Dual Channel Package



Pin Configuration – 134 balls BGA-VFBGA Package

< TOP View>

See the balls through the package



	1	2	3	4	5	6	7	8	9	10
A	DNU	DNU							DNU	DNU
B	DNU	N/C	VACC		VDD2	VDD1	DQ31 N/C	DQ29 N/C	DQ26 N/C	DNU
C	VDD1	VSS	ZQ1		VSS	VSSQ	VDDQ	DQ25 N/C	VSSQ	VDDQ
D	VSS	VDD2	ZQ0		VDDQ	DQ30 N/C	DQ27 N/C	DQS3_t N/C	DQS3_c N/C	VSSQ
E	VSSCA	CA9	CA8		DQ28 N/C	DQ24 N/C	DM3 N/C	DQ15	VDDQ	VSSQ
F	VDDCA	CA6	CA7		VSSQ	DQ11	DQ13	DQ14	DQ12	VDDQ
G	VDD2	CA5	Vref(CA)		DQS1_c	DQS1_t	DQ10	DQ9	DQ8	VSSQ
H	VDDCA	VSS	CK_c		DM1	VDDQ				
J	VSSCA	N/C	CK_t		VSSQ	VDDQ	VDD2	VSS	Vref(DQ)	
K	CKE0	CKE1	CKE2		DM0	VDDQ				
L	CS0_n	CS1_n	CS2_n		DQS0_c	DQS0_t	DQ5	DQ6	DQ7	VSSQ
M	CA4	CA3	CA2		VSSQ	DQ4	DQ2	DQ1	DQ3	VDDQ
N	VSSCA	VDDCA	CA1		DQ19 N/C	DQ23 N/C	DM2 N/C	DQ0	VDDQ	VSSQ
P	VSS	VDD2	CA0		VDDQ	DQ17 N/C	DQ20 N/C	DQS2_t N/C	DQS2_c N/C	VSSQ
R	VDD1	VSS	VACC		VSS	VSSQ	VDDQ	DQ22 N/C	VSSQ	VDDQ
T	DNU	N/C	N/C		VDD2	VDD1	DQ16 N/C	DQ18 N/C	DQ21 N/C	DNU
U	DNU	DNU							DNU	DNU

Note: 1. 11.5x11.5 mm, 0.65mm pitch

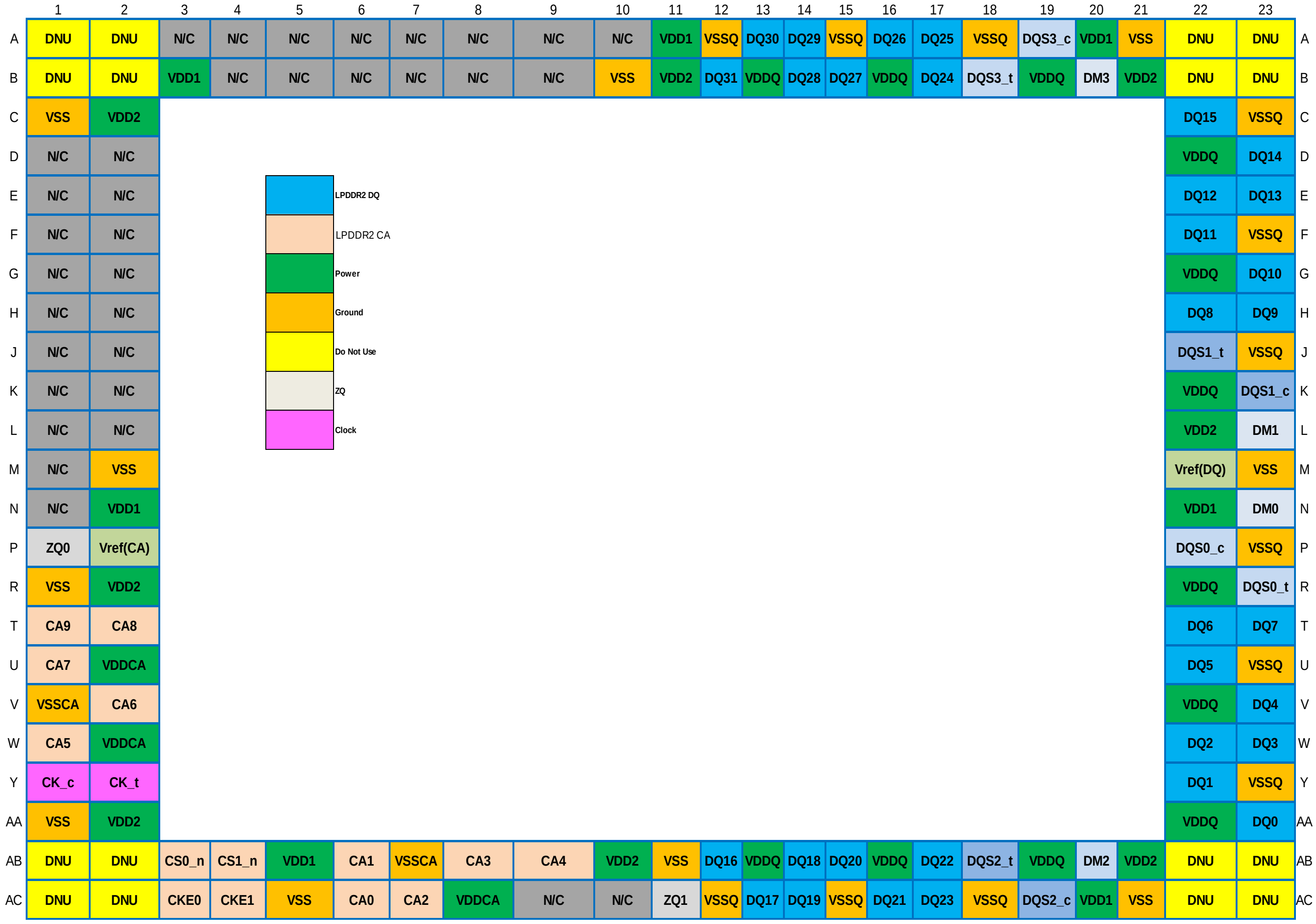
2. 134 Ball Count

3. Top View, A1 in Top Left Corner

Pin Configuration – 168 balls PoP-VFBGA Package

< TOP View>

See the balls through the package



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	DNU	DNU	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	VDD1	VSSQ	DQ30	DQ29	VSSQ	DQ26	DQ25	VSSQ	DQS3_c	VDD1	VSS	DNU	DNU	A
B	DNU	DNU	VDD1	N/C	N/C	N/C	N/C	N/C	N/C	VSS	VDD2	DQ31	VDDQ	DQ28	DQ27	VDDQ	DQ24	DQS3_t	VDDQ	DM3	VDD2	DNU	DNU	B
C	VSS	VDD2																				DQ15	VSSQ	C
D	N/C	N/C																				VDDQ	DQ14	D
E	N/C	N/C																				DQ12	DQ13	E
F	N/C	N/C																				DQ11	VSSQ	F
G	N/C	N/C																				VDDQ	DQ10	G
H	N/C	N/C																				DQ8	DQ9	H
J	N/C	N/C																				DQS1_t	VSSQ	J
K	N/C	N/C																				VDDQ	DQS1_c	K
L	N/C	N/C																				VDD2	DM1	L
M	N/C	VSS																				Vref(DQ)	VSS	M
N	N/C	VDD1																				VDD1	DM0	N
P	ZQ0	Vref(CA)																				DQS0_c	VSSQ	P
R	VSS	VDD2																				VDDQ	DQS0_t	R
T	CA9	CA8																				DQ6	DQ7	T
U	CA7	VDDCA																				DQ5	VSSQ	U
V	VSSCA	CA6																				VDDQ	DQ4	V
W	CA5	VDDCA																				DQ2	DQ3	W
Y	CK_c	CK_t																				DQ1	VSSQ	Y
AA	VSS	VDD2																				VDDQ	DQ0	AA
AB	DNU	DNU	CS0_n	CS1_n	VDD1	CA1	VSSCA	CA3	CA4	VDD2	VSS	DQ16	VDDQ	DQ18	DQ20	VDDQ	DQ22	DQS2_t	VDDQ	DM2	VDD2	DNU	DNU	AB
AC	DNU	DNU	CKE0	CKE1	VSS	CA0	CA2	VDDCA	N/C	N/C	ZQ1	VSSQ	DQ17	DQ19	VSSQ	DQ21	DQ23	VSSQ	DQS2_c	VDD1	VSS	DNU	DNU	AC

LPDDR2 DQ
LPDDR2 CA
Power
Ground
Do Not Use
ZQ
Clock

Note: 1. 12x12 mm, 0.5mm pitch

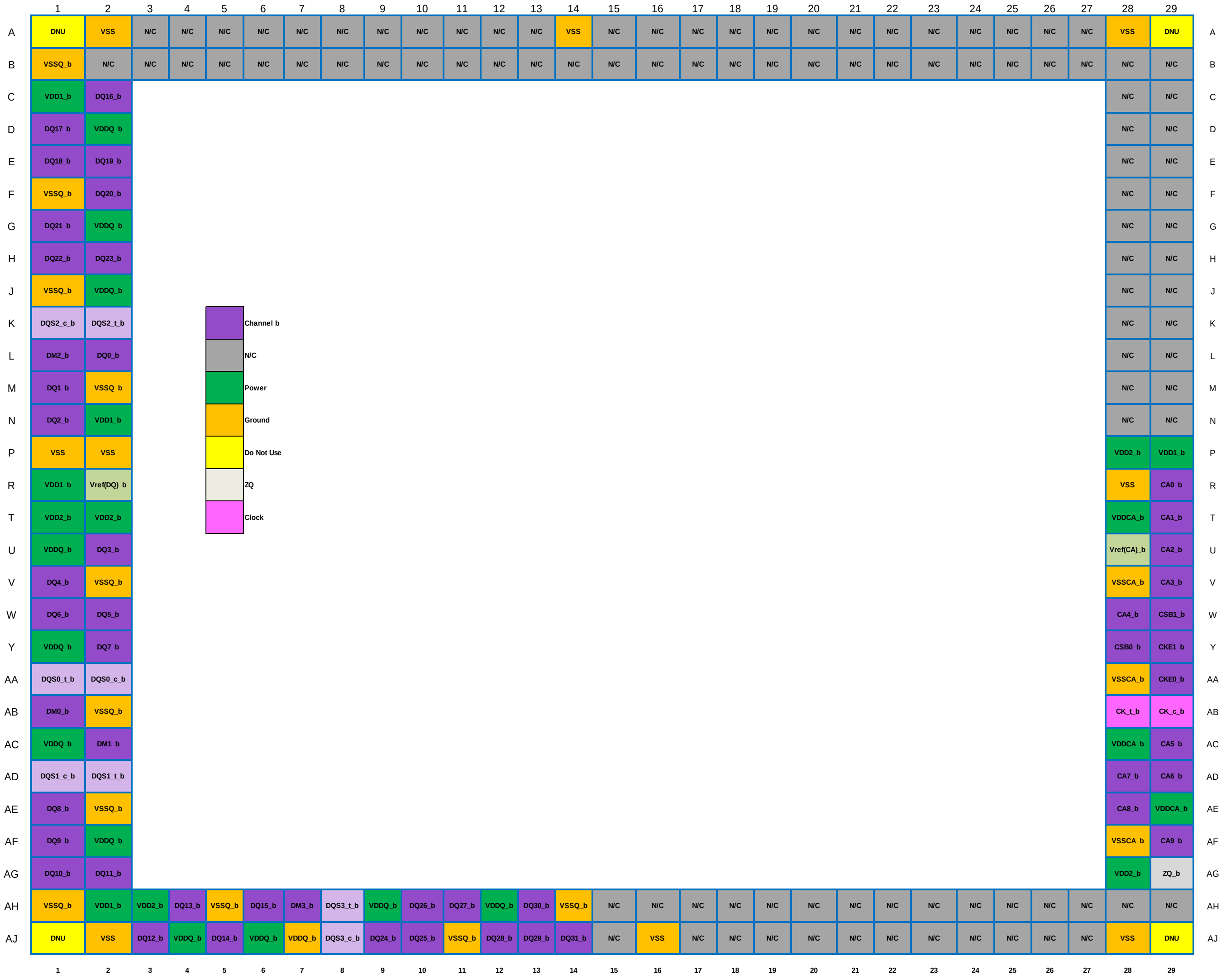
2. 168 Ball Count

3. Top View, A1 in Top Left Corner

Pin Configuration – 216 balls PoP-VFBGA Package (Channel B)

< TOP View>

See the balls through the package



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
A	DNU	VSS	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	VSS	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	VSS	DNU	A
B	VSSQ_b	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	B
C	VDD1_b	DQ16_b																										N/C	N/C	C
D	DQ17_b	VDDQ_b																										N/C	N/C	D
E	DQ18_b	DQ19_b																										N/C	N/C	E
F	VSSQ_b	DQ20_b																										N/C	N/C	F
G	DQ21_b	VDDQ_b																										N/C	N/C	G
H	DQ22_b	DQ23_b																										N/C	N/C	H
J	VSSQ_b	VDDQ_b																										N/C	N/C	J
K	DQS2_c_b	DQS2_t_b																										N/C	N/C	K
L	DM2_b	DQ0_b																										N/C	N/C	L
M	DQ1_b	VSSQ_b																										N/C	N/C	M
N	DQ2_b	VDD1_b																										N/C	N/C	N
P	VSS	VSS																										VDD2_b	VDD1_b	P
R	VDD1_b	Vref(DQ)_b																										VSS	CA0_b	R
T	VDD2_b	VDD2_b																										VDDCA_b	CA1_b	T
U	VDDQ_b	DQ3_b																										Vref(CA)_b	CA2_b	U
V	DQ4_b	VSSQ_b																										VSSCA_b	CA3_b	V
W	DQ6_b	DQ5_b																										CA4_b	CSB1_b	W
Y	VDDQ_b	DQ7_b																										CSB0_b	CKE1_b	Y
AA	DQS0_t_b	DQS0_c_b																										VSSCA_b	CKE0_b	AA
AB	DM0_b	VSSQ_b																										CK_t_b	CK_c_b	AB
AC	VDDQ_b	DM1_b																										VDDCA_b	CA5_b	AC
AD	DQS1_c_b	DQS1_t_b																										CA7_b	CA6_b	AD
AE	DQ8_b	VSSQ_b																										CA8_b	VDDCA_b	AE
AF	DQ9_b	VDDQ_b																										VSSCA_b	CA9_b	AF
AG	DQ10_b	DQ11_b																										VDD2_b	ZQ_b	AG
AH	VSSQ_b	VDD1_b	VDD2_b	DQ13_b	VSSQ_b	DQ15_b	DM3_b	DQS3_t_b	VDDQ_b	DQ26_b	DQ27_b	VDDQ_b	DQ30_b	VSSQ_b	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	AH
AJ	DNU	VSS	DQ12_b	VDDQ_b	DQ14_b	VDDQ_b	VDDQ_b	DQS3_c_b	DQ24_b	DQ25_b	VSSQ_b	DQ28_b	DQ29_b	DQ31_b	N/C	VSS	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	VSS	DNU	AJ
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

- 🟪 Channel b
- ⬜ N/C
- 🟩 Power
- 🟧 Ground
- 🟨 Do Not Use
- ⬜ ZQ
- 🟪 Clock

Note: 1. 12x12 mm, 0.4mm pitch

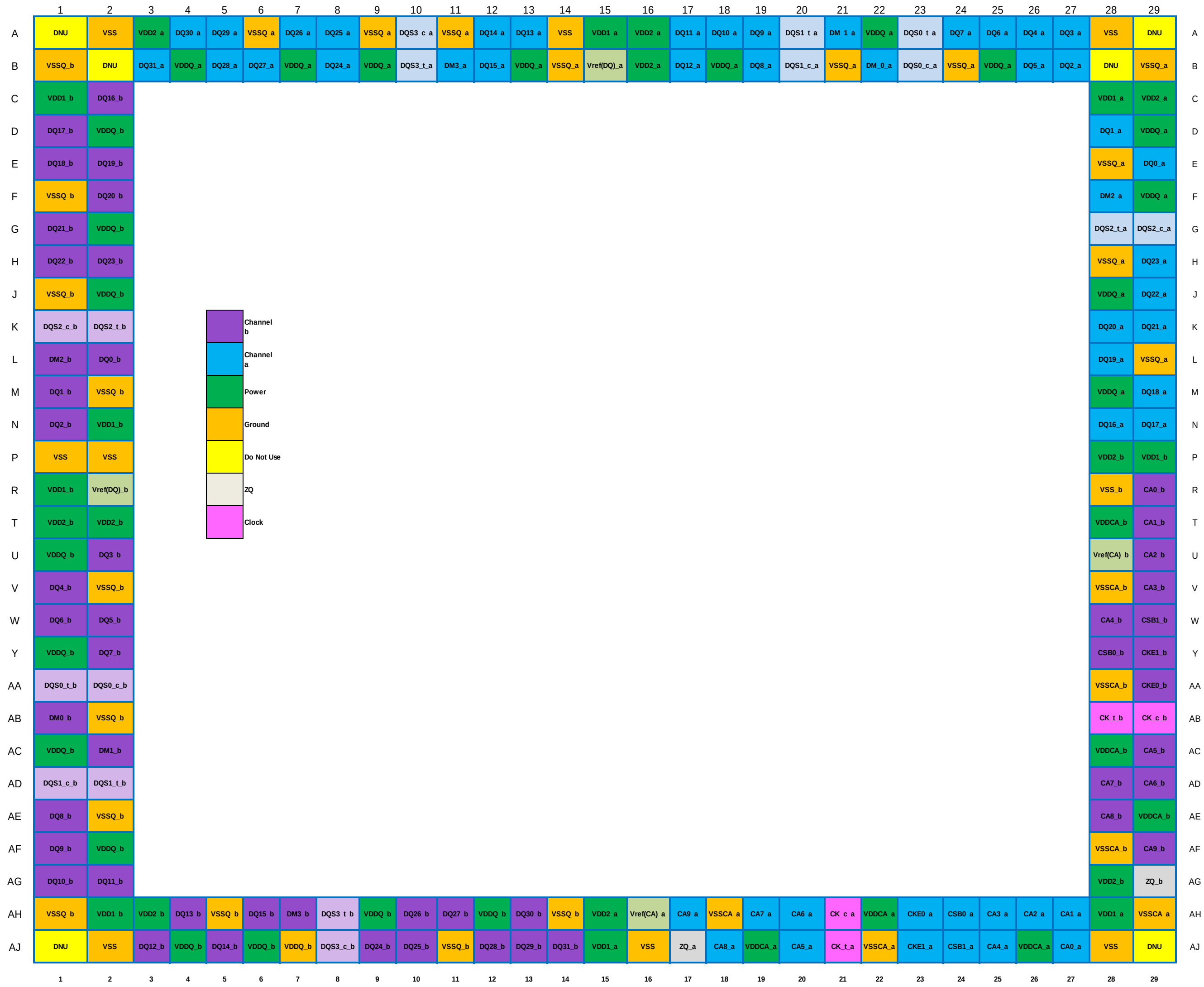
2. 216 Ball Count

3. Top View, A1 in Top Left Corner

Pin Configuration – 216 balls PoP-VFBGA Package (Dual Channel)

< TOP View>

See the balls through the package



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
A	DNU	VSS	VDD2_a	DQ30_a	DQ29_a	VSSQ_a	DQ26_a	DQ25_a	VSSQ_a	DQS3_c_a	VSSQ_a	DQ14_a	DQ13_a	VSS	VDD1_a	VDD2_a	DQ11_a	DQ10_a	DQ9_a	DQS1_t_a	DM_1_a	VDDQ_a	DQS0_t_a	DQ7_a	DQ6_a	DQ4_a	DQ3_a	VSS	DNU	A
B	VSSQ_b	DNU	DQ31_a	VDDQ_a	DQ28_a	DQ27_a	VDDQ_a	DQ24_a	VDDQ_a	DQS3_t_a	DM3_a	DQ15_a	VDDQ_a	VSSQ_a	Vref(DQ)_a	VDD2_a	DQ12_a	VDDQ_a	DQ8_a	DQS1_c_a	VSSQ_a	DM_0_a	DQS0_c_a	VSSQ_a	VDDQ_a	DQ5_a	DQ2_a	DNU	VSSQ_a	B
C	VDD1_b	DQ16_b																										VDD1_a	VDD2_a	C
D	DQ17_b	VDDQ_b																										DQ1_a	VDDQ_a	D
E	DQ18_b	DQ19_b																										VSSQ_a	DQ0_a	E
F	VSSQ_b	DQ20_b																										DM2_a	VDDQ_a	F
G	DQ21_b	VDDQ_b																										DQS2_t_a	DQS2_c_a	G
H	DQ22_b	DQ23_b																										VSSQ_a	DQ23_a	H
J	VSSQ_b	VDDQ_b																										VDDQ_a	DQ22_a	J
K	DQS2_c_b	DQS2_t_b																										DQ20_a	DQ21_a	K
L	DM2_b	DQ0_b																										DQ19_a	VSSQ_a	L
M	DQ1_b	VSSQ_b																										VDDQ_a	DQ18_a	M
N	DQ2_b	VDD1_b																										DQ16_a	DQ17_a	N
P	VSS	VSS																										VDD2_b	VDD1_b	P
R	VDD1_b	Vref(DQ)_b																										VSS_b	CA0_b	R
T	VDD2_b	VDD2_b																										VDDCA_b	CA1_b	T
U	VDDQ_b	DQ3_b																										Vref(CA)_b	CA2_b	U
V	DQ4_b	VSSQ_b																										VSSCA_b	CA3_b	V
W	DQ6_b	DQ5_b																										CA4_b	CSB1_b	W
Y	VDDQ_b	DQ7_b																										CSB0_b	CKE1_b	Y
AA	DQS0_t_b	DQS0_c_b																										VSSCA_b	CKE0_b	AA
AB	DM0_b	VSSQ_b																										CK_t_b	CK_c_b	AB
AC	VDDQ_b	DM1_b																										VDDCA_b	CA5_b	AC
AD	DQS1_c_b	DQS1_t_b																										CA7_b	CA6_b	AD
AE	DQ8_b	VSSQ_b																										CA8_b	VDDCA_b	AE
AF	DQ9_b	VDDQ_b																										VSSCA_b	CA9_b	AF
AG	DQ10_b	DQ11_b																										VDD2_b	ZQ_b	AG
AH	VSSQ_b	VDD1_b	VDD2_b	DQ13_b	VSSQ_b	DQ15_b	DM3_b	DQS3_t_b	VDDQ_b	DQ26_b	DQ27_b	VDDQ_b	DQ30_b	VSSQ_b	VDD2_a	Vref(CA)_a	CA9_a	VSSCA_a	CA7_a	CA6_a	CK_c_a	VDDCA_a	CKE0_a	CSB0_a	CA3_a	CA2_a	CA1_a	VDD1_a	VSSCA_a	AH
AJ	DNU	VSS	DQ12_b	VDDQ_b	DQ14_b	VDDQ_b	VDDQ_b	DQS3_c_b	DQ24_b	DQ25_b	VSSQ_b	DQ28_b	DQ29_b	DQ31_b	VDD1_a	VSS	ZQ_a	CA8_a	VDDCA_a	CA5_a	CK_t_a	VSSCA_a	CKE1_a	CSB1_a	CA4_a	VDDCA_a	CA0_a	VSS	DNU	AJ
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

Note: 1. 12x12 mm, 0.4mm pitch

2. 216 Ball Count

3. Top View, A1 in Top Left Corner

Pin Configuration – 220 balls PoP-VFBGA Package (Dual Channel)

< TOP View>

See the balls through the package

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	
A	DNU	VSS_b	VDD2_b	VSSQ_b	DQ29_b	DQ28_b	VSSQ_b	DQ25_b	DQ24_b	DQS3_c_b	DM3_b	DQ15_b	VSSQ_b	DQ13_b	DQ11_b	VSSQ_b	DQ9_b	DQS1_c_b	DM1_b	VSSQ_b	VSS_b	VDD2_b	DQS0_c_b	DQ7_b	VSSQ_b	VSS_b	DNU	A
B	VDD1_b	VACC	VDDQ_b	DQ31_b	DQ30_b	VDDQ_b	DQ27_b	DQ26_b	VDDQ_b	DQS3_t_b	VSSQ_b	VDDQ_b	DQ14_b	DQ12_b	VDDQ_b	DQ10_b	DQ8_b	DQS1_t_b	VDDQ_b	Vref(DQ)_b	VDD1-b	DM0_b	DQS0_t_b	VDDQ_b	DQ6_b	VACC	VDD2_b	B
C	DQ16_a	DQ17_a																								DQ5_b	DQ4_b	C
D	DQ18_a	VDDQ_a																								VDDQ_b	DQ3_b	D
E	VSSQ_a	DQ20_a	DQ19_a																						DQ2_b	DQ1_b	VSSQ_b	E
F	DQ21_a	VDDQ_a																								VDDQ_b	DQ0_b	F
G	VSSQ_a	DQ22_a	DQ23_a																						DM2_b	DQS2_t_b	VSSQ_b	G
H	DQS2_t_a	DQS2_c_a																								DQS2_c_b	DQ23_b	H
J	VSSQ_a	DM2_a	DQ0_a																						DQ21_b	DQ22_b	VSSQ_b	J
K	DQ1_a	VDDQ_a																								VDDQ_b	DQ20_b	K
L	VSSQ_a	DQ2_a	DQ3_a																						DQ19_b	DQ18_b	VSSQ_b	L
M	DQ4_a	VDDQ_a																								VDD2_b	DQ17_b	M
N	VSSQ_a	DQ5_a	DQ6_a																						DQ16_b	VDDQ_b	VSS_b	N
P	DQ7_a	VDDQ_a																								VDDCA_a	CA0_a	P
R	VSSQ_a	DQS0_c_a	DQS0_t_a																						CA1_a	CA2_a	VSSCA_a	R
T	DM0_a	VDDQ_a																								CA3_a	CA4_a	T
U	VSS_a	VSSQ_a	Vref(DQ)_a		VDD1_a	VDD1-b																			CS0_n_a	CS1_n_a	VSS_a	U
V	VDD2_a	VDD1_a			VDD2_a	VDD2_b																				CKE0_a	CKE1_a	V
W	VSS_a	VDD2_a	DM1_a		VSS_a	VSS_b																			CK_c_a	CK_t_a	VSSCA_a	W
Y	DQS1_c_a	DQS1_t_a																								VDDCA_a	CA5_a	Y
AA	VSSQ_a	DQ9_a	DQ10_a																						Vref(CA)_a	CA6_a	VDD2_a	AA
AB	DQ8_a	VDDQ_a																								CA7_a	VSS_a	AB
AC	VSSQ_a	DQ11_a	DQ12_a																						CA8_a	CA9_a	VSSCA_a	AC
AD	DQ13_a	DQ14_a																								VDDCA_a	VDD2_a	AD
AE	VSSQ_a	DQ15_a																								VDD1_a	ZQ_a	AE
AF	VSS_a	VDDQ_a	DM3_a	DQS3_t_a	DQS3_c_a	DQ25_a	DQ27_a	VDDQ_a	DQ29_a	DQ31_a	VDD2_a	VDD1_a	VDDCA_b	CA9_b	CA7_b	VDD2_b	Vref(CA)_b	VDDCA_b	CK_t_b	CKE1_b	CS0_n_b	CA4_b	VDDCA_b	CA2_b	CA0_b	VDD2_b	VSS_a	AF
AG	DNU	VDD2_a	VSSQ_a	VDDQ_a	DQ24_a	DQ26_a	VSSQ_a	DQ28_a	DQ30_a	VSSQ_a	VSS_b	ZQ_b	VSSCA_b	CA8_b	CA6_b	CA5_b	VSS_b	VSSCA_b	CK_c_b	CKE0_b	CS1_n_b	VSSCA_b	CA3_b	CA1_b	VSS_b	VDD1_b	DNU	AG

🟪 Channel a
■ Channel b
🟩 Power a
▨ Power b
🟧 Ground
🟨 Do not use
🟦 ZQ

Note: 1. 14x14 mm, 0.5mm pitch, 27 rows

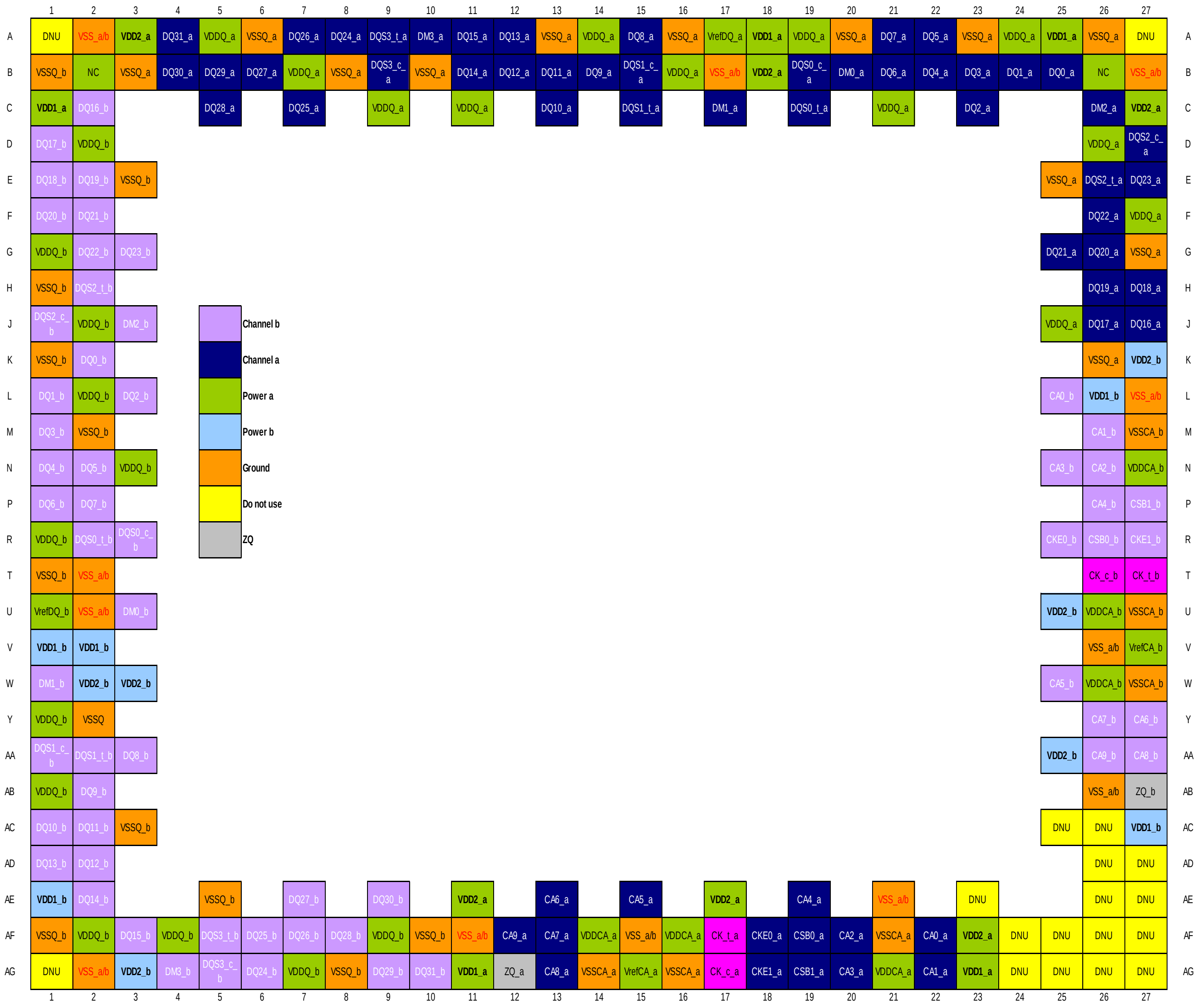
2. 220 Ball Count

3. Top View, A1 in Top Left Corner

Pin Configuration – 240 balls PoP-VFBGA Package (Dual Channel)

< TOP View>

See the balls through the package



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	
A	DNU	VSS_a/b	**VDD2_a**	DQ31_a	VDDQ_a	VSSQ_a	DQ26_a	DQ24_a	DQS3_t_a	DM3_a	DQ15_a	DQ13_a	VSSQ_a	VDDQ_a	DQ8_a	VSSQ_a	VrefDQ_a	**VDD1_a**	VDDQ_a	VSSQ_a	DQ7_a	DQ5_a	VSSQ_a	VDDQ_a	**VDD1_a**	VSSQ_a	DNU	A
B	VSSQ_b	NC	VSSQ_a	DQ30_a	DQ29_a	DQ27_a	VDDQ_a	VSSQ_a	DQS3_c_a	VSSQ_a	DQ14_a	DQ12_a	DQ11_a	DQ9_a	DQS1_c_a	VDDQ_a	VSS_a/b	**VDD2_a**	DQS0_c_a	DM0_a	DQ6_a	DQ4_a	DQ3_a	DQ1_a	DQ0_a	NC	VSS_a/b	B
C	**VDD1_a**	DQ16_b			DQ28_a		DQ25_a		VDDQ_a		VDDQ_a		DQ10_a		DQS1_t_a		DM1_a		DQS0_t_a		VDDQ_a		DQ2_a			DM2_a	**VDD2_a**	C
D	DQ17_b	VDDQ_b																								VDDQ_a	DQS2_c_a	D
E	DQ18_b	DQ19_b	VSSQ_b																						VSSQ_a	DQS2_t_a	DQ23_a	E
F	DQ20_b	DQ21_b																								DQ22_a	VDDQ_a	F
G	VDDQ_b	DQ22_b	DQ23_b																						DQ21_a	DQ20_a	VSSQ_a	G
H	VSSQ_b	DQS2_t_b																								DQ19_a	DQ18_a	H
J	DQS2_c_b	VDDQ_b	DM2_b																						VDDQ_a	DQ17_a	DQ16_a	J
K	VSSQ_b	DQ0_b																								VSSQ_a	**VDD2_b**	K
L	DQ1_b	VDDQ_b	DQ2_b																						CA0_b	**VDD1_b**	VSS_a/b	L
M	DQ3_b	VSSQ_b																								CA1_b	VSSCA_b	M
N	DQ4_b	DQ5_b	VDDQ_b																						CA3_b	CA2_b	VDDCA_b	N
P	DQ6_b	DQ7_b																								CA4_b	CSB1_b	P
R	VDDQ_b	DQS0_t_b	DQS0_c_b																						CKE0_b	CSB0_b	CKE1_b	R
T	VSSQ_b	VSS_a/b																								CK_c_b	CK_t_b	T
U	VrefDQ_b	VSS_a/b	DM0_b																						**VDD2_b**	VDDCA_b	VSSCA_b	U
V	**VDD1_b**	**VDD1_b**																								VSS_a/b	VrefCA_b	V
W	DM1_b	**VDD2_b**	**VDD2_b**																						CA5_b	VDDCA_b	VSSCA_b	W
Y	VDDQ_b	VSSQ																								CA7_b	CA6_b	Y
AA	DQS1_c_b	DQS1_t_b	DQ8_b																						**VDD2_b**	CA9_b	CA8_b	AA
AB	VDDQ_b	DQ9_b																								VSS_a/b	ZQ_b	AB
AC	DQ10_b	DQ11_b	VSSQ_b																						DNU	DNU	**VDD1_b**	AC
AD	DQ13_b	DQ12_b																								DNU	DNU	AD
AE	**VDD1_b**	DQ14_b			VSSQ_b		DQ27_b		DQ30_b		**VDD2_a**		CA6_a		CA5_a		**VDD2_a**		CA4_a		VSS_a/b		DNU			DNU	DNU	AE
AF	VSSQ_b	VDDQ_b	DQ15_b	VDDQ_b	DQS3_t_b	DQ25_b	DQ26_b	DQ28_b	VDDQ_b	VSSQ_b	VSS_a/b	CA9_a	CA7_a	VDDCA_a	VSS_a/b	VDDCA_a	CK_t_a	CKE0_a	CSB0_a	CA2_a	VSSCA_a	CA0_a	**VDD2_a**	DNU	DNU	DNU	DNU	AF
AG	DNU	VSS_a/b	**VDD2_b**	DM3_b	DQS3_c_b	DQ24_b	VDDQ_b	VSSQ_b	DQ29_b	DQ31_b	**VDD1_a**	ZQ_a	CA8_a	VSSCA_a	VrefCA_a	VSSCA_a	CK_c_a	CKE1_a	CSB1_a	CA3_a	VDDCA_a	CA1_a	**VDD1_a**	DNU	DNU	DNU	DNU	AG
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	

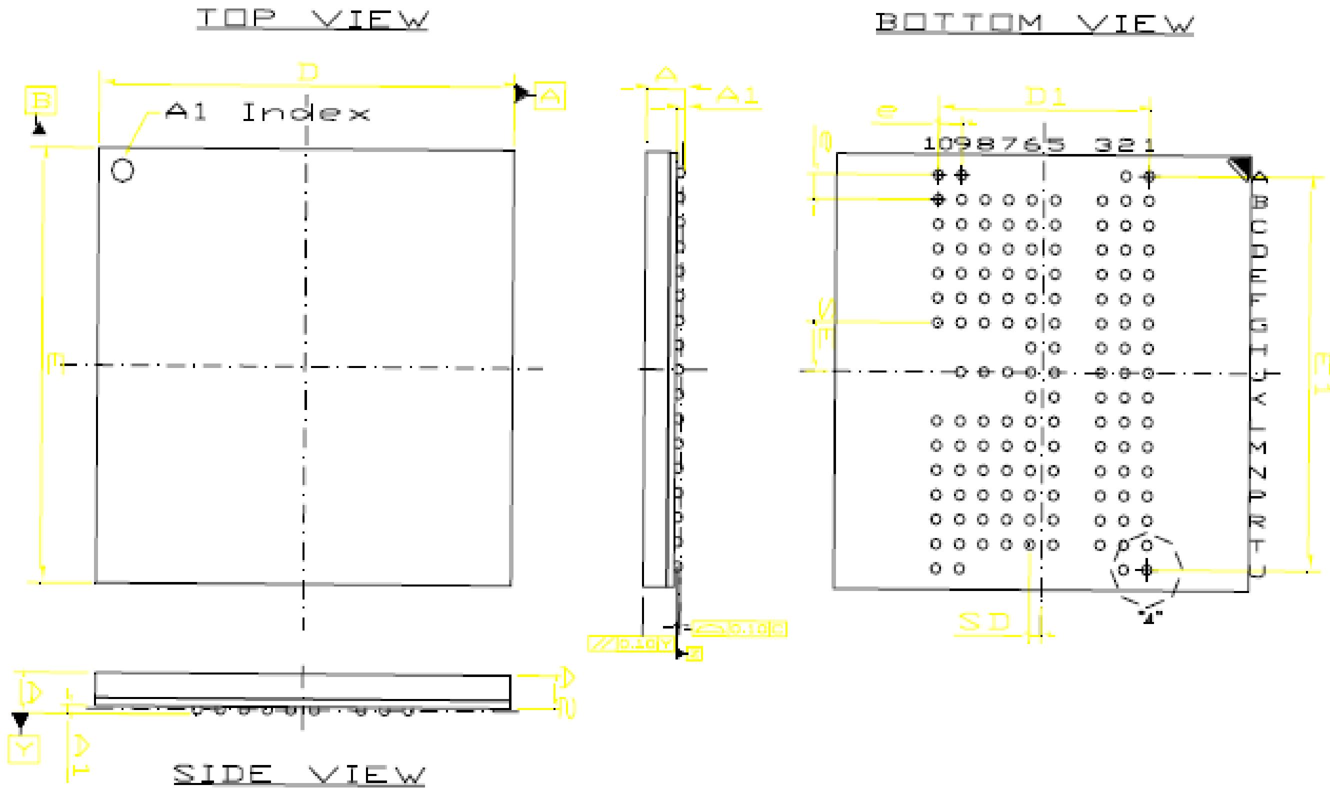
- ■ **Channel b**
- ■ **Channel a**
- ■ **Power a**
- ■ **Power b**
- ■ **Ground**
- ■ **Do not use**
- ■ **ZQ**

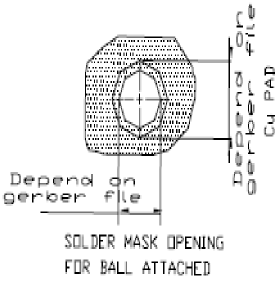
Note: 1. 14x14 mm, 0.5mm pitch, 27 rows

2. 240 Ball Count

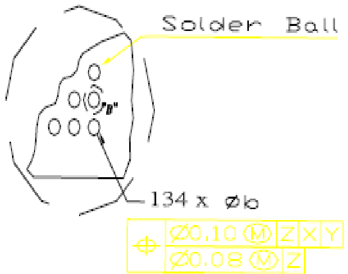
3. Top View, A1 in Top Left Corner

Package Dimensions (134 balls; 11.5mm x 11.5mm)

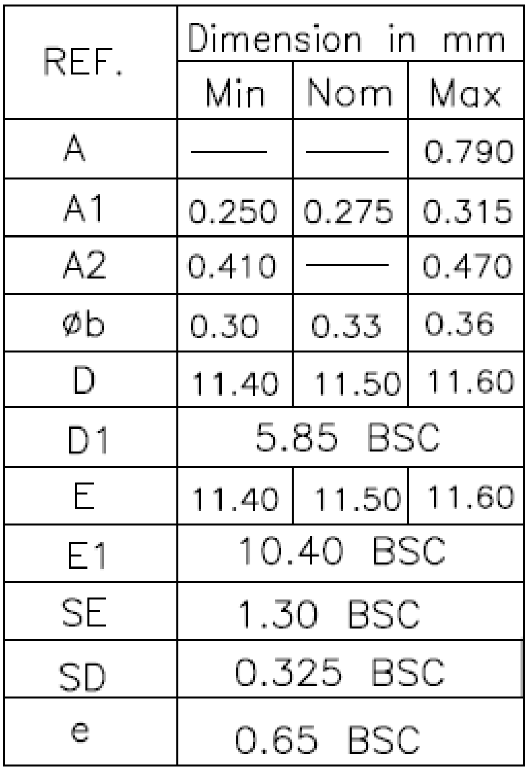




SOLDER MASK OPENING
FOR BALL ATTACHED
Detail B

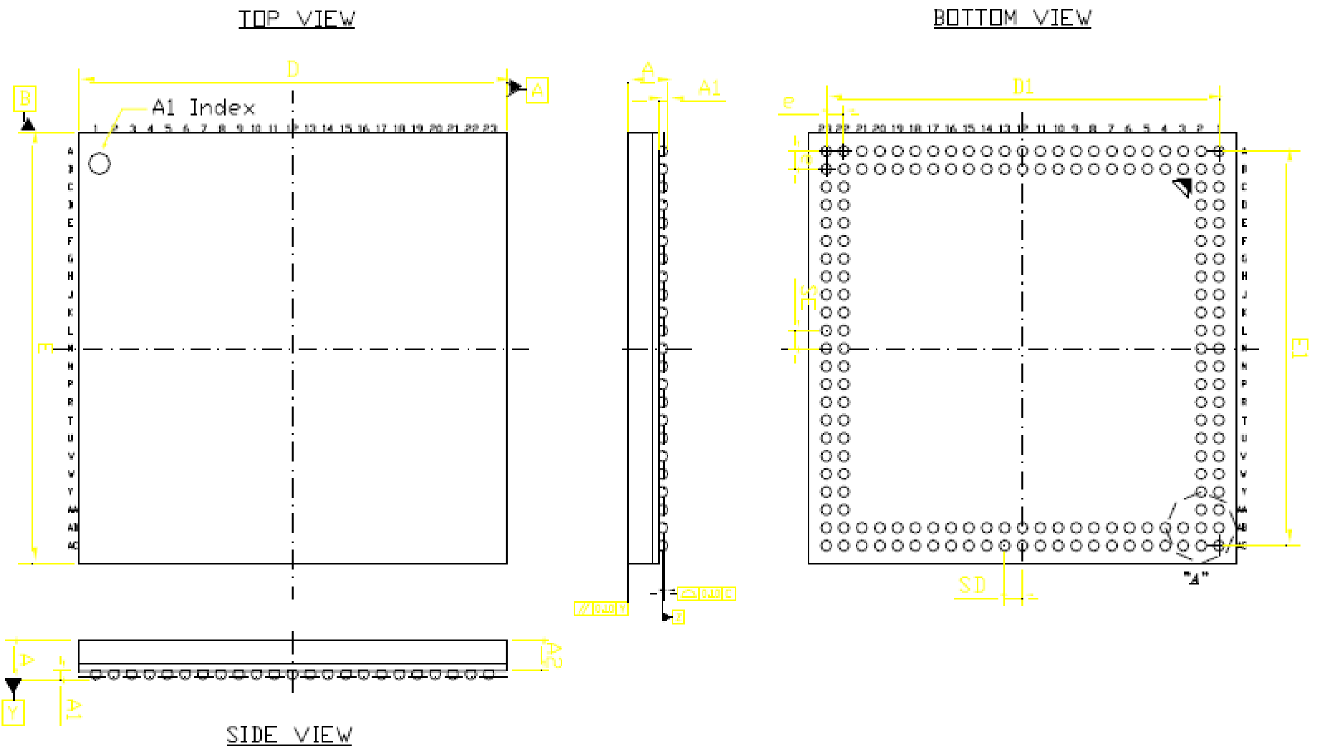


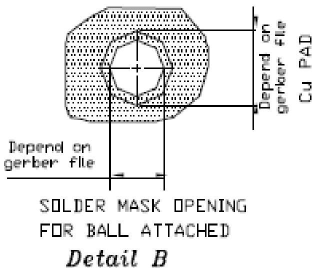
Detail A

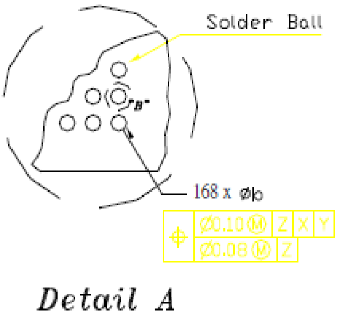


REF.	Dimension in mm		
	Min	Nom	Max
A	——	——	0.790
A1	0.250	0.275	0.315
A2	0.410	——	0.470
Øb	0.30	0.33	0.36
D	11.40	11.50	11.60
D1	5.85 BSC		
E	11.40	11.50	11.60
E1	10.40 BSC		
SE	1.30 BSC		
SD	0.325 BSC		
e	0.65 BSC		

Package Dimensions (168 balls; 12mm x 12mm)

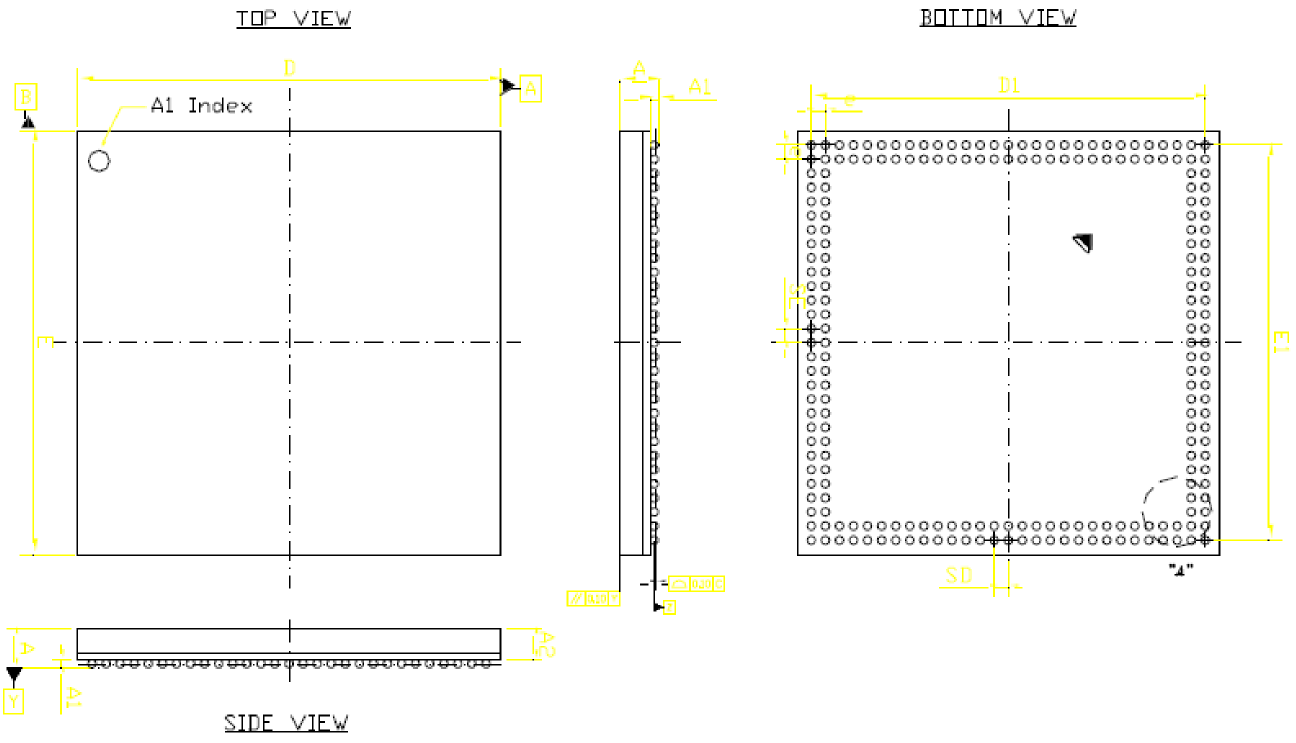


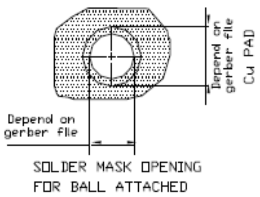




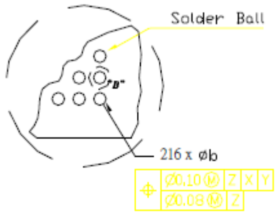
REF.	Dimension in mm		
	Min	Nom	Max
A	——	——	0.790
A1	0.250	0.275	0.315
A2	0.410	——	0.470
⌀b	0.30	0.33	0.36
D	11.90	12.00	12.10
D1	11.00 BSC		
E	119.0	12.00	12.10
E1	11.00 BSC		
SE	0.50 BSC		
SD	0.50 BSC		
e	0.50 BSC		

Package Dimensions (216 balls; 12mm x 12mm)





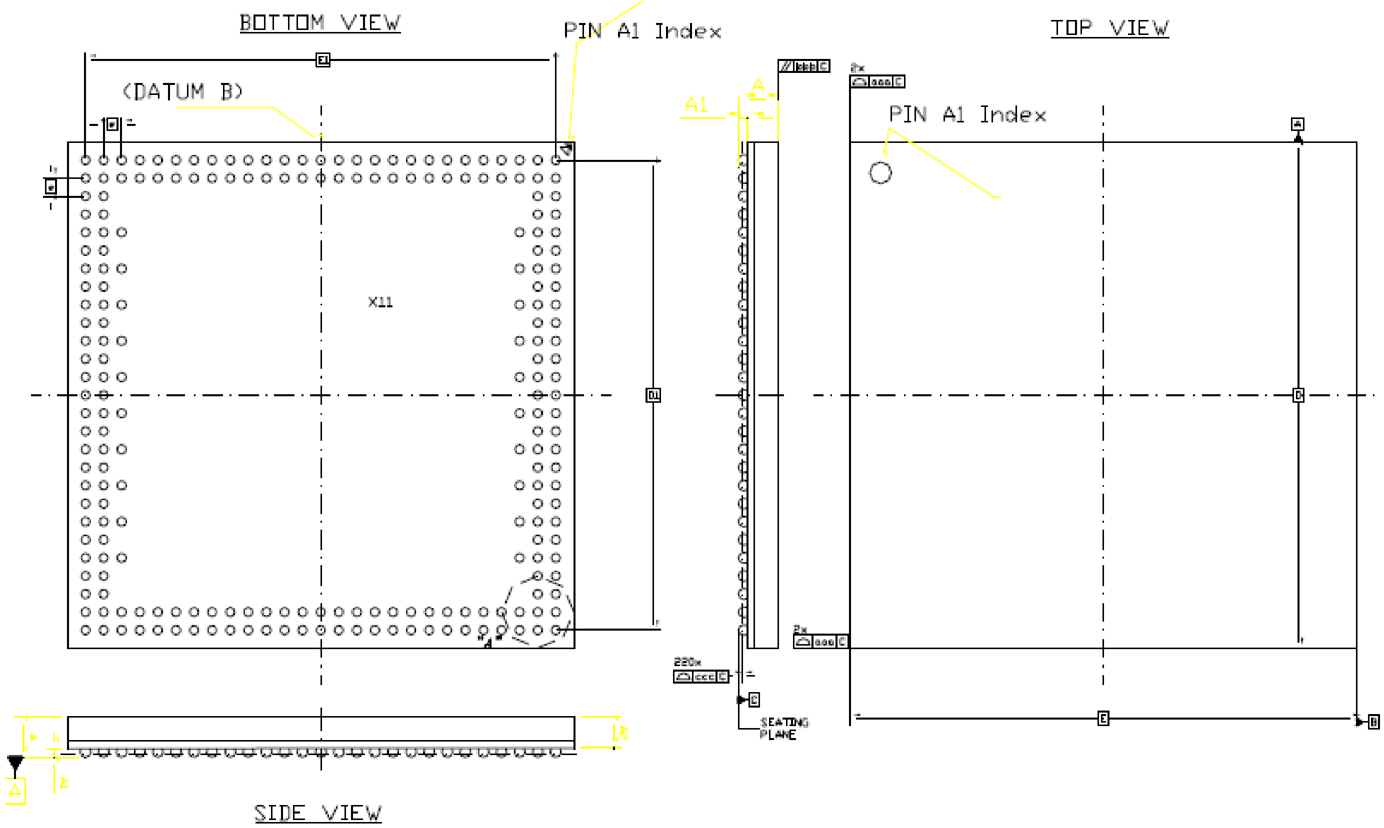
Detail B



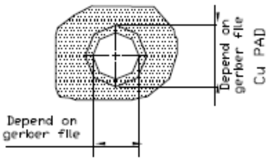
Detail A

REF.	Dimension in mm		
	Min	Nom	Max
A	——	——	0.690
A1	0.150	——	0.210
A2	0.410	——	0.470
øb	0.22	0.25	0.28
D	11.90	12.00	12.10
D1	11.20 BSC		
E	119.0	12.00	12.10
E1	11.20 BSC		
SE	0.40 BSC		
SD	0.40 BSC		
e	0.40 BSC		

Package Dimensions (220 balls 14mm x 14mm)

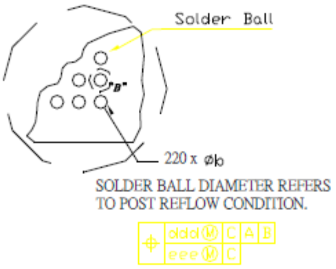


REF.	Dimension in mm		
	Min	Nom	Max
A	——	——	0.790
A1	0.250	0.275	0.315
A2	0.410	——	0.470
Øb	0.30	0.33	0.36
D	14.00 BSC		
D1	13.00 BSC		
E	14.00 BSC		
E1	13.00 BSC		
e	0.50 BSC		
aaa	0.10		
bbb	0.10		
ccc	0.12		
ddd	0.15		
eee	0.05		



SOLDER MASK OPENING FOR BALL ATTACHED

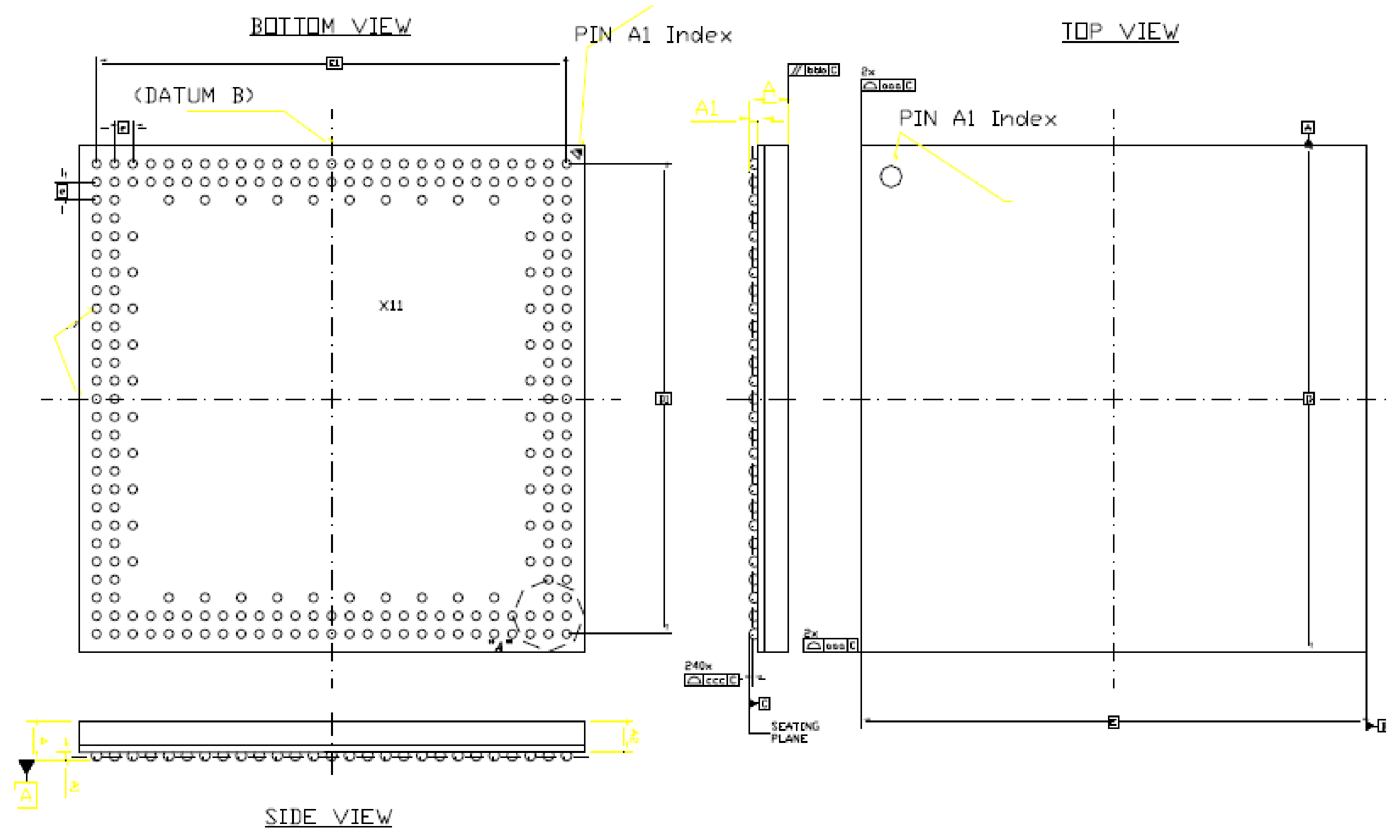
Detail B

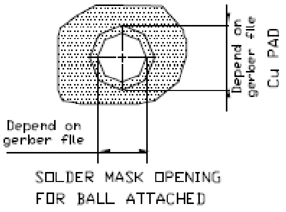


SOLDER BALL DIAMETER REFERS TO POST REFLOW CONDITION.

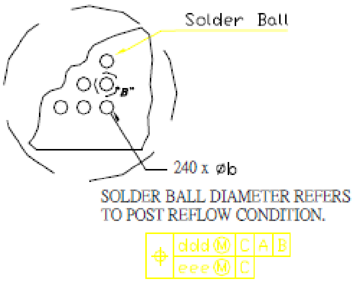
Detail A

Package Dimensions (240 balls 14mm x 14mm)





Detail B



Detail A

REF.	Dimension in mm		
	Min	Nom	Max
A	——	——	0.790
A1	0.250	0.275	0.315
A2	0.410	——	0.470
øb	0.30	0.33	0.36
D	14.00 BSC		
D1	13.00 BSC		
E	14.00 BSC		
E1	13.00 BSC		
e	0.50 BSC		
aaa	0.10		
bbb	0.10		
ccc	0.12		
ddd	0.15		
eee	0.05		

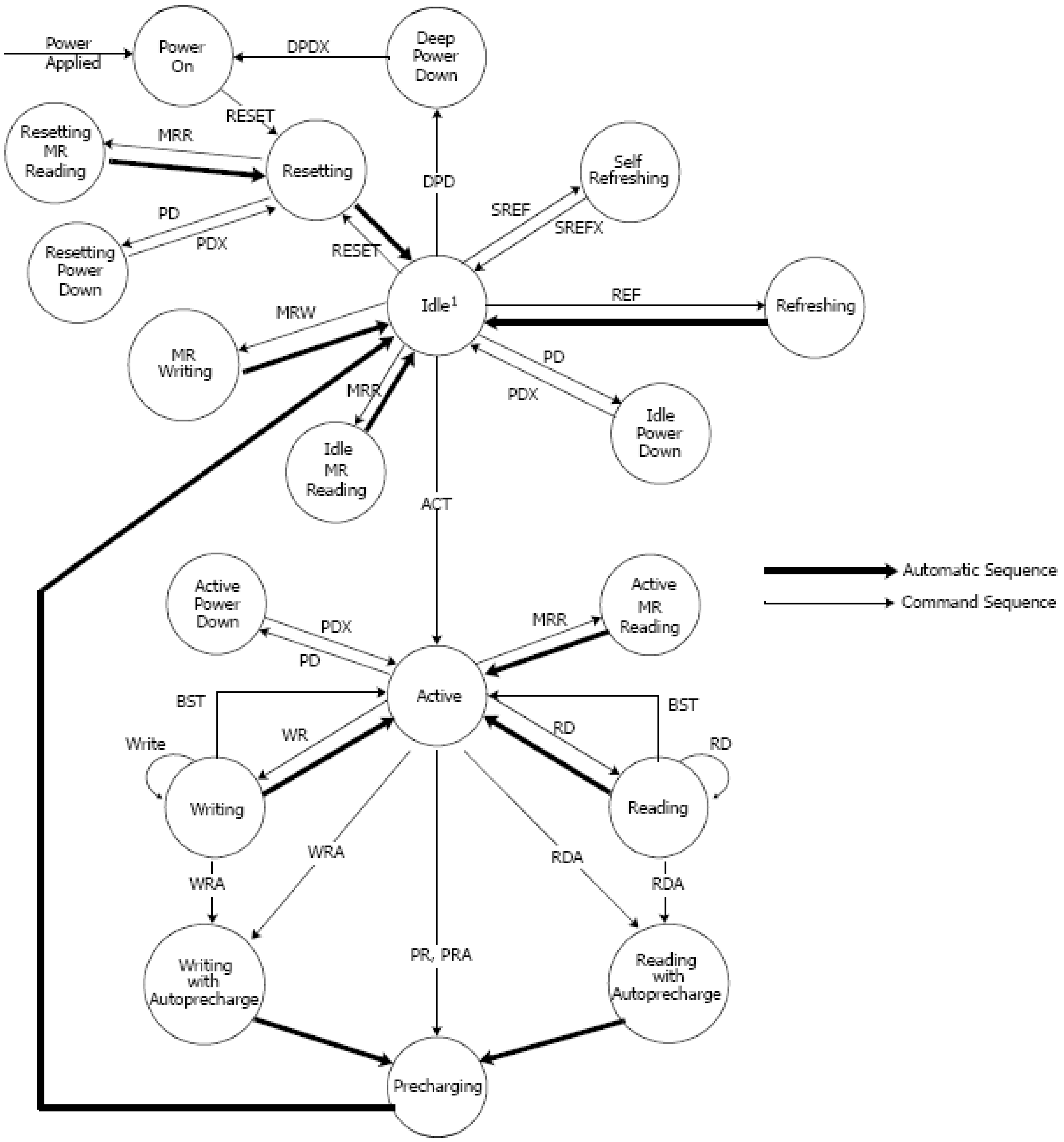
Input / Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All Double Data Rate (DDR) CA input signals are sampled on both positive and negative edge of CK. CS_n and CKE inputs are sampled at the positive edge of CK. AC timings are referenced to clock.
CKE	Input	**Clock Enable:** CKE high activates, and CKE low deactivates internal clock signals, and device input buffers and output drivers. Power saving modes are entered and exited through CKE transitions. CKE is considered part of the command code. CKE is sampled at the positive Clock edge.
CS_n	Input	**Chip Select:** CS_n is considered part of the command code. CS_n is sampled at the positive Clock edge.
CA0 – CA9	Input	**Command/Address Inputs:** Uni-directional command/address bus inputs. Provide the command and address inputs according to the command truth table. CA is considered part of the command code.
DM0-DM3	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading matched the DQ and DQS (or $\overline{DQS}$). DM0 corresponds to the data on DQ0-DQ7, DM1 corresponds to the data on DQ8-DQ15, DM2 corresponds to the data on DQ16-DQ23, and DM3 corresponds to the data on DQ24-DQ31.
DQ0-DQ31	Input/output	**Data Bus:** Bi-directional Input / Output data bus.
DQS, $\overline{DQS}$ DQS0-3, $\overline{DQS0\text{-}3}$	Input/output	**Data Strobe (Bi-directional, Differential):** The data strobe is bi-directional (used for read and write data) and Differential (DQS and $\overline{DQS}$). It is output with read data and input with write data. DQS is edge-aligned to read data, and centered with write data. DQS0 & $\overline{DQS0}$ corresponds to the data on DQ0-DQ7, DQS1 & $\overline{DQS1}$ corresponds to the data on DQ8-DQ15, DQS2 & $\overline{DQS2}$ corresponds to the data on DQ16-DQ23, DQS3 & $\overline{DQS3}$ corresponds to the data on DQ24-DQ31.
NC	-	**No Connect:** No internal electrical connection is present.
ZQ	Input	**Reference Pin for Output Drive Strength Calibration.** External impedance (240-ohm): this signal is used to calibrate the device output impedance.
VDDQ	Supply	**DQ Power Supply:** Isolated on the die for improved noise immunity.
VSSQ	Supply	**DQ Ground:** Isolated on the die for improved noise immunity.
VDDCA	Supply	**Command / Address Power Supply.**
VSSCA	Supply	**Command / Address Ground:** Isolated on the die for improved noise immunity.
VREFDQ, VREFCA	Supply	**Reference Voltage:** VREFDQ is reference for DQ input buffers. VREFCA is reference for Command / Address input buffers.

Symbol	Type	Function
V_{DD1}	Supply	**Core power supply 1.**
V_{DD2}	Supply	**Core power supply2.**
V_{SS}	Supply	**Common Ground.**

Notes: Data includes DQ and DM.

Simplified State Diagram



Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Active	PD	Enter Power Down	REF	Refresh
RD(A)	Read (w/ Autoprecharge)	PDX	Exit Power Down	SREF	Enter self refresh
WR(A)	Write (w/ Autoprecharge)	DPD	Enter Deep Power Down	SREFX	Exit self refresh
PR(A)	Precharge (All)	DPDX	Exit Deep Power Down		
MRW	Mode Register Write	BST	Burst Terminate		
MRR	Mode Register Read	RESET	Reset is achieved through MRW command		

Notes: 1. For LPDDR2-S4 SDRAM in the idle state, all banks are precharged.

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD1}	Voltage on V_{DD1} pin relative to Vss	-0.4	2.3	V
V_{DD2}	Voltage on V_{DD2} pin relative to Vss	-0.4	1.6	V
V_{DDCA}	Voltage on V_{DDCA} pin relative to Vss	-0.4	1.6	V
V_{DDQ}	Voltage on V_{DDQ} pin relative to Vss	-0.4	1.6	V
Vin, Vout	Voltage on any pin relative to Vss	-0.4	1.6	V
Tstg	Storage Temperature (plastic)	-55	+125	°C

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For measurement conditions, refer to the JESD51-2 standard.
3. VDD2 and VDDQ / VDDCA must be within 200Mv of each other at all times.
4. Voltage on any I/O may not exceed voltage on VDDQ; Voltage on any CA input may not exceed voltage on VDDCA.
5. VREF must always be less than all other supply voltages.
6. The voltage difference between any VSS, VSSQ, or VSSCA pins may not exceed 100Mv.

AC/DC Operating Conditions

DC Operating Conditions

Symbol	Parameter	Min	Norm	Max	Unit	Notes
Power Supply						
V_{DD1}	Core Supply voltage 1	1.70	1.80	1.95	V	
V_{DD2}	Core Supply voltage 2	1.14	1.20	1.30	V	
V_{DDCA}	Input Supply Voltage (Command / Address)	1.14	1.20	1.30	V	
V_{DDQ}	I/O Supply voltage (DQ)	1.14	1.20	1.30	V	
Leakage current						
I_I	Input leakage current Any input 0 $\leqq V_{IN} \leqq V_{DDQ} / V_{DDCA}$, All other pins not under test = 0V	-2	-	2	Ua	1
I_{VREF}	V_{REF} leakage current; $V_{REFDQ} = V_{DDQ}/2$ or $V_{REFCA} = V_{DDCA}/2$ (all other pins not under test = 0V)	-1	-	1	Ua	1

Notes:

1. The minimum limit requirement is for testing purposes. The leakage current on VREFCA and VREFDQ pins should be minimal. Although DM is for input only, the DM leakage shall match the DQ and DQS_t, $\overline{\text{DQS\_c}}$ output leakage specification.

Temperature Range

Symbol	Parameter / Condition	Min	Norm	Max	Unit	Notes
T_{CASE}	Commercial	-25	-	+85	°C	
T_{CASE}	Industrial (IT)	-40	-	+85	°C	

Notes:

1. Operating temperature is the case surface temperature at the center of the top side of the device. For measurement conditions, refer to the JESD51-2 standard.
2. Either the device case temperature rating or the temperature sensor (See “Temperature Sensor” on page 117) may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature (SDRAM and NVM). When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} rating that applies for the Standard or Extended Temperature Ranges. For example, T_{CASE} may be above 85°C when the temperature sensor indicates a temperature of less than 85 °C.

AC/DC Input Measurement Level

AC and DC Logic Levels for Single-Ended Signals

CA inputs (Address and Command) and $\overline{CS}$ inputs

Symbol	Parameter	LPDDR2 1066-466		LPDDR2 400-200		Unit	Notes
		Min	Max	Min	Max		
$V_{IHCA(AC)}$	AC Input logic HIGH voltage	V_{REFCA} + 220Mv	-	V_{REFCA} + 300Mv	-	Mv	
$V_{IHCA(DC)}$	DC Input logic HIGH voltage	V_{REFCA} + 130Mv	V_{DDCA}	V_{REFCA} + 200Mv	V_{DDCA}	Mv	
$V_{ILCA(AC)}$	AC Input logic LOW voltage	-	V_{REFCA} – 220Mv	-	V_{REFCA} – 300Mv	Mv	
$V_{ILCA(DC)}$	DC Input logic LOW voltage	V_{SSCA}	V_{REFCA} – 130Mv	V_{SSCA}	V_{REFCA} – 200Mv	Mv	
$V_{REFCA(DC)}$	Reference voltage for CA and $\overline{CS}$ inputs	0.49 x V_{DDCA}	0.51 x V_{DDCA}	0.49 x V_{DDCA}	0.51 x V_{DDCA}	V	
Data inputs (DQ & DM)							
$V_{IHDQ(AC)}$	AC Input logic HIGH voltage	V_{REFDQ} + 220Mv	-	V_{REFDQ} + 300Mv	-	Mv	
$V_{IHDQ(DC)}$	DC Input logic HIGH voltage	V_{REFDQ} + 130Mv	V_{DDQ}	V_{REFDQ} + 200Mv	V_{DDQ}	Mv	
$V_{ILDQ(AC)}$	AC Input logic LOW voltage	-	V_{REFDQ} – 220Mv	-	V_{REFDQ} – 300Mv	Mv	
$V_{ILDQ(DC)}$	DC Input logic LOW voltage	V_{SSQ}	V_{REFDQ} – 130Mv	V_{SSQ}	V_{REFDQ} – 200Mv	Mv	
$V_{REFDQ(DC)}$	Reference voltage for DQ and DM inputs	0.49 x V_{DDQ}	0.51 x V_{DDQ}	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	

Clock enable inputs (CKE)

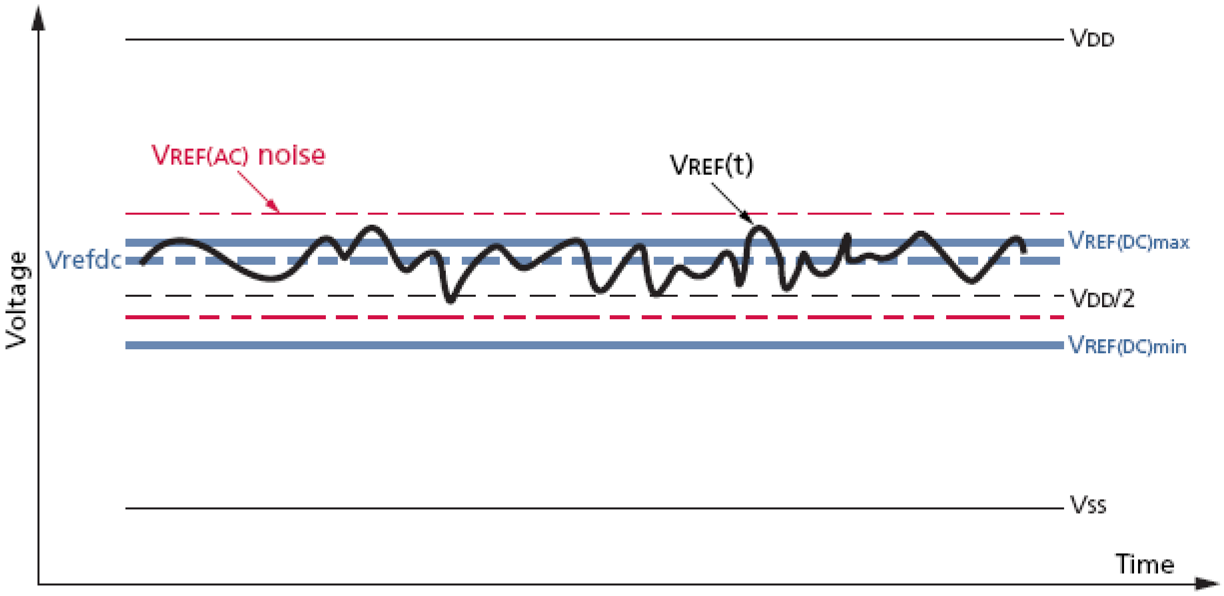
Symbol	Parameter	Min	Max	Unit	Notes
$V_{IHCKE\ (AC)}$	CKE AC Input HIGH voltage	0.8 * V_{DDCA}	-	V	
$V_{ILCKE\ (AC)}$	CKE AC Input LOW voltage	-	0.2 * V_{DDCA}	V	

Notes:

2. V_{DD2} and V_{DDQ}/V_{DDCA} must be within 200Mv of each other all the times.
3. For VREF deviation tolerance, refer to “VREF Tolerance” on page 14.
4. V_{DD} and V_{DDQ} must track each other and V_{DDQ} must be less than or equal to V_{DD}.
5. All voltages referenced to V_{SS}.
6. All parameters assume proper device initialization.
7. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage and temperature range specified.
8. The typical value of $V_{OX\,(AC)}$ is expected to be about 0.5 x V_{DDQ} of the transmitting device and $V_{OX\,(AC)}$ is expected to track variations in V_{DDQ}. $V_{OX\,(AC)}$ indicates the voltage at which differential output signals must cross.
9. The minimum limit requirement is for testing purposes. The leakage current on VREFCA and VREFDQ pins should be minimal. Although DM is for input only, the DM leakage shall match the DQ and DQS_t, $\overline{\text{DQS\_c}}$ output leakage specification.

V_{REF} Tolerance

The DC tolerance limits and AC noise limits for the reference voltages V_{REFCA} and V_{REFDQ} are illustrated bellow. This figure shows a valid reference voltage V_{REF}(t) as a function of time. VDD is used in place of V_{DDCA} for V_{REFCA}, and V_{DDQ} for V_{REFDQ}. $V_{REF(DC)}$ is the linear average of V_{REF}(t) over a very long period of time (e.g., 1 second) and is specified as a fraction of the linear average of V_{DDQ} or V_{DDCA}, also over a very long period of time (e.g., 1 second). This average must meet the MIN/MAX requirements. Additionally, V_{REF}(t) can temporarily deviate from $V_{REF(DC)}$ by no more than ±1% VDD. V_{REF}(t) cannot track noise on V_{DDQ} or V_{DDCA} if doing so would force V_{REF} outside these specifications.



V_{REF} DC Tolerance and V_{REF} AC Noise Limits

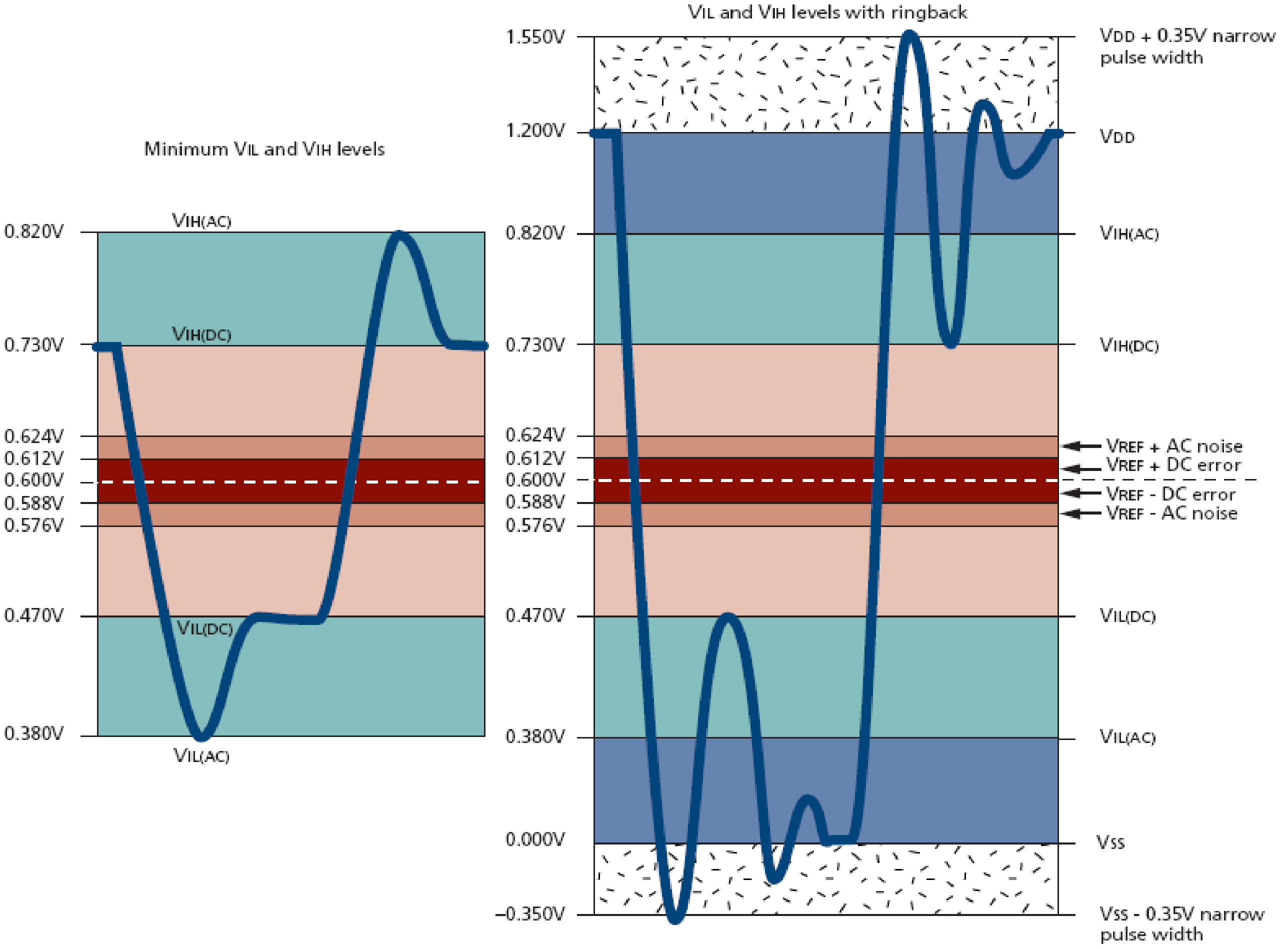
The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $V_{IH(DC)}$, $V_{IL(AC)}$, and $V_{IL(DC)}$ are dependent on V_{REF}. V_{REF} DC variations affect the absolute voltage a signal must reach to achieve a valid HIGH or LOW, as well as the time from which setup and hold times are measured. When V_{REF} is outside the specified levels, devices will function correctly with appropriate timing deratings as long as:

- V_{REF} is maintained between 0.44 x V_{DDQ} (or V_{DDCA}) and 0.56 x V_{DDQ} (or V_{DDCA}), and the controller achieves the required single-ended AC and DC input levels from instantaneous V_{REF}.

System timing and voltage budgets must account for V_{REF} deviations outside this range.

The setup/hold specification and derating values must include time and voltage associated with V_{REF} AC noise. Timing and voltage effects due to AC noise on VREF up to the specified limit (±1% VDD) are included in LPDDR2 timings and their associated deratings.

Input Signal

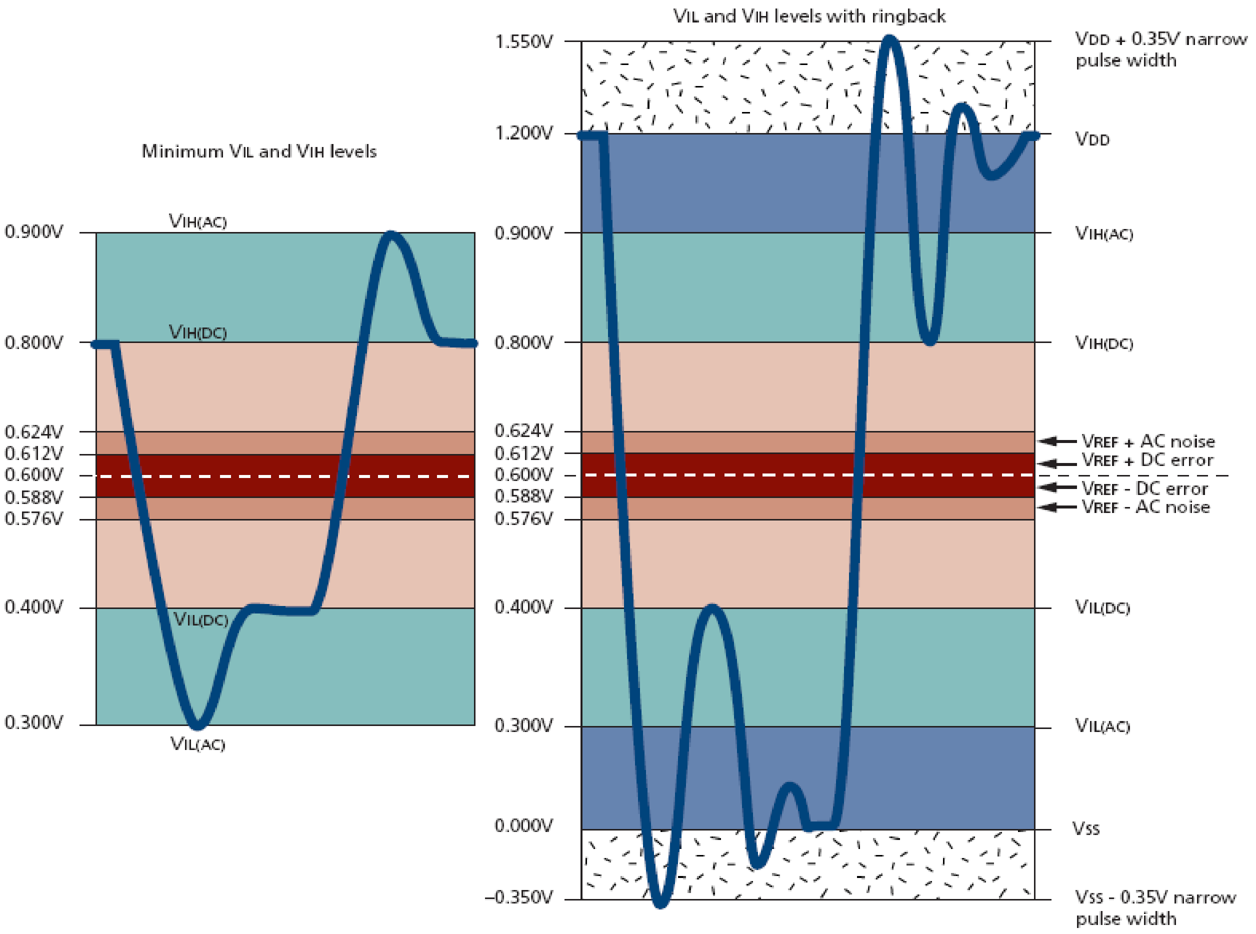


LPDDR2 466-1066 Input Signal

Notes:

1. Numbers reflect typical values.
2. For CA[9:0], CK, $\overline{\text{CK}}$, $\overline{\text{CS}}$, and CKE, VDD stands for VDDCA. For DQ, DM, DQS, and $\overline{\text{DQS}}$, VDD stands for VDDQ.
3. For CA[9:0], CK, $\overline{\text{CK}}$, $\overline{\text{CS}}$, and CKE, VSS stands for VSSCA. For DQ, DM, DQS, and $\overline{\text{DQS}}$, VSS stands for VSSQ.

Input Signal (Continued)

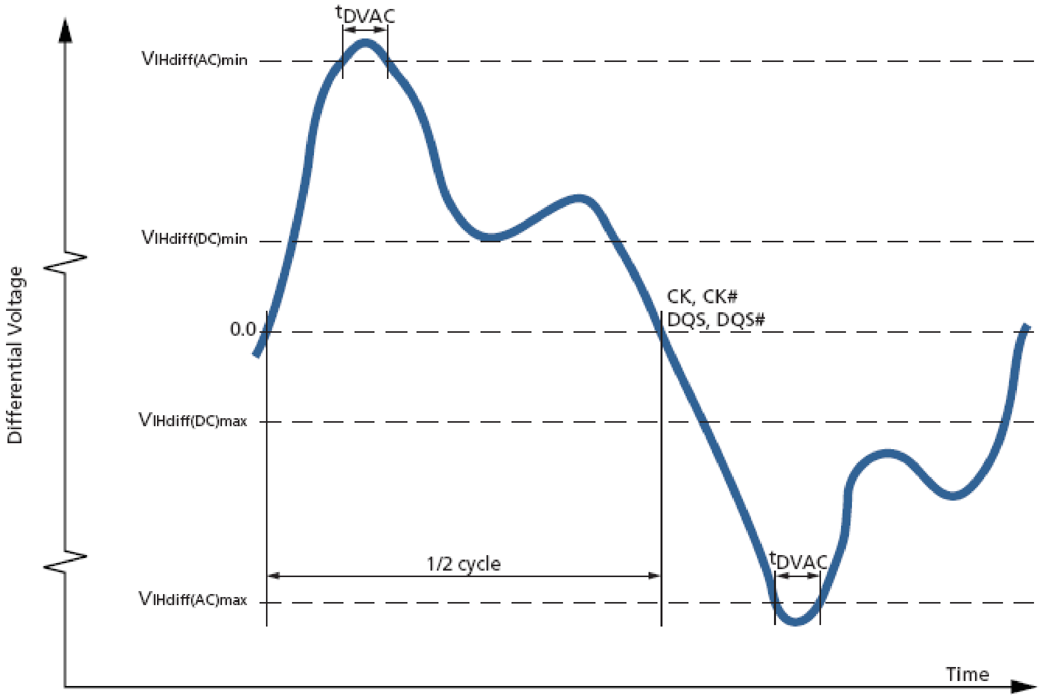


LPDDR2 200-400 Input Signal

Notes:

1. Numbers reflect typical values.
2. For CA[9:0], CK, $\overline{\text{CK}}$, $\overline{\text{CS}}$, and CKE, VDD stands for VDDCA. For DQ, DM, DQS, and $\overline{\text{DQS}}$, VDD stands for VDDQ.
3. For CA[9:0], CK, $\overline{\text{CK}}$, $\overline{\text{CS}}$, and CKE, VSS stands for VSSCA. For DQ, DM, DQS, and $\overline{\text{DQS}}$, VSS stands for VSSQ.

AC and DC Logic Levels for Differential Signals



Differential AC and DC Input Levels

Differential Inputs logical levels (CK, $\overline{CK}$ – V_{REF} = $V_{REFCA(DC)}$; DQS, $\overline{DQS}$: V_{REF} = $V_{REFDQ(DC)}$)

Symbol	Parameter	LPDDR2 1066-466		LPDDR2 400-200		Unit	Notes
		Min	Max	Min	Max		
$V_{Ihdiff(AC)}$	Differential input voltage HIGH AC	2 x $(V_{IH(AC)}-V_{REF})$	Note 3	2 x $(V_{IH(AC)}-V_{REF})$	Note 3	V	
$V_{Ildiff(AC)}$	Differential input voltage LOW AC	Note 3	2 x $(V_{REF}-V_{IL(AC)})$	Note 3	2 x $(V_{REF}-V_{IL(AC)})$	V	
$V_{Ihdiff(DC)}$	Differential input voltage HIGH DC	2 x $(V_{IH(DC)}-V_{REF})$	Note 3	2 x $(V_{IH(DC)}-V_{REF})$	Note 3	V	
$V_{Ildiff(DC)}$	Differential input voltage LOW DC	Note 3	2 x $(V_{REF}-V_{IL(DC)})$	Note 3	2 x $(V_{REF}-V_{IL(DC)})$	V	

Notes:

1. Used to define a differential signal slew-rate. For CK_t – CK_c use VIH/VIL(dc) of CA and VREFCA; for DQS_t – DQS_c, use VIH/VIL(dc) of DQs and VREFDQ; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.

2. For CK and $\overline{CK}$, use $V_{IH/VIL(AC)}$ of CA and V_{REFCA}; for DQS and $\overline{DQS}$, use $V_{IH/VIL(AC)}$ of DQ and V_{REFDQ}. If a reduced AC HIGH or AC LOW is used for a signal group, the reduced voltage level also applies.

3. These values are not defined, however the single-ended signals CK, $\overline{CK}$, DQS, and $\overline{DQS}$ must be within the respective limits ($V_{IH(DC)}$max, $V_{IL(DC)}$min) for single-ended signals and must comply with the specified limitations for overshoot and undershoot.

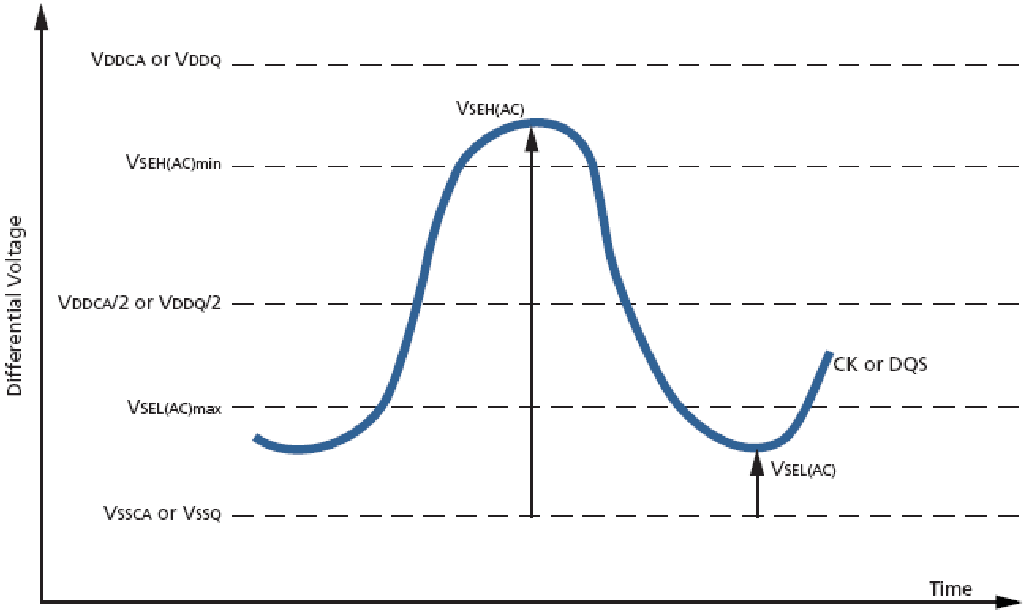
CK, $\overline{CK}$ and DQS, $\overline{DQS}$ Time Requirement before Ring back (t_{DVAC})

Slew Rate (V/ns)	t_{DVAC}(ps) at $V_{IH}/V_{Ildiff(AC)}$ = 440Mv	t_{DVAC}(ps) at $V_{IH}/V_{Ildiff(AC)}$ = 600Mv
	Min	Max
>4.0	175	75
4.0	170	57
3.0	167	50
2.0	163	38
1.8	162	34
1.6	161	29
1.4	159	22
1.2	155	13
1.0	150	0
<1.0	150	0

Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (CK, $\overline{CK}$, DQS, and $\overline{DQS}$) must also comply with certain requirements for single-ended signals. CK and $\overline{CK}$ must meet $V_{SEH(AC)}$min/$V_{SEL(AC)}$max in every half cycle. DQS, $\overline{DQS}$ must meet $V_{SEH(AC)}$min/$V_{SEL(AC)}$max in every half cycle preceding and following a valid transition.

The applicable AC levels for CA and DQ differ by speed-bin.



Single-Ended Requirement for Differential Signals

Note that while CA and DQ signal requirements are referenced to VREF, the single-ended components of differential signals also have a requirement with respect to VDDQ/2 for DQS, and VDDCA/2 for CK. The transition of single-ended signals through the AC levels is used to measure setup time. For single-ended components of differential signals, the requirement to reach $V_{SEL(AC)}$max or $V_{SEH(AC)}$min has no bearing on timing; this requirement does, however, add a restriction on the common mode characteristics of these signals.

Single-Ended Levels for CK, $\overline{\text{CK}}$, DQS, $\overline{\text{DQS}}$

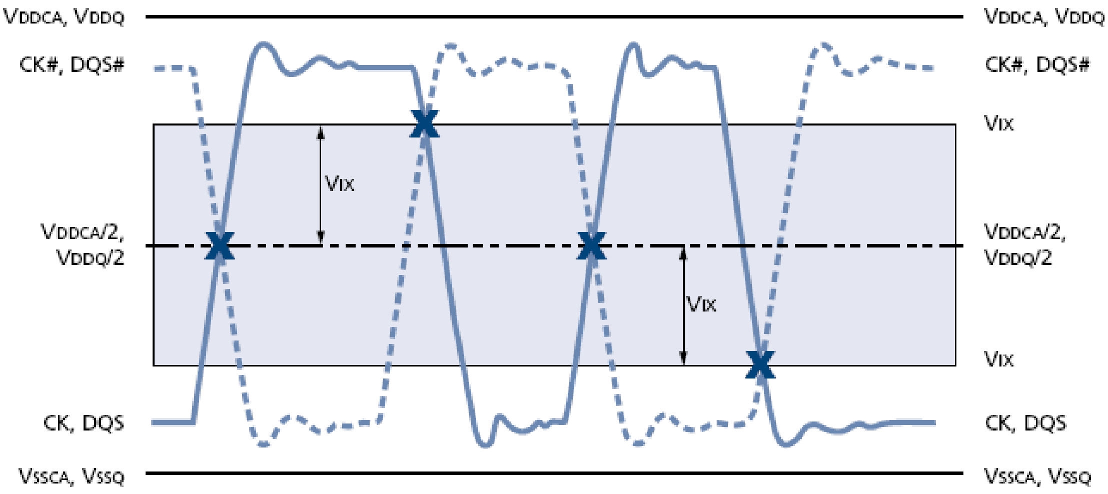
Symbol	Parameter	LPDDR2 1066-466		LPDDR2 400-200		Unit	Notes
		Min	Max	Min	Max		
$V_{SEH(AC)}$	Single-ended HIGH level for strobes	$(V_{DDQ}/2)+0.22$	Note 3	$(V_{DDQ}/2)+0.30$	Note 3	V	
	Single-ended HIGH level for CK, $\overline{\text{CK}}$	$(V_{DDCA}/2)+0.22$	Note 3	$(V_{DDCA}/2)+0.30$	Note 3	V	
$V_{SEL(AC)}$	Single-ended LOW level for strobes	Note 3	$(V_{DDQ}/2)-0.22$	Note 3	$(V_{DDQ}/2)+0.30$	V	
	Single-ended LOW level for CK, $\overline{\text{CK}}$	Note 3	$(V_{DDCA}/2)-0.22$	Note 3	$(V_{DDCA}/2)+0.30$	V	

Notes:

1. For CK and $\overline{\text{CK}}$, use $V_{SEH}/V_{SEL(AC)}$ of CA; for strobes (DQS[3:0] and $\overline{\text{DQS}}$[3:0]) use $V_{IH}/V_{IL(AC)}$ of DQ.
2. $V_{IH(AC)}$ and $V_{IL(AC)}$ for DQ are based on V_{REFDQ}; $V_{SEH(AC)}$ and $V_{SEL(AC)}$ for CA are based on V_{REFCA}. If a reduced AC HIGH or AC LOW is used for a signal group, the reduced level applies.
3. These values are not defined, however the single-ended signals CK, $\overline{\text{CK}}$, DQS0, $\overline{\text{DQS0}}$, DQS1, $\overline{\text{DQS1}}$, DQS2, $\overline{\text{DQS2}}$, DQS3, $\overline{\text{DQS3}}$ must be within the respective limits ($V_{IH(DC)max}$, $V_{IL(DC)min}$) for single-ended signals, and must comply with the specified limitations for overshoot and undershoot.

Differential input Cross-Point Voltage

To ensure tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross-point voltage of differential input signals (CK, $\overline{CK}$, DQS, and $\overline{DQS}$) must meet the specifications bellow. The differential input cross-point voltage (**V_{IX}**) is measured from the actual cross point of true and complement signals to the midlevel between VDD and Vss .



V_{IX} definition

Cross-Point Voltage for Differential Input Signals (CK, $\overline{CK}$, DQS, $\overline{DQS}$)

Symbol	Parameter	LPDDR2 200-1066		Unit	Notes
		Min	Max		
$V_{IXCA(AC)}$	Differential input cross-point voltage relative to VDDCA/2 for CK and $\overline{CK}$	-120	+120	Mv	
$V_{IXDQ(AC)}$	Differential input cross-point voltage relative to VDDQ/2 for DQS and $\overline{DQ}$	-120	+120	Mv	

Notes:

1. The typical value of $V_{IX(AC)}$ is expected to be about 0.5 × VDD of the transmitting device, and it is expected to track variations in VDD. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.
2. For CK and $\overline{CK}$, $V_{REF} = V_{REFCA(DC)}$. For DQS and $\overline{DQS}$, $V_{REF} = V_{REFDQ(DC)}$.

Slew Rate Definitions for Single-Ended Input Signals

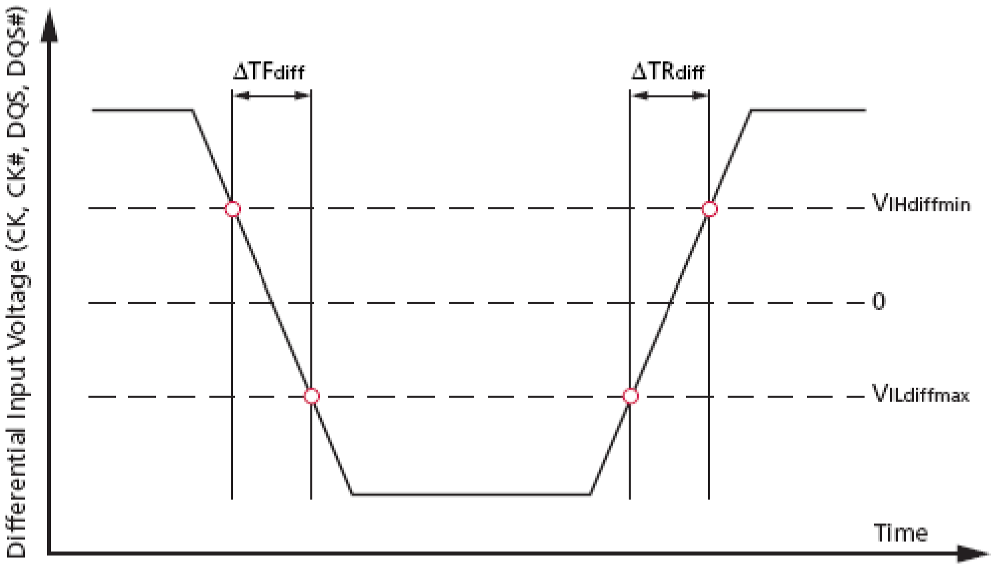
Refer to page 51, 57 for single-ended slew rate definition for address, command and data signals respectively.

Slew Rate Definitions for Differential Input Signals

Description	Defined by	Measured	
		From	To
Differential input slew rate for rising edge (CK, $\overline{CK}$ and DQS, $\overline{DQS}$)	$[V_{IHdiffmin} – V_{ILdiffmax}] / \Delta TR_{diff}$	$V_{ILdiffmax}$	$V_{IHdiffmin}$
Differential input slew rate for falling edge (CK, $\overline{CK}$ and DQS, $\overline{DQS}$).	$[V_{IHdiffmin} – V_{ILdiffmax}] / \Delta TF_{diff}$	$V_{IHdiffmin}$	$V_{ILdiffmax}$

Notes:

The differential signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) must be linear between these thresholds.



Differential Input Slew Rate Definition for CK, $\overline{CK}$, DQS and $\overline{DQS}$

AC/DC Output Measurement Level

Single-Ended AC and DC Output Levels

Symbol	Parameter		LPDDR2 200-1066	Unit	Notes
VOH(AC)	AC output HIGH measurement level (for output slew rate)		VREF + 0.12	V	
VOL(AC)	AC output LOW measurement level (for output slew rate)		VREF – 0.12	V	
VOH(DC)	DC output HIGH measurement level (for I-V curve linearity)		0.9 x VDDQ	V	
VOL(DC)	DC output LOW measurement level (for I-V curve linearity)		0.1 x VDDQ	V	
IOZ	Output leakage current (DQ, DM, DQS, $\overline{DQS}$) (DQ, DQS, $\overline{DQS}$ are disabled; 0V ≤ VOUT ≤ VDDQ)	Min	-5	Ua	
		Max	5	Ua	
Mmpupd	Delta output impedance between pull-up and pull-down for DQ/DM	Min	-15	%	
		Max	15	%	

Notes:

1. I_{OH} = –0.1Ma.
2. I_{OL} = 0.1Ma.

Differential AC and DC Output Levels

Symbol	Parameter	LPDDR2 200-1066	Unit	Notes
VOHdiff(AC)	AC differential output HIGH measurement level (for output slew rate)	+ 0.20 x VDDQ	V	
VOLdiff(AC)	AC differential output LOW measurement level (for output slew rate)	- 0.20 x VDDQ	V	

Notes:

1. I_{OH} = –0.1Ma.
2. I_{OL} = 0.1Ma.

Single Ended Output Slew Rate

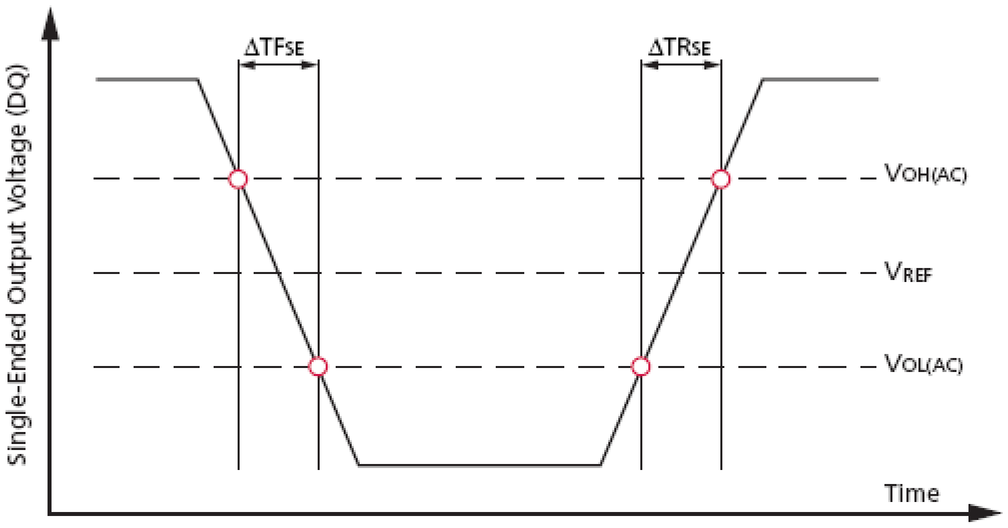
With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown below.

Single-Ended Output Slew Rate Definition

Description	Defined by	Measured	
		From	To
Single-ended output slew rate for rising edge	[VOH(AC) – VOL(AC)] / ΔTRSE	VOL(AC)	VOH(AC)
Single-ended output slew rate for falling edge	[VOH(AC) – VOL(AC)] / ΔTFSE	VOH(AC)	VOL(AC)

Notes:

Output slew rate is verified by design and characterization, and may not be subject to production testing.



Single-Ended Output Slew Rate Definition

Single-Ended Output Slew Rate

Symbol	Parameter	LPDDR2 200-1066		Unit
		Min	Max	
SRQSE	Single-ended output slew rate (output impedance = 40Ω ± 30%)	1.5	3.5	V/ns
SRQSE	Single-ended output slew rate (output impedance = 60Ω ± 30%)	1.0	2.5	V/ns
	Output slew-rate-matching ratio (pull-up to pull-down)	0.7	1.4	
Definitions: SR = slew rate, Q = query output (similar to DQ = data-in, query-output), se = single-ended signals				

Notes:

1. Measured with output reference load.
2. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage over the entire temperature and voltage range. For a given output, the ratio represents the maximum difference between pull-up and pull-down drivers due to process variation.
3. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.
4. Slew rates are measured under typical simultaneous switching output (SSO) conditions, with one-half of DQ signals per data byte driving HIGH and one-half of DQ signals per data byte driving LOW.

Differential Output Slew Rate

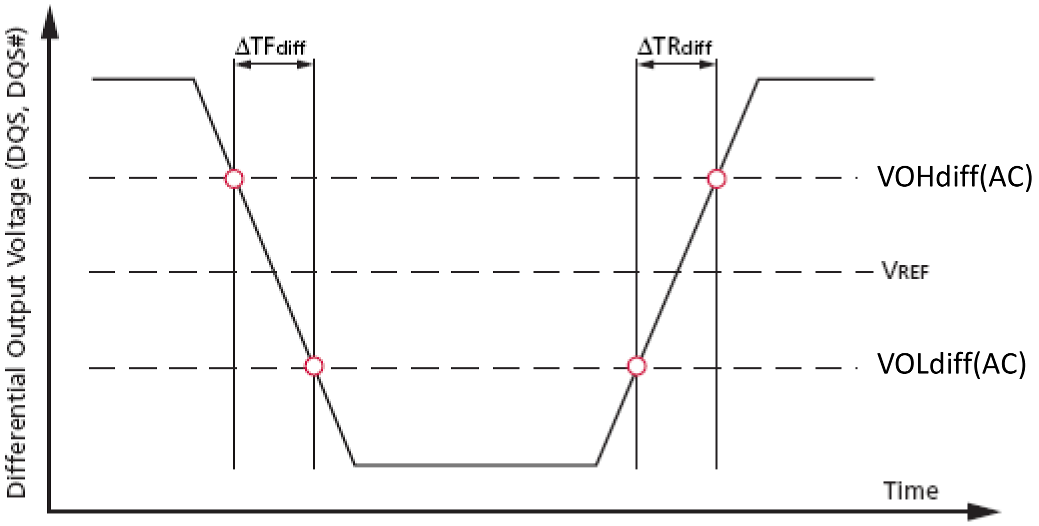
With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between $V_{Oldiff(AC)}$ and $V_{Ohdiff(AC)}$ for differential signals as shown below.

Differential Input Slew Rate Definition

Description	Defined by	Measured	
		From	To
Differential output slew rate for rising edge	[VOHdiff(AC) – VOLdiff(AC)] / ΔTRdiff	VOLdiff(AC)	VOHdiff(AC)
Differential output slew rate for falling edge	[VOHdiff(AC) – VOLdiff(AC)] / ΔTFdiff	VOHdiff(AC)	VOLdiff(AC)

Notes:

Output slew rate is verified by design and characterization, and may not be subject to production testing.



Differential Output Slew Rate Definition

Differential Input Slew Rate

Symbol	Parameter	LPDDR2 200-1066		Unit
		Min	Max	
SRQ_{diff}	Differential output slew rate (output impedance = 40Ω ± 30%)	3.0	7.0	V/ns
SRQ_{diff}	Differential output slew rate (output impedance = 60Ω ± 30%)	2.0	5.0	V/ns
Definitions: SR = slew rate, Q = query output (similar to DQ = data-in, query-output), diff = differential signals				

Notes:

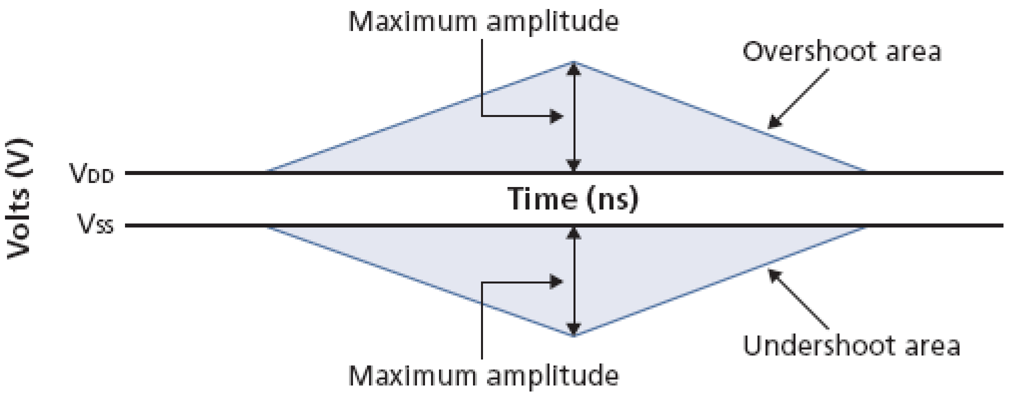
1. Measured with output reference load.
2. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$.
3. Slew rates are measured under typical simultaneous switching output (SSO) conditions, with one-half of DQ signals per data byte driving HIGH and one-half of DQ signals per data byte driving LOW.

AC Overshoot/Undershoot Specification

Parameter		1066	933	800	667	533	400	333	Unit
Maximum peak amplitude provided for overshoot area	Max	0.35							V
Maximum peak amplitude provided for undershoot area	Max	0.35							V
Maximum area above VDD	Max	0.15	0.17	0.20	0.24	0.30	0.40	0.48	V
Maximum area below VSS	Max	0.15	0.17	0.20	0.24	0.30	0.40	0.48	V

Notes:

1. VDD stands for VDDCA for CA[9:0], CK, $\overline{CK}$, $\overline{CS}$, and CKE. VDD stands for VDDQ for DQ, DM, DQS, and $\overline{DQS}$.
2. VSS stands for VSSCA for CA[9:0], CK, $\overline{CK}$, $\overline{CS}$, and CKE. VSS stands for VSSQ for DQ, DM, DQS, and $\overline{DQS}$.
3. Values are referenced from actual VDDQ, VDDCA, VSSQ and VSSCA levels.



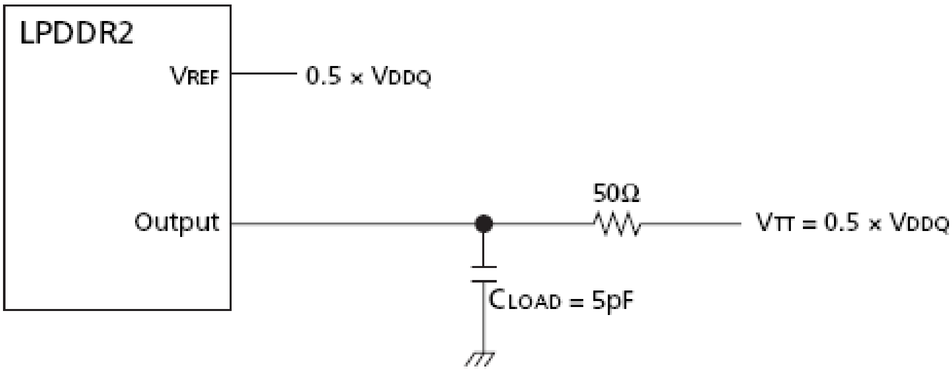
Overshoot and Undershoot Definition

Notes:

1. VDD stands for VDDCA for CA[9:0], CK, $\overline{CK}$, $\overline{CS}$, and CKE. VDD stands for VDDQ for DQ, DM, DQS, and $\overline{DQS}$.
2. VSS stands for VSSCA for CA[9:0], CK, $\overline{CK}$, $\overline{CS}$, and CKE. VSS stands for VSSQ for DQ, DM, DQS, and $\overline{DQS}$.

HSUL_12 Driver Output Timing Reference Load

The timing reference loads are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally with one or more coaxial transmission lines terminated at the tester electronics.



HSUL_12 Driver Output Reference Load for Timing and Slew Rate

Notes:

All output timing parameter values (Tdqsck, Tdqsq, Tqhs, Thz, Trpre etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

Output Driver Impedance Definition

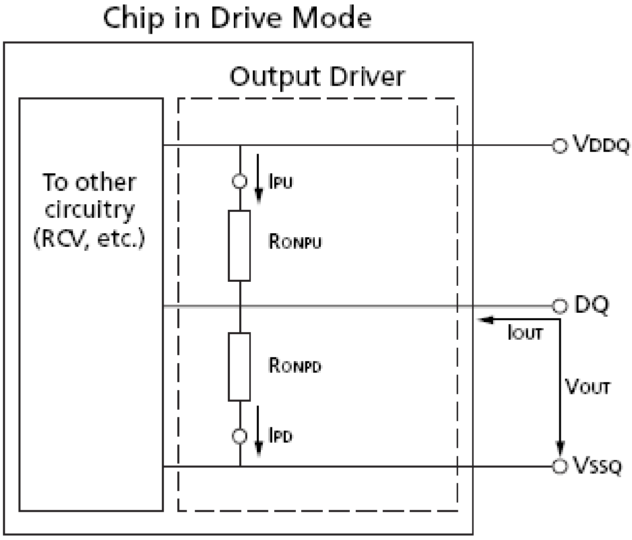
The output driver impedance is selected by a mode register during initialization. The selected value is able to maintain the tight tolerances specified if proper ZQ calibration is performed. Output specifications refer to the default output driver unless specifically stated otherwise. A functional representation of the output buffer is shown in below. The output driver impedance RON is defined by the value of the external reference resistor RZQ as follows:

$$R_{ONPU} = \frac{V_{DDQ} - V_{OUT}}{ABS(I_{OUT})}$$

When R_{ONPD} is turned off.

$$R_{ONPD} = \frac{V_{OUT}}{ABS(I_{OUT})}$$

When R_{ONPU} is turned off.



Output Driver

RON_{PU} and RON_{PD} Characteristics with ZQ Calibration

Output driver impedance RON is defined by the value of the external reference resistor RZQ. Typical RZQ is 240Ω.

Output Driver DC Electrical Characteristics with ZQ Calibration

R_{Onnom}	Resistor	V_{OUT}	Min	Typ	Max	Unit
34.3Ω	RON34PD	0.5 × VDDQ	29.2	34.3	39.4	Ω
	RON34PU	0.5 × VDDQ	29.2	34.3	39.4	Ω
40.0Ω	RON40PD	0.5 × VDDQ	34	40	46	Ω
	RON40PU	0.5 × VDDQ	34	40	46	Ω
48.0Ω	RON48PD	0.5 × VDDQ	40.8	48	55.2	Ω
	RON48PU	0.5 × VDDQ	40.8	48	55.2	Ω
60.0Ω	RON60PD	0.5 × VDDQ	51	60	69	Ω
	RON60PU	0.5 × VDDQ	51	60	69	Ω
80.0Ω	RON80PD	0.5 × VDDQ	68	80	92	Ω
	RON80PU	0.5 × VDDQ	68	80	92	Ω
120.0Ω	RON120PD	0.5 × VDDQ	102	120	138	Ω
	RON120PU	0.5 × VDDQ	102	120	138	Ω
Mismatch between pull-up and pull-down	MMPUPD		-15.00		+15.00	%

Notes:

1. Applies across entire operating temperature range after calibration.
2. RZQ = 240Ω.
3. The tolerance limits are specified after calibration, with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see “Output Driver Temperature and Voltage Sensitivity”.
4. Pull-down and pull-up output driver impedances should be calibrated at 0.5 x VDDQ.
5. Measurement definition for mismatch between pull-up and pull-down,

   MMPUPD: Measure RONPU and RONPD, both at 0.5 × VDDQ:

$$MM_{PUPD} = \frac{R_{ONPU} - R_{ONPD}}{R_{ONNOM}} \times 100$$

For example, with MMPUPD (MAX) = 15% and RONPD = 0.85, RONPU must be less than 1.0

Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen as specified bellow.

Output Driver Sensitivity Definition

Resistor	V_{OUT}	Min	Max	Unit
RONPD	0.5 × VDDQ	85 – (*dRONdT* × |Δ*T*|) – (*dRONdV* × |Δ*V*|)	115 – (*dRONdT* × |Δ*T*|) + (*dRONdV* × |Δ*V*|)	%
RONPU				

Notes:

1. Δ*T* = *T* – *T* (@ calibration). Δ*V* = *V* – *V* (@calibration).

2. dRONdT and dRONdV are not subject to production testing; they are verified by design and characterization.

Output Driver Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
dRONdT	RON temperature sensitivity	0.00	0.75	%/°C
dRONdV	RON voltage sensitivity	0.00	0.20	%/Mv

Output Impedance Characteristics without ZQ Calibration

Output driver impedance is defined by design and characterization as the default setting.

Output Driver DC Electrical Characteristics without ZQ Calibration

R_{Onnom}	Resistor	V_{OUT}	Min	Typ	Max	Unit
34.3Ω	R_{ON34PD}	0.5 × V_{DDQ}	24	34.3	44.6	Ω
	R_{ON34PU}	0.5 × V_{DDQ}	24	34.3	44.6	Ω
40.0Ω	R_{ON40PD}	0.5 × V_{DDQ}	28	40	52	Ω
	R_{ON40PU}	0.5 × V_{DDQ}	28	40	52	Ω
48.0Ω	R_{ON48PD}	0.5 × V_{DDQ}	33.6	48	62.4	Ω
	R_{ON48PU}	0.5 × V_{DDQ}	33.6	48	62.4	Ω
60.0Ω	R_{ON60PD}	0.5 × V_{DDQ}	42	60	78	Ω
	R_{ON60PU}	0.5 × V_{DDQ}	42	60	78	Ω
80.0Ω	R_{ON80PD}	0.5 × V_{DDQ}	56	80	104	Ω
	R_{ON80PU}	0.5 × V_{DDQ}	56	80	104	Ω
120.0Ω	$R_{ON120PD}$	0.5 × V_{DDQ}	84	120	156	Ω
	$R_{ON120PU}$	0.5 × V_{DDQ}	84	120	156	Ω

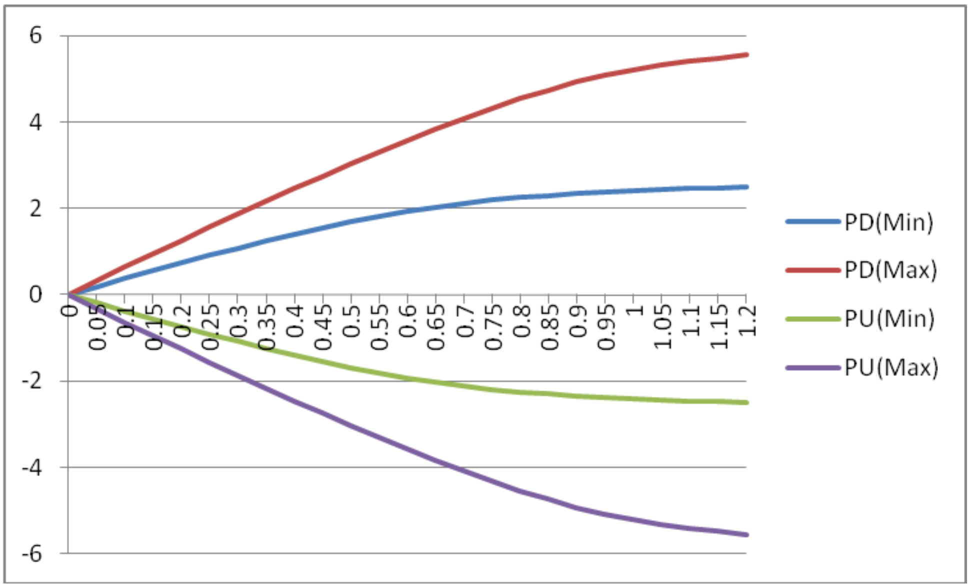
Notes:

1. Applies across entire operating temperature range, without calibration.
2. R_{ZQ} = 240Ω.

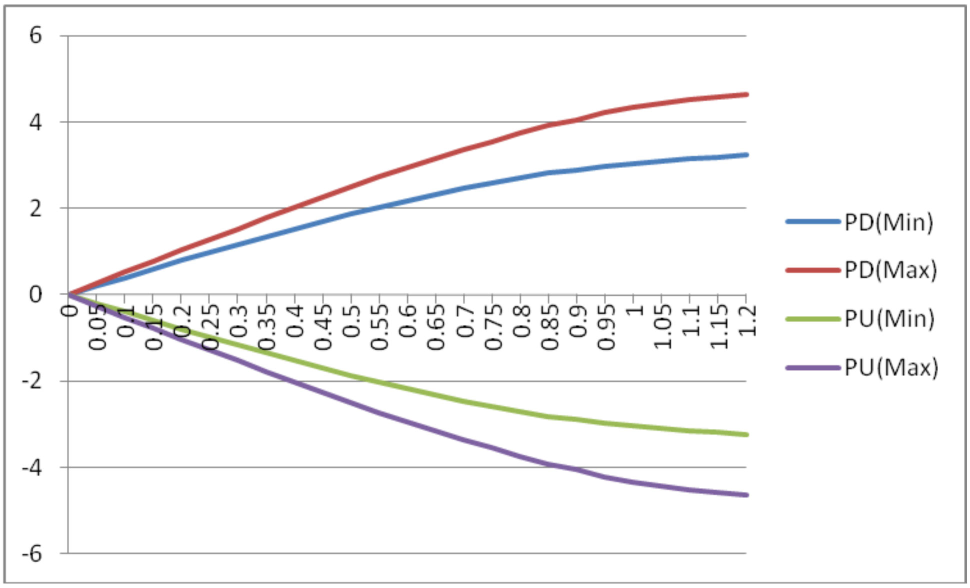
RZQ I-V Curve

RZQ I-V curve

Voltage (V)	RON = 240Ω (RZQ)							
	Pull-Down				Pull-Up			
	Current (Ma) / RON (ohms)				Current (Ma) / RON (ohms)			
	Default Value after ZQRESET		With Calibration		Default Value after ZQRESET		With Calibration	
	Min (Ma)	Max (Ma)	Min (Ma)	Max (Ma)	Min (Ma)	Max (Ma)	Min (Ma)	Max (Ma)
0	0	0	0	0	0	0	0	0
0.05	0.19	0.32	0.21	0.26	–0.19	–0.32	–0.21	–0.26
0.1	0.38	0.64	0.4	0.53	–0.38	–0.64	–0.40	–0.53
0.15	0.56	0.94	0.6	0.78	–0.56	–0.94	–0.60	–0.78
0.2	0.74	1.26	0.79	1.04	–0.74	–1.26	–0.79	–1.04
0.25	0.92	1.57	0.98	1.29	–0.92	–1.57	–0.98	–1.29
0.3	1.08	1.86	1.17	1.53	–1.08	–1.86	–1.17	–1.53
0.35	1.25	2.17	1.35	1.79	–1.25	–2.17	–1.35	–1.79
0.4	1.4	2.46	1.52	2.03	–1.40	–2.46	–1.52	–2.03
0.45	1.54	2.74	1.69	2.26	–1.54	–2.74	–1.69	–2.26
0.5	1.68	3.02	1.86	2.49	–1.68	–3.02	–1.86	–2.49
0.55	1.81	3.3	2.02	2.72	–1.81	–3.30	–2.02	–2.72
0.6	1.92	3.57	2.17	2.94	–1.92	–3.57	–2.17	–2.94
0.65	2.02	3.83	2.32	3.15	–2.02	–3.83	–2.32	–3.15
0.7	2.11	4.08	2.46	3.36	–2.11	–4.08	–2.46	–3.36
0.75	2.19	4.31	2.58	3.55	–2.19	–4.31	–2.58	–3.55
0.8	2.25	4.54	2.7	3.74	–2.25	–4.54	–2.70	–3.74
0.85	2.3	4.74	2.81	3.91	–2.30	–4.74	–2.81	–3.91
0.9	2.34	4.92	2.89	4.05	–2.34	–4.92	–2.89	–4.05
0.95	2.37	5.08	2.97	4.23	–2.37	–5.08	–2.97	–4.23
1	2.41	5.2	3.04	4.33	–2.41	–5.20	–3.04	–4.33
1.05	2.43	5.31	3.09	4.44	–2.43	–5.31	–3.09	–4.44
1.1	2.46	5.41	3.14	4.52	–2.46	–5.41	–3.14	–4.52
1.15	2.48	5.48	3.19	4.59	–2.48	–5.48	–3.19	–4.59
1.2	2.5	5.55	3.23	4.65	–2.50	–5.55	–3.23	–4.65



Output Impedance = 240 Ohms, I-V Curve after ZQRESET



Output Impedance = 240 Ohms, I-V Curve after Calibration

Input / Output Capacitance

Symbol	Parameter	LPDDR2 1066-466		LPDDR2 400-200		Unit
		Min	Max	Min	Max	
C_{CK}	Input capacitance : CK, $\overline{CK}$	1	2	1	2	Pf
C_{DCK}	Input capacitance delta : CK, $\overline{CK}$	0	0.2	0	0.25	Pf
C_{I}	Input capacitance: all other input-only pins	1	2	1	2	Pf
C_{DI}	Input capacitance delta: all other input-only pins	-0.4	0.4	-0.5	0.5	Pf
C_{IO}	Input/output capacitance : DQ, DQS, $\overline{DQS}$, DM	1.25	2.5	1.25	2.5	Pf
C_{DDQS}	Input/output capacitance delta : DQS, $\overline{DQS}$	0	0.25	0	0.3	Pf
C_{DIO}	Input/output capacitance delta : DQ, DM	-0.5	0.5	-0.6	0.6	Pf
C_{ZQ}	Input/output capacitance : ZQ	**0**	**2.5**	**0**	**2.5**	Pf

Notes:

1. This parameter applies to die devices only (does not include package capacitance).
2. This parameter is not subject to production testing. It is verified by design and characterization. The capacitance is measured according to JEP147 (procedure for measuring input capacitance using a vector network analyzer), with VDD1, VDD2, VDDQ, VSS, VSSCA, and VSSQ applied; all other pins are left floating.
3. Absolute value of CCK - $\overline{CCK}$.
4. CI applies to $\overline{CS}$, CKE, and CA[9:0].
5. CDI = CI – 0.5 × (CCK + $\overline{CCK}$)
6. DM loading matches DQ and DQS.
7. MR3 I/O configuration DS OP[3:0] = 0001B (34.3 ohm typical)
8. Absolute value of CDQS and $\overline{CDQS}$.
9. CDIO = CIO – 0.5 × (CDQS + $\overline{CDQS}$) in byte-lane.
10. Maximum external load capacitance on ZQ pin, including packaging, board, pin, resistor, and other LPDDR2 devices: 5Pf.

IDD Specification Parameters and Test Conditions

IDD Measurement Conditions

The following definitions and conditions are used in the IDD measurement tables unless stated otherwise:

- LOW: $V_{IN} \leq V_{IL(DC)}$max
- HIGH: $V_{IN} \geq V_{IH(DC)}$min
- STABLE: Inputs are stable at a HIGH or LOW level
- SWITCHING: See Tables bellow

Switching for CA Input Signal

	CK (Rising) / $\overline{CK}$(Falling)	CK (Falling) / $\overline{CK}$(Rising)	CK (Rising) / $\overline{CK}$(Falling)	CK (Falling) / $\overline{CK}$(Rising)	CK (Rising) / $\overline{CK}$(Falling)	CK (Falling) / $\overline{CK}$(Rising)	CK (Rising) / $\overline{CK}$(Falling)	CK (Falling) / $\overline{CK}$(Rising)
Cycle	**N**		**N+1**		**N+2**		**N+3**	
$\overline{CS}$	HIGH		HIGH		HIGH		HIGH	
CA0	H	L	L	L	L	H	H	H
CA1	H	H	H	L	L	L	L	H
CA2	H	L	L	L	L	H	H	H
CA3	H	H	H	L	L	L	L	H
CA4	H	L	L	L	L	H	H	H
CA5	H	H	H	L	L	L	L	H
CA6	H	L	L	L	L	H	H	H
CA7	H	H	H	L	L	L	L	H
CA8	H	L	L	L	L	H	H	H
CA9	H	H	H	L	L	L	L	H

Notes:

1. $\overline{CS}$ must always be driven HIGH.
2. For each clock cycle, 50% of the CA bus is changing between HIGH and LOW.
3. The noted pattern (N, N + 1, N + 2, N + 3...) is used continuously during IDD measurement for IDD values that require switching on the CA bus.

IDD Measurement Conditions (Continued)

Switching for IDD4R

Clock	CKE	$\overline{CS}$	Clock Cycle Number	Command	CA[2:0]	CA[9:3]	All DQ
Rising	H	L	N	Read_Rising	HLH	LHLHLHL	L
Falling	H	L	N	Read_Falling	LLL	LLLLLLL	L
Rising	H	H	N+1	NOP	LLL	LLLLLLL	H
Falling	H	H	N+1	NOP	HLH	HLHL**LHL**	L
Rising	H	L	N+2	Read_Rising	HLH	HLHLLHL	H
Falling	H	L	N+2	Read_Falling	LLL	HHHHHHH	H
Rising	H	H	N+3	NOP	LLL	HHHHHHH	H
Falling	H	H	N+3	NOP	HLH	LHLHLHL	L

Notes:

1. Data strobe (DQS) is changing between HIGH and LOW with every clock cycle.
2. The noted pattern (N, N + 1...) is used continuously during IDD measurement for IDD4R.

Switching for IDD4W

Clock	CKE	$\overline{CS}$	Clock Cycle Number	Command	CA[2:0]	CA[9:3]	All DQ
Rising	H	L	N	Write_Rising	HLL	LHLHLHL	L
Falling	H	L	N	Write_Falling	LLL	LLLLLLL	L
Rising	H	H	N+1	NOP	LLL	LLLLLLL	H
Falling	H	H	N+1	NOP	HLH	HLHLLHL	L
Rising	H	L	N+2	Write_Rising	HLL	HLHLLHL	H
Falling	H	L	N+2	Write_Falling	LLL	HHHHHHH	H
Rising	H	H	N+3	NOP	LLL	HHHHHHH	H
Falling	H	H	N+3	NOP	HLH	LHLHLHL	L

Notes:

1. Data strobe (DQS) is changing between HIGH and LOW with every clock cycle.
2. Data masking (DM) must always be driven LOW.
3. The noted pattern (N, N + 1...) is used continuously during IDD measurement for IDD4W

IDD Specifications

LPDDR2 IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Notes
Operating one bank active-precharge current (SDRAM): tCK = tCK(avg)min; tRC = tRCmin; CKE is HIGH; $\overline{CS}$ is HIGH between valid commands; CA bus inputs are switching; Data bus inputs are stable	IDD01	VDD1	
	IDD02	VDD2	
	IDD0in	VDDCA,VDDQ	**4**
Idle power-down standby current: tCK = tCK(avg)min; CKE is LOW; $\overline{CS}$ is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable	IDD2P1	VDD1	
	IDD2P2	VDD2	
	IDD2P,in	VDDCA,VDDQ	**4**
Idle power-down standby current with clock stop: CK = LOW, $\overline{CK}$ = HIGH; CKE is LOW; $\overline{CS}$ is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable	IDD2PS1	VDD1	
	IDD2PS2	VDD2	
	IDD2PS,in	VDDCA,VDDQ	**4**
Idle non-power-down standby current: tCK = tCK(avg)min; CKE is HIGH; $\overline{CS}$ is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable	IDD2N1	VDD1	
	IDD2N2	VDD2	
	IDD2N,in	VDDCA,VDDQ	**4**
Active power-down standby current: tCK = tCK(avg)min; CKE is LOW; $\overline{CS}$ is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable	IDD3P1	VDD1	
	IDD3P2	VDD2	
	IDD3P,in	VDDCA,VDDQ	**4**
Active power-down standby current with clock stop: CK = LOW, $\overline{CK}$ = HIGH; CKE is LOW; $\overline{CS}$ is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable	IDD3PS1	VDD1	
	IDD3PSS2	VDD2	
	IDD3PS,in	VDDCA,VDDQ	**4**

IDD Specifications (Continued)

Parameter/Condition	Symbol	Power Supply	Notes
Active non-power-down standby current: Tck = Tck(avg)min; CKE is HIGH; $\overline{CS}$ is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable	IDD3N1	VDD1	
	IDD3N2	VDD2	
	IDD3N,in	VDDCA,VDDQ	**4**
Operating burst READ current: Tck = Tck(avg)min; $\overline{CS}$ is HIGH between valid commands; One bank is active; BL = 4; RL = RL (MIN); CA bus inputs are switching; 50% data change each burst transfer	IDD4R1	VDD1	
	IDD4R2	VDD2	
	IDD4R,in	VDDCA	
	IDD4RQ	VDDQ	**5**
Operating burst WRITE current: Tck = Tck(avg)min; $\overline{CS}$ is HIGH between valid commands; One bank is active; BL = 4; WL = Wlmin; CA bus inputs are switching; 50% data change each burst transfer	IDD4W1	VDD1	
	IDD4W2	VDD2	
	IDD4W,in	VDDCA,VDDQ	**4**
All-bank REFRESH burst current: Tck = Tck(avg)min CKE is HIGH between valid commands; Trc = tRFCabmin; Burst refresh; CA bus inputs are switching; Data bus inputs are stable	IDD51	VDD1	
	IDD52	VDD2	
	IDD5IN	VDDCA,VDDQ	**4**
All-bank REFRESH average current: Tck = Tck(avg)min; CKE is HIGH between valid commands; Trc = Trefi; CA bus inputs are switching; Data bus inputs are stable	IDD5AB1	VDD1	
	IDD5AB2	VDD2	
	IDD5AB,in	VDDCA,VDDQ	**4**
Per-bank REFRESH average current: Tck = Tck(avg)min; CKE is HIGH between valid commands; Trc = Trefi/8; CA bus inputs are switching;Data bus inputs are stable	IDD5PB1	VDD1	**6**
	IDD5PB2	VDD2	**6**
	IDD5PB,in	VDDCA,VDDQ	**4,6**

IDD Specifications (Continued)

Parameter/Condition	Symbol	Power Supply	Notes
Self refresh current (–40°C to +85°C): CK = LOW, $\overline{CK}$ = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x self refresh rate	IDD61	VDD1	**7**
	IDD62	VDD2	**7**
	IDD6IN	VDDCA,VDDQ	**4,7**
Self refresh current (+85°C to +105°C): CK = LOW, $\overline{CK}$ = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable	IDD6ET1	VDD1	**7,8**
	IDD6ET2	VDD2	**7,8**
	IDD6ET,in	VDDCA,VDDQ	**4,7,8**
Deep power-down current: CK = LOW, $\overline{CK}$ = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable	IDD81	VDD1	**8**
	IDD82	VDD2	**8**
	IDD8IN	VDDCA,VDDQ	**4,8**

Notes:

1. Published IDD values are the maximum of the distribution of the arithmetic mean.
2. IDD current specifications are tested after the device is properly initialized.
3. The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh, before going into the extended temperature range.
4. Measured currents are the summation of VDDQ and VDDCA.
5. Guaranteed by design with output load of 5Pf and RON = 40Ohm.
6. Per Bank Refresh only applicable for LPDDR2-S4 devices of 1Gb or higher densities
7. This is the general definition that applies to full-array SELF REFRESH).
8. IDD6ET and IDD8 are typical values, are sampled only, and are not tested.

IDD Specifications and Measurement Conditions

IDD Specifications; V_{DD2}, VDDQ,VDDCA = 1.14~1.30V, V_{DD1} = 1.70~1.95V

Symbol		Supply	Package		Unit	Notes
			SDP	DDP		
IDD0	I_{DD01}	V_{DD1}	15	30	mA	
	I_{DD02}	V_{DD2}	70	140		
	I_{DD0IN}	$V_{DDCA} + V_{DDQ}$	6	12		
IDD2P	I_{DD2P1}	V_{DD1}	600	1200	uA	
	I_{DD2P2}	V_{DD2}	800	1600		
	I_{DD2PIN}	$V_{DDCA} + V_{DDQ}$	50	100		
IDD2PS	I_{DD2PS1}	V_{DD1}	600	1200	uA	
	I_{DD2PS2}	V_{DD2}	800	1600		
	$I_{DD2PSIN}$	$V_{DDCA} + V_{DDQ}$	50	100		
IDD2N	I_{DD2N1}	V_{DD1}	2	4	mA	
	I_{DD2N2}	V_{DD2}	40	80		
	I_{DD2NIN}	$V_{DDCA} + V_{DDQ}$	7	14		
IDD2NS	I_{DD2N1}	V_{DD1}	1.7	3.4	mA	
	I_{DD2N2}	V_{DD2}	40	80		
	I_{DD2SIN}	$V_{DDCA} + V_{DDQ}$	6	12		
IDD3P	I_{DD3P1}	V_{DD1}	1200	2400	uA	
	I_{DD3P2}	V_{DD2}	8	16	mA	
	I_{DD3PIN}	$V_{DDCA} + V_{DDQ}$	150	300	uA	
IDD3PS	I_{DD3PS1}	V_{DD1}	1200	2400	uA	
	I_{DD3PS2}	V_{DD2}	8	16	mA	
	$I_{DD3PSIN}$	$V_{DDCA} + V_{DDQ}$	150	300	uA	
IDD3N	I_{DD3N1}	V_{DD1}	2.5	5	mA	
	I_{DD3N2}	V_{DD2}	30	60		
	I_{DD3NIN}	$V_{DDCA} + V_{DDQ}$	6	12		
IDD3NS	I_{DD3N1}	V_{DD1}	2	4	mA	
	I_{DD3N2}	V_{DD2}	27	54		
	I_{DD3SIN}	$V_{DDCA} + V_{DDQ}$	6	12		
IDD4R	I_{DD4R1}	V_{DD1}	3	6	mA	
	I_{DD4R2}	V_{DD2}	194	388		
	I_{DD4RIN}	V_{DDCA}	25	50		
	I_{DD4RQ}	V_{DDQ}	244	488		
IDD4W	I_{DD4W1}	V_{DD1}	10	20	mA	
	I_{DD4W2}	V_{DD2}	185	370		

	I_{DD4WIN}	V_{DDCA} + V_{DDQ}	25	50		
IDD5	I_{DD51}	V_{DD1}	40	80	mA	
	I_{DD52}	V_{DD2}	150	300		
	I_{DD5IN}	V_{DDCA} + V_{DDQ}	6	12		
IDD5AB	I_{DD5AB1}	V_{DD1}	5	10	mA	
	I_{DD5AB2}	V_{DD2}	18	36		
	$I_{DD5ABIN}$	V_{DDCA} + V_{DDQ}	8	16		
IDD5PB	I_{DD5PB1}	V_{DD1}	5	10	mA	
	I_{DD5PB2}	V_{DD2}	50	100		
	$I_{DD5PBIN}$	V_{DDCA} + V_{DDQ}	8	16		
IDD6	I_{DD61}	V_{DD1}	1000	2000	uA	
	I_{DD62}	V_{DD2}	3200	6400		
	I_{DD6IN}	V_{DDCA} + V_{DDQ}	50	100		
IDD8	I_{DD81}	V_{DD1}	25	50	uA	
	I_{DD82}	V_{DD2}	100	200		
	I_{DD8IN}	V_{DDCA} + V_{DDQ}	100	200		

IDD6 Partial Array Self-refresh current; V_{DD2},V_{DDQ},V_{DDCA} = 1.14~1.30V, V_{DD1} = 1.70~1.95V

PASR	**Supply**	**Package**		**Unit**	**Notes**
		SDP	**DDP**		
Full Array	V_{DD1}	1000	2000	uA	
	V_{DD2}	3200	6400		
	V_{DDCA} + V_{DDQ}	50	100		
1/2 Array	V_{DD1}	950	1900		
	V_{DD2}	2700	5400		
	V_{DDCA} + V_{DDQ}	50	100		
1/4 Array	V_{DD1}	900	1800		
	V_{DD2}	2400	4800		
	V_{DDCA} + V_{DDQ}	50	100		
1/8 Array	V_{DD1}	850	1700		
	V_{DD2}	2000	4000		
	V_{DDCA} + V_{DDQ}	50	100		

Electrical Characteristic and AC Timing

Clock Specification

The specified clock jitter is a random jitter with Gaussian distribution. Input clocks violating minimum or maximum values may result in device malfunction.

Definitions and Calculations

Symbol	Description	Calculation	Notes
ᴛck(avg) and *N*ck	The average clock period across any consecutive 200-cycle window. Each clock period is calculated from rising clock edge to rising clock edge. Unit *ᴛck(avg)* represents the actual clock average *ᴛck(avg)* of the input clock under operation. Unit *N*ck represents one clock cycle of the input clock, counting from actual clock edge to actual clock edge. *ᴛck(avg)* can change no more than ±1% within a 100-clock-cycle window, provided that all jitter and timing specifications are met.	$t_{CK(avg)} = \left[\sum_{j=1}^{N} t_{CK_j}\right] / N$ Where $N = 200$	
ᴛck(abs)	The absolute clock period, as measured from one rising clock edge to the next consecutive rising clock edge.		
ᴛch(avg)	The average HIGH pulse width, as calculated across any 200 consecutive HIGH pulses.	$t_{CH(avg)} = \left[\sum_{j=1}^{N} t_{CH_j}\right] / (N \times t_{CK(avg)})$ Where $N = 200$	
ᴛcl(avg)	The average LOW pulse width, as calculated across any 200 consecutive LOW pulses.	$t_{CL(avg)} = \left[\sum_{j=1}^{N} t_{CL_j}\right] / (N \times t_{CK(avg)})$ Where $N = 200$	
ᴛjit(per)	The single-period jitter defined as the largest deviation of any signal ᴛck from *ᴛck(avg).*	$t_{JIT(per)} = \text{min/max of } \left\{t_{CK_i} - t_{CK(avg)}\right\}$ Where $i = 1 \text{ to } 200$	
ᴛjit(per),act	The actual clock jitter for a given system.		
ᴛjit(per),allowed	The specified clock period jitter allowance.		
ᴛjit(cc)	The absolute difference in clock periods between two consecutive clock cycles. *ᴛjit(cc)* defines the cycle-to-cycle jitter.	$t_{JIT(cc)} = \text{max of } \left\{t_{CK_{i+1}} - t_{CK_i}\right\}$	

Symbol	Description	Calculation	Notes
terr(nper)	The cumulative error across *n* multiple consecutive cycles from *tck(avg)*.	$t_{ERR(nper)} = \left(\sum_{j=i}^{i+n-1} t_{CK_j} \right) - (n \times t_{CK(avg)})$	
terr(nper),act	The actual cumulative error over *n* cycles for a given system.		
terr(nper),allowed	The specified cumulative error allowance over *n* cycles.		
terr(nper),min	The minimum *terr(nper).*	$t_{ERR(nper),min} = (1 + 0.68LN(n)) \times t_{JIT(per),min}$	
terr(nper),max	The maximum *terr(nper).*	$t_{ERR(nper),max} = (1 + 0.68LN(n)) \times t_{JIT(per),max}$	
tjit(duty)	Defined with tch jitter and tcl jitter. tch jitter is the largest deviation of any single tch from *tch(avg).* tcl jitter is the largest deviation of any single tcl from *tcl(avg).*	$t_{JIT(duty)} = min/max\ of\ [t_{JIT(CH)}, t_{JIT(CL)}]$ *Where:* $t_{JIT(CH)} = [t_{CH_i} - t_{CH(avg)}\ where\ i = 1\ to\ 200]$ $t_{JIT(CL)} = [t_{CH_i} - t_{CH(avg)}\ where\ i = 1\ to\ 200]$	

Tck(abs), Tch(abs) and Tcl(abs)

These parameters are specified per their average values, however, it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

Symbol	Parameter	Minimum	Unit
tck(abs)	Absolute clock period	*tck(avg),min* + *tjit(per),min*	**ps**
tch(abs)	Absolute clock HIGH pulse width	*tch(avg),min* + *tjit(duty),min/ tck(avg)min*	*tck(avg)*
tcl(abs)	Absolute clock LOW pulse width	*tcl(avg),min* + *tjit(duty),min / tck(avg)min*	*tck(avg)*

Notes:

1. *tck(avg),min* is expressed in ps for this table.
2. *tjit(duty),min* is a negative value.

Period Clock Jitter

LPDDR2 devices can tolerate some clock period jitter without core timing parameter derating. This section describes device timing requirements with clock period jitter (Tjit(per)) in excess of the values found in the AC timing table. Calculating cycle time derating and clock cycle derating are also described.

Clock Period Jitter Effects on Core Timing Parameters

Core timing parameters (Trcd, Trp, Trtp, Twr, Twra, Twtr, Trc, Tras, Trrd, Tfaw) extend across multiple clock cycles. Period clock jitter impacts these parameters when measured in numbers of clock cycles. Within the specification limits, the device is characterized and verified to support tnPARAM = RU[Tparam / Tck(avg)]. During device operation where clock jitter is outside specification limits, the number of clocks or Tck(avg), may need to be increased based on the values for each core timing parameter.

Cycle Time Derating for Core Timing Parameters

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period(Tck(avg)) and actual cumulative period error (Terr(tnPARAM), act) in excess of the allowed cumulative period error (Terr(tnPARAM),allowed) , the equation below calculates the amount of cycle time de-rating(in ns) required if the equation results in a positive value for a core timing parameter(Tcore). A cycle time de-rating analysis should be conducted for each core timing parameter. The amount of cycle time de-rating required is the maximum of the cycle time de-rating determined for each individual core timing parameter.

$$CycleTimeDerating = max\left\{\left[\frac{{}^{t}PARAM + {}^{t}ERR({}^{t}nPARAM),act - {}^{t}ERR({}^{t}nPARAM),allowed}{{}^{t}nPARAM} - {}^{t}CK(avg)\right], 0\right\}$$

Clock Cycle Derating for Core Timing Parameters

For each core timing parameter and a given number of clocks (tnPARAM), clock cycle derating should be specified with Tjit(per). For a given number of clocks (tnPARAM), for each core parameter, average clock period(Tck(avg)) and actual cumulative period error (Terr(tnPARAM),act) in excess of the allowed cumulative period error (Terr(tnPARAM),allowed), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter (Tcore), A clock cycle de-rating analysis should be conducted for each core timing parameter.

$$ClockCycleDerating = RU\left\{\frac{{}^{t}PARAM + {}^{t}ERR({}^{t}nPARAM),act - {}^{t}ERR({}^{t}nPARAM),allowed}{{}^{t}CK(avg)}\right\} - {}^{t}nPARAM$$

Clock Jitter Effects on Command/Address Timing Parameters

Command/address timing parameters (Tis, Tih, Tiscke, Tihcke, tISb, tIHb, tISCKEb, tIHCKEb) are measured from a command/address signal (CKE, CS, or CA[9:0]) transition edge to its respective clock signal (CK, $\overline{CK}$) crossing. The specification values are not affected by the Tjit(per) applied, as the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

Clock Jitter Effects on READ Timing Parameters

Trpre

When the device is operated with input clock jitter, Trpre must be derated by the actual period jitter(Tjit(per),act,max) of the input clock that exceeds the allowed period jitter(Tjit(per),allowed,max.). Output de-ratings are relative to the input clock.

$$^{t}RPRE(min,derated) = 0.9 - \left(\frac{^{t}JIT(per),act,max - {}^{t}JIT(per),allowed,max}{^{t}CK(avg)} \right)$$

For example, if the measured jitter into a LPDDR2-800 device has Tck(avg) = 2500ps, Tjit(per),act,min = –172ps, and JIT(per),act,max = +193ps, then Trpre,min, derated = 0.9 – (Tjit(per), act,max – Tjit(per), allowed,max)/Tck(avg) = 0.9 – (193 – 100)/2500 = 0.8628 Tck(avg).

Tlz(DQ), Thz(DQ), Tdqsck, Tlz(DQS), Thz(DQS)

These parameters are measured from a specific clock edge to a data signal transition (DMn or DQm, where: n = 0, 1, 2, or 3; and m = DQ[31:0]), and specified timings must be met with respect to that clock edge. Therefore, they are not affected by Tjit(per).

Tqsh, Tqsl

These parameters are affected by duty cycle jitter, represented by Tch(abs)min and Tcl(abs)min. Therefore Tqsh(abs)min and Tqsl(abs)min can be specified with Tch(abs)min and Tcl(abs)min. Tqsh(abs)min = Tch(abs)min – 0.05, Tqsl(abs)min = Tcl(abs)min – 0.05. These parameters determine the absolute data-valid window at the device pin. The absolute minimum data-valid window @ the device pin = min [(Tqsh(abs)min × Tck(avg)min – tDQSQmax – tQHSmax), (Tqsl(abs)min × Tck(avg)min – tDQSQmax – tQHSmax)]. This minimum data-valid window must be met at the target frequency regardless of clock jitter.

Trpst

Trpst is affected by duty cycle jitter, represented by Tcl(abs). Therefore, Trpst(abs)min can be specified by Tcl(abs)min. Trpst(abs)min = Tcl(abs)min – 0.05 = Tqsl(abs)min.

Clock Jitter Effects on WRITE Timing Parameters

Tds, Tdh

These parameters are measured from a data signal (DMn or DQm, where n = 0, 1, 2, 3; and m = DQ[31:0]) transition edge to its respective data strobe signal (DQSn, $\overline{\text{DQSn}}$: n = 0,1,2,3) crossing. The specification values are not affected by the amount of Tjit(per) applied, as the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

Tdss, Tdsh

These parameters are measured from a data strobe signal (DQSx, $\overline{\text{DQSx}}$) crossing to its respective clock signal (CK, $\overline{\text{CK}}$) crossing. The specification values are not affected by the amount of Tjit(per)) applied, as the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

Tdqss

This parameter is measured from the clock signal (CK, $\overline{\text{CK}}$) crossing to the first latching data strobe signal (DQSx, $\overline{\text{DQSx}}$) crossing. When the device is operated with input clock jitter, this parameter must be derated by the actual period jitter (Tjit(per),act) of the input clock in excess of the allowed period jitter (Tjit(per),allowed).

$$^{t}DQSS(min,derated) = 0.75 - \left(\frac{^{t}JIT(per),act,min - {}^{t}JIT(per),allowed,\ min}{^{t}CK(avg)}\right)$$

$$^{t}DQSS(max,derated) = 1.25 - \left(\frac{^{t}JIT(per),act,max - {}^{t}JIT(per),allowed,\ max}{^{t}CK(avg)}\right)$$

For example, if the measured jitter into an LPDDR2-800 device has Tck(avg) = 2500ps, Tjit(per),act,min = -172ps, and Tjit(per),act,max = +193ps, then:

Tdqss,(min,derated)

= 0.75 – (Tjit(per),act,min – Tjit(per),allowed,min)/Tck(avg) = 0.75 – (-172 + 100)/2500 = 0.7788 Tck(avg),

And

Tdqss,(max,derated)

= 1.25 – (Tjit(per),act,max – Tjit(per),allowed,max)/Tck(avg) = 1.25 – (193 – 100)/2500 = 1.2128 Tck(avg).

REFRESH Requirements by Device Density

LPDDR2-S4 Refresh Requirement Parameters (per density)

Symbol	Parameter	4Gb	8Gb	Unit
	Number of banks	8		
Trefw	Refresh window: TCASE ≤ 85°	32		ms
Trefw	Refresh window: 85°C < TCASE ≤ 105°C	8		ms
R	Required number of REFRESH commands (MIN)	8192	8192	
Trefi	Average time between REFRESH commands (for reference only) TCASE ≤ 85°C	3.9	3.9	us
tREFIpb		0.4875	0.4875	us
tRFCab	Refresh cycle time	130	210	ns
tRFCpb	Per-bank REFRESH cycle time	60	90	ns
Trefbw	Burst REFRESH window = 4 × 8 × tRFCab	4.16	6.72	us

Electrical Characteristics and Recommended AC Timing

V_{DD2},V_{DDQ},V_{DDCA} = 1.14~1.30V, V_{DD1} = 1.70~1.95V

Symbol	Parameter	Min/ Max	Min ^{t}CK	Speed Grade			Unit
				1066	800	667	
Clock parameters							
f	Frequency	max		533	400	333	MHz
^{t}CK	Clock cycle time	min		1.875	2.5	3	ns
		max		100			ns
^{t}CH	CK high-level width	min		0.45			^{t}CK
		max		0.55			^{t}CK
^{t}CL	CK low-level width	min		0.45			^{t}CK
		max		0.55			^{t}CK
^{t}HP	Half-clock period	=		min(^{t}CH, ^{t}CL)			^{t}CK
^{t}CK(avg)	Average Clock period	min		1.875	2.5	3	^{t}CK(avg)
		max		100			
^{t}CH(avg)	Average HIGH pulse width	min		0.45			^{t}CK(avg)
		max		0.55			

Symbol	Parameter	Min/ Max	Min ^{t}CK	Speed Grade			Unit
				1066	800	667	
^{t}CL(avg)	Average LOW pulse width	min		0.45			^{t}CK(avg)
		max		0.55			
tck(abs)	Absolute clock period	min		*tck(avg)* MIN ± *tjit(per)* MIN			ps
tch(abs)	Absolute clock HIGH pulse width	min		0.43			^{t}CK(avg)
tcl(abs)	Absolute clock LOW pulse width	min		0.43			^{t}CK(avg)
tjit(per), allowed	Clock period jitter (with supported jitter)	min		-90	-100	-110	ps
		max		-90	-100	-110	ps
terr(2per), allowed	Cumulative errors across 2 cycles	min		-132	-147	-162	ps
		max		132	147	162	ps
terr(3per), allowed	Cumulative errors across 3 cycles	min		-157	-175	-192	ps
		max		157	175	192	ps
terr(4per), allowed	Cumulative errors across 4 cycles	min		-175	-194	-214	ps
		max		175	194	214	ps
terr(5per), allowed	Cumulative errors across 5 cycles	min		-188	-209	-230	ps
		max		188	209	230	ps
terr(6per), allowed	Cumulative errors across 6 cycles	min		-200	-222	-244	ps
		max		200	222	244	ps
terr(7per), allowed	Cumulative errors across 7 cycles	min		-209	-232	-256	ps
		max		209	232	256	ps
terr(8per), allowed	Cumulative errors across 8 cycles	min		-217	-241	-266	ps
		max		217	241	266	ps
terr(9per), allowed	Cumulative errors across 9 cycles	min		-224	-249	-274	ps
		max		224	249	274	ps
terr(10per), allowed	Cumulative errors across 10 cycles	min		-231	-257	-282	ps
		max		231	257	282	ps
terr(11per), allowed	Cumulative errors across 11 cycles	min		-237	-263	-289	ps
		max		237	263	289	ps
terr(12per), allowed	Cumulative errors across 12 cycles	min		-242	-269	-296	ps
		max		242	269	296	ps
terr(nper), allowed	Cumulative errors across *n* = 13, 14, 15…, 49, 50 cycles	min		*terr(nper),allowed* MIN = (1 + 0.68ln(n)) × *tjit(per),allowed* MIN			ps
		max		*terr (nper), allowed* MAX=(1 + 0.68ln(n)) × *tjit(per),allowed* MAX			ps

Symbol	Parameter	Min/ Max	Min ^{t}CK	Speed Grade			Unit
				1066	800	667	
ZQ calibration parameters							
^{t}Zqinit	Calibration initialization Time	min		1			us
^{t}ZQCL	Long (Full) Calibration Time	min		360			ns
^{t}ZQCS	Short Calibration Time	min		90			ns
^{t}Zqreset	Calibration Reset Time	Min	3	50			ns
Read parameters							
^{t}DQSCK	DQS output access time from CK, /CK	Min		2500			ps
		Max		5500			ps
^{t}DQSCKDS	DQSCK Delta Short	Max		330	450	540	ps
^{t}DQSCKDM	DQSCK Delta Medium	Max		680	900	1050	ps
^{t}DQSCKDL	DQSCK Long	Max		920	1200	1400	ps
^{t}DQSQ	DQS-DQ skew, DQS to last DQ valid, per group, per access	Max		200	240	280	ps
^{t}QHS	Data Hold Skew Factor	Max		230	280	340	ps
^{t}QSH	DQS output HIGH pulse width	Min		Tch – 0.05			^{t}CK
^{t}QSL	DQS output LOW pulse width	Min		Tcl – 0.05			^{t}CK
^{t}QHP	Data half period	Min		MIN (Tqsh, Tqsl)			^{t}CK
^{t}QH	DQ-DQS hold, DQS to first DQ to go non-valid, per access	Min		^{t}HP – ^{t}QHS			ps
^{t}RPRE	READ Preamble	Min		0.9			^{t}CK
^{t}RPST	READ postamble	Min		Tcl – 0.05			^{t}CK
^{t}LZ(DQS)	DQS Low-Z from CK	Min		^{t}DQSCK$_{min}$ – 300			ps
^{t}LZ(DQ)	DQ Low-Z from CK	Min		Tdqsck(MIN) – (1.4 × Tqhs(MAX))			ps
^{t}HZ(DQS)	DQS High-Z from CK	Max		^{t}DQSCK$_{max}$ – 100			ps
^{t}HZ(DQ)	DQ High-Z from CK	Max		Tdqsck(MAX) + (1.4 × Tdqsq(MAX))			ps
Write parameters							
^{t}DH	DQ and DM input hold time (V_{REF} based)	Min		210	270	350	ps
^{t}DS	DQ and DM input setup time (V_{REF} based)	Min		210	270	350	ps
^{t}DIPW	DQ and DM input pulse width	Min		0.35			^{t}CK
Tdqss	Write command to 1st DQS latching transition	Min		0.75			^{t}CK
		Max		1.25			^{t}CK
Tdqsh	DQS input high-level width	Min		0.4			^{t}CK
Tdqsl	DQS input low-level width	Min		0.4			^{t}CK
Tdss	DQS falling edge to CK setup time	Min		0.2			^{t}CK

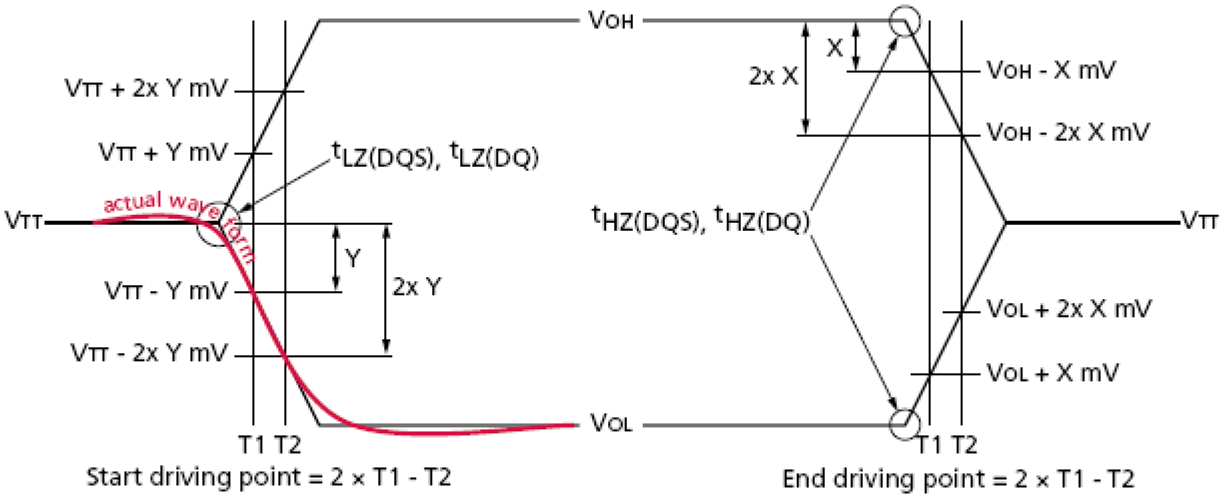
Symbol	Parameter	Min/ Max	Min ^{t}CK	Speed Grade			Unit
				1066	800	667	
Tdsh	DQS falling edge hold time from CK	Min		0.2			^{t}CK
Twpst	Write postamble	Min		0.4			^{t}CK
Twpre	Write preamble	Min		0.35			^{t}CK
CKE input parameters							
^{t}CKE	CKE min. pulse width (high and low)	Min	3	3			^{t}CK
^{t}ISCKE	CKE input set-up time	Min		0.25			^{t}CK
^{t}IHCKE	CKE input hold time	Min		0.25			^{t}CK
Command / Address Input parameters							
^{t}IH	Address and Control input hold time	Min		220	290	370	ps
^{t}IS	Address and Control input setup time	Min		220	290	370	ps
^{t}IPW	Address and Control input pulse width	Min		0.4			^{t}CK
Mode register parameters							
^{t}MRR	MODE Register Read command period	Min	2	2			^{t}CK
^{t}MRW	MODE Register Write command period	Min	5	5			^{t}CK
SDRAM core parameters							
RL	Read Latency	Min	3	8	6	5	^{t}CK
WL	Write Latency	Min	1	4	3	2	^{t}CK
Tckesr	CKE minimum pulse width during SELF REFRESH (low pulse width during SELF REFRESH)	Min	3	15			ns
^{t}XSR	Exit SELF REFRESH to first valid command (min)	min	2	^{t}RFC$_{AB}$ +10			ns
^{t}XP	Exit power-down mode to first valid command	min	2	7.5			ns
^{t}DPD	Minimum Deep Power-Down time	min	-	500			us
^{t}FAW	Four-Bank Activate Window	min	8	50			ns
^{t}WTR	Internal WRITE to READ command delay	min	2	7.5			ns
^{t}RC	ACTIVE to ACTIVE command period	min		^{t}RAS + ^{t}RP$_{AB}$ (with all-bank Precharge) ^{t}RAS + ^{t}RP$_{PB}$ (with per-bank Precharge)			ns
^{t}CCD	CAS-to-CAS delay	min	2	2			^{t}CK
^{t}RTP	Internal READ to PRECHARGE command delay	min	2	7.5			ns
^{t}RCD	RAS-to-CAS delay	min	3	18			ns
^{t}RAS	Row Active Time	min	3	42			ns
		max	-	70			us
^{t}WR	Write recovery time	min	3	15			ns

Symbol	Parameter	Min/ Max	Min ^{t}CK	Speed Grade			Unit
				1066	800	667	
$^{t}RP_{PB}$	PRECHARGE command period (single bank)	min	3	18			ns
$^{t}RP_{PAB}$	PRECHARGE command period (all banks – 8bnak)	min	3	21			ns
^{t}RRD	ACTIVE *bank-a* to ACTIVE *bank-b* command	min	2	10			ns
Temperature Derating							
tdqsck (derated)	tdqsck derating	max		5620	6000	6000	ps
trcd (derated)	Core timing temperature derating	min		trcd + 1.875			ns
trc (derated)		min		trc + 1.875			ns
tras (derated)		min		tras + 1.875			ns
trp (derated)		min		trp + 1.875			ns
trrd (derated)		min		trrd + 1.875			ns
Boot parameters (10MHz ~ 55MHz)							
^{t}CKb	Clock cycle time	min		18			ns
		max		100			ns
$^{t}ISCKEb$	CKE input setup time	min		2.5			ns
$^{t}IHCKEb$	CKE input hold time	min		2.5			ns
^{t}ISb	Input setup time	min		1150			ps
^{t}IHb	Input hold time	min		1150			ps
$^{t}DQSCKb$	Access window of DQS from CK, /CK	min		2.0			ns
		max		10.0			ns
$^{t}DQSQb$	DQS-DQ skew	max		1.2			ns
$^{t}QHSb$	Data hold skew factor	max		1.2			ns

Notes:

1. Frequency values are for reference only. Clock cycle time (tck) is used to determine device capabilities.
2. All AC timings assume an input slew rate of 1 V/ns.
3. READ, WRITE, and input setup and hold values are referenced to V_{REF}.
4. tdqsckds is the absolute value of the difference between any two tdqsck measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window. tdqsckds is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.
5. tdqsckdm is the absolute value of the difference between any two tdqsck measurements (in a byte lane) within a 1.6µs rolling window. tdqsckdm is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter.
6. tdqsckdl is the absolute value of the difference between any two tdqsck measurements (in a byte lane) within a 32ms rolling window. tdqsckdl is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter.
7. For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition

threshold (V_{TT}). tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Figure shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.



Data Out measurement reference points

The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS, $\overline{DQS}$.

8. Measured from the point when DQS, $\overline{DQS}$ begins driving the signal to the point when DQS, $\overline{DQS}$ begins driving the first rising strobe edge.
9. Measured from the last falling strobe edge of DQS, $\overline{DQS}$ to the point when DQS, $\overline{DQS}$ finishes driving the signal.
10. CKE input setup time is measured from CKE reaching a HIGH/LOW voltage level to CK, $\overline{CK}$ crossing.
11. CKE input hold time is measured from CK, $\overline{CK}$ crossing to CKE reaching a HIGH/LOW voltage level.
12. Input set-up/hold time for signal (CA[9:0], $\overline{CS}$).
13. To ensure device operation before the device is configured, a number of AC boot-timing parameters are defined in this table. Boot parameter symbols have the letter b appended (for example, tCK during boot is tCKb).
14. The LPDDR device will set some mode register default values upon receiving a RESET (MRW) command as specified in “Mode Register Definition”.
15. The output skew parameters are measured with default output impedance settings using the reference load.
16. The minimum tCK column applies only when tCK is greater than 6ns.
17. Timing derating applies for operation at 85°C to 105°C when the requirement to derate is indicated by mode register 4 op-codes.

CA and $\overline{CS}$ Setup, Hold, and Derating

The For all input signals (CA and $\overline{CS}$), the total required setup time (Tis) and hold time (Tih) is calculated by adding the data sheet Tis (base) and Tih (base) values to the ΔtIS and ΔtIH derating values, respectively. Example: Tis (total setup time) = Tis(base) + ΔtIS.

Setup (Tis) typical slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of VIH(AC)min. The setup (Tis) typical slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of VIL(AC)max. If the actual signal is always earlier than the typical slew rate line between the shaded VREF(DC)-to-(AC) region, use the typical slew rate for the derating value. If the actual signal is later than the typical slew rate line anywhere between the shaded VREF(DC)-to-AC region, the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for the derating value.

The hold (Tih) typical slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VREF(DC). The hold (Tih) typical slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VREF(DC). If the actual signal is always later than the typical slew rate line between the shaded DC-to-VREF(DC) region, use the typical slew rate for the derating value. If the actual signal is earlier than the typical slew rate line anywhere between the shaded DC-to-VREF(DC) region, the slew rate of a tangent line to the actual signal from the DC level to VREF(DC) level is used for the derating value.

For a valid transition, the input signal must remain above or below VIH/VIL(AC) for a specified time, Tvac. For slow slew rates the total setup time could be a negative value (that is, a valid input signal will not have reached VIH/VIL(AC) at the time of the rising clock transition). A valid input signal is still required to complete the transition and reach VIH/VIL(AC).

For slew rates between the values listed, the derating values are obtained using linear interpolation. Slew rate values are not typically subject to production testing. They are verified by design and characterization.

CA and $\overline{CS}$ Setup and Hold Base Values (> 400 MHz, 1 V/ns slew rate)

Parameter	**Data Rate**				**Reference**
	1066	**800**	**667**	**533**	
Tis (base)	0	70	150	240	$V_{IH}/V_{IL(AC)} = V_{REF(DC)}$ ± 220Mv
Tih (base)	90	160	240	330	$V_{IH}/V_{IL(DC)} = V_{REF(DC)}$ ± 130Mv

Notes: AC/DC referenced for 1 V/ns CA and $\overline{CS}$ slew rate and 2 V/ns differential CK, $\overline{CK}$ slew rate.

CA and $\overline{CS}$ Setup, Hold, and Derating (Continued)

Derating Values for AC/DC-based Tis/Tih (AC220) – ΔtIS, ΔtIH derating in [ps], AC/DC-based

		CK, CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH
CA, CS# slew rate V/ns	2.0	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

Notes: Cell contents shaded in green are defined as “not supported.”.

Derating Values for AC/DC-based Tis/Tih (AC300) – ΔtIS, ΔtIH derating in [ps], AC/DC-based

		CK, CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH
CA, CS# slew rate V/ns	2.0	150	100	150	100	150	100										
	1.5	100	67	100	67	100	67	116	83								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-4	-8	-4	-8	12	8	28	24	44	40				
	0.8					-12	-20	4	-4	20	12	36	28	52	48		
	0.7							-3	-18	13	-2	29	14	45	34	61	66
	0.6									2	-21	18	-5	34	15	50	47
	0.5											-12	-32	4	-12	20	20
	0.4													-35	-40	-11	-8

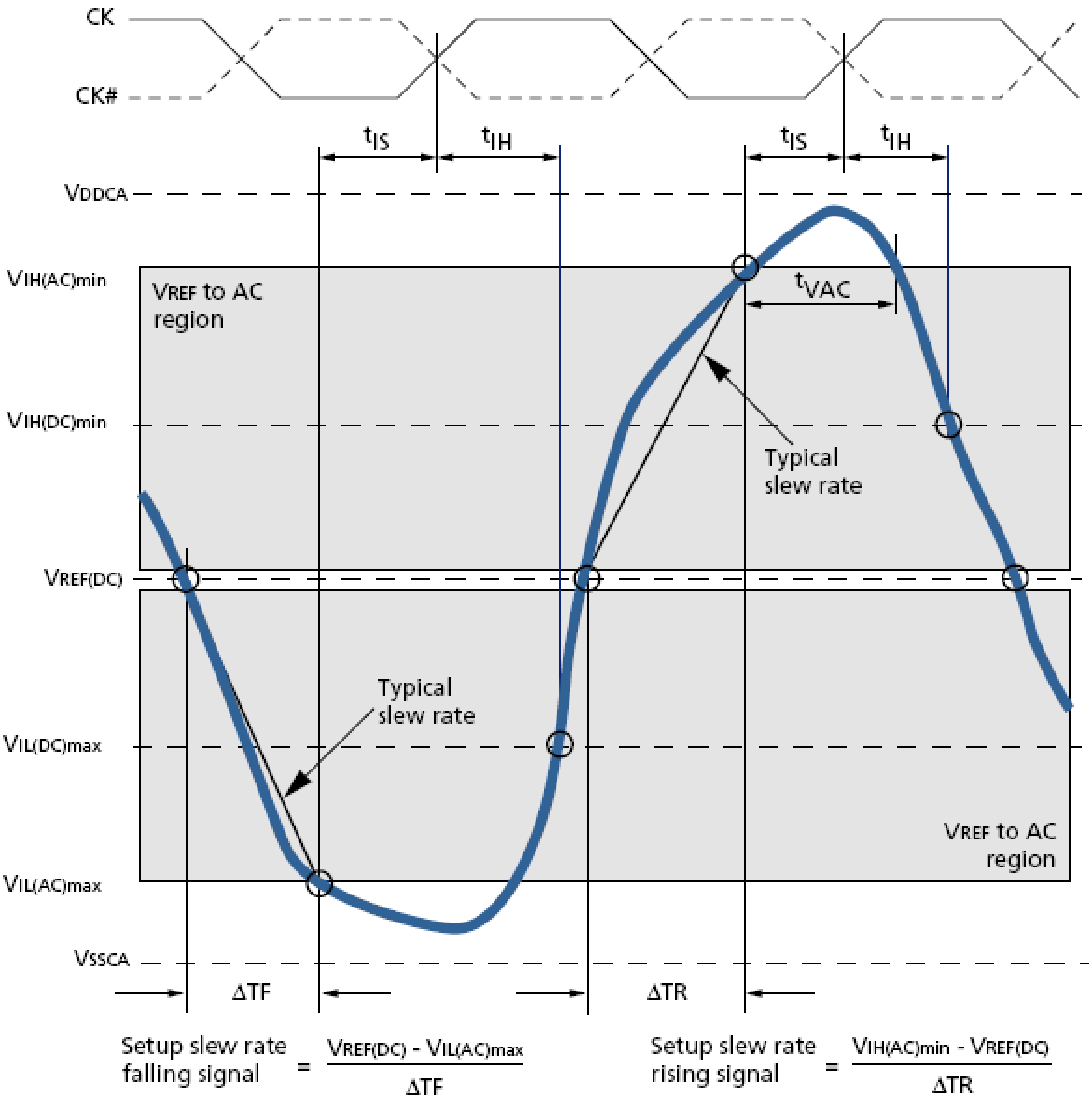
Notes: Cell contents shaded in green are defined as “not supported.”

Required Time for Valid Transition with Tvac Above VIH(AC) and Below VIL(AC)

Slew Rate (V/ns)	Tvac at 300Mv (ps)		Tvac at 220Mv (ps)	
	Min	Max	Min	Max
>2.0	75	–	175	–
2	57	–	170	–
1.5	50	–	167	–
1	38	–	163	–
0.9	34	–	162	–
0.8	29	–	161	–
0.7	22	–	159	–
0.6	13	–	155	–
0.5	0	–	150	–

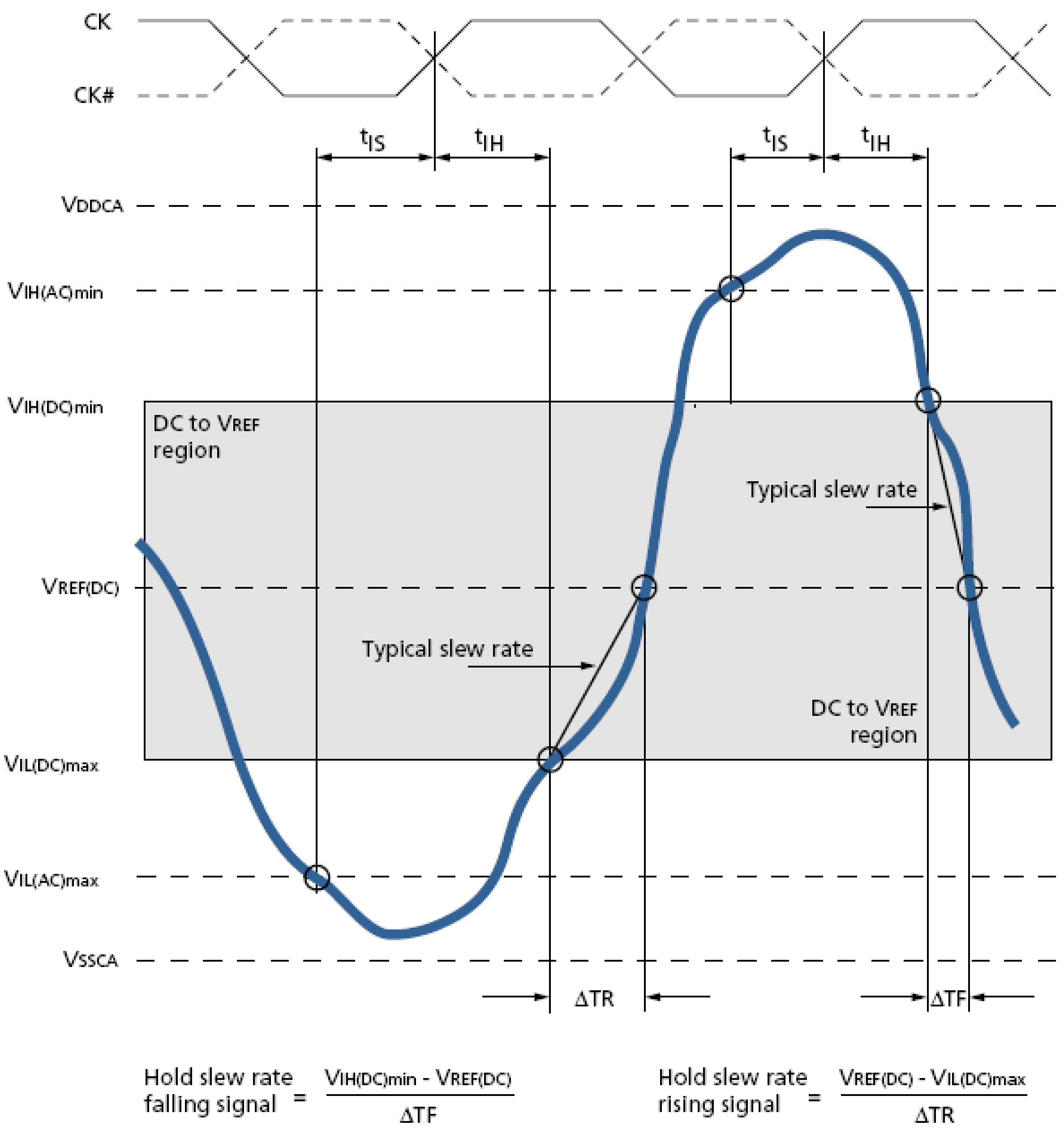
<0.5	0	–	150	–

CA and $\overline{CS}$ Setup, Hold, and Derating (Continued)



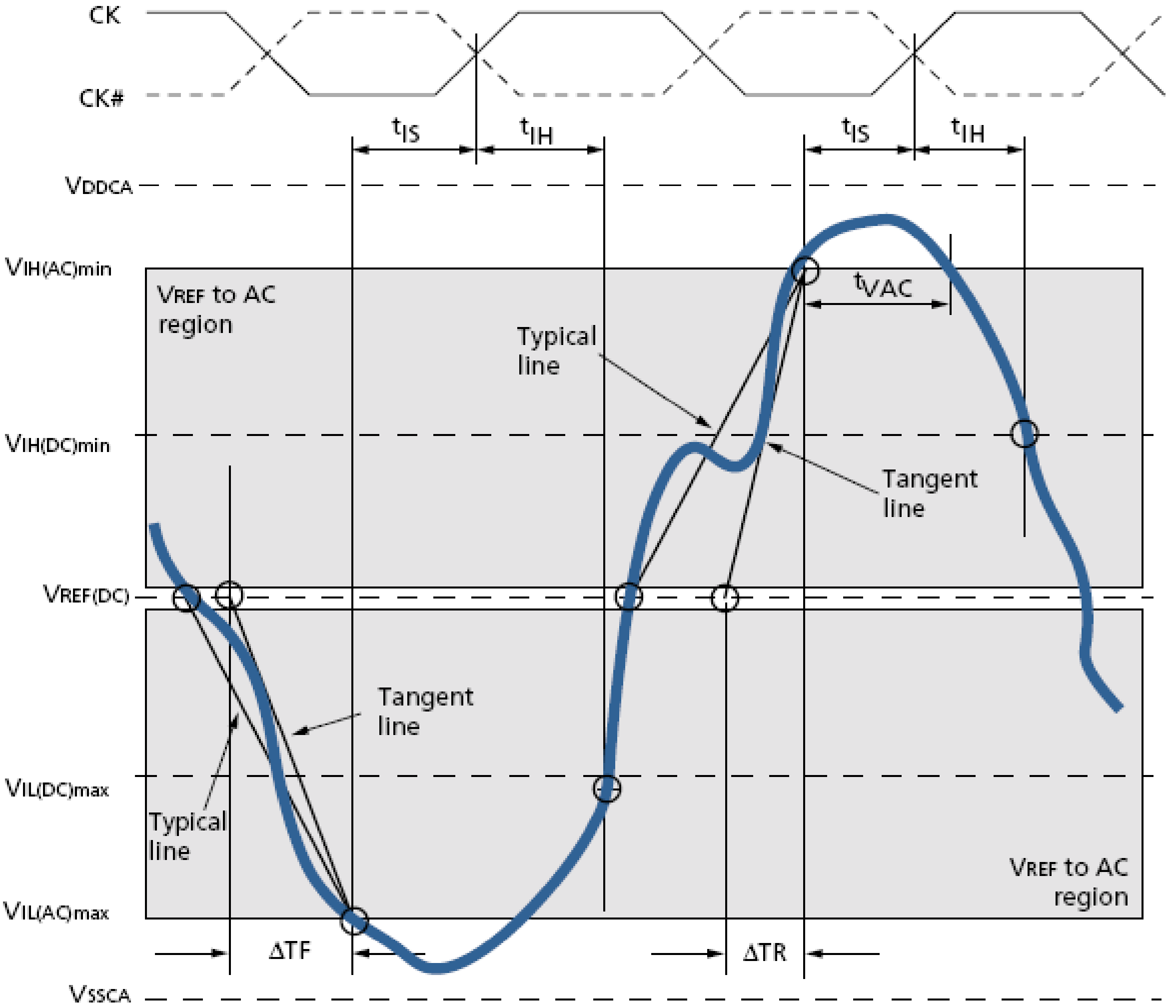
Typical Slew Rate and Tvac: Tis for CA and $\overline{CS}$ Relative to Clock

CA and $\overline{CS}$ Setup Hold, and Derating (Continued)



Typical Slew Rate: Tih for CA and $\overline{CS}$ Relative to Clock

CA and $\overline{\text{CS}}$ Setup Hold, and Derating (Continued)

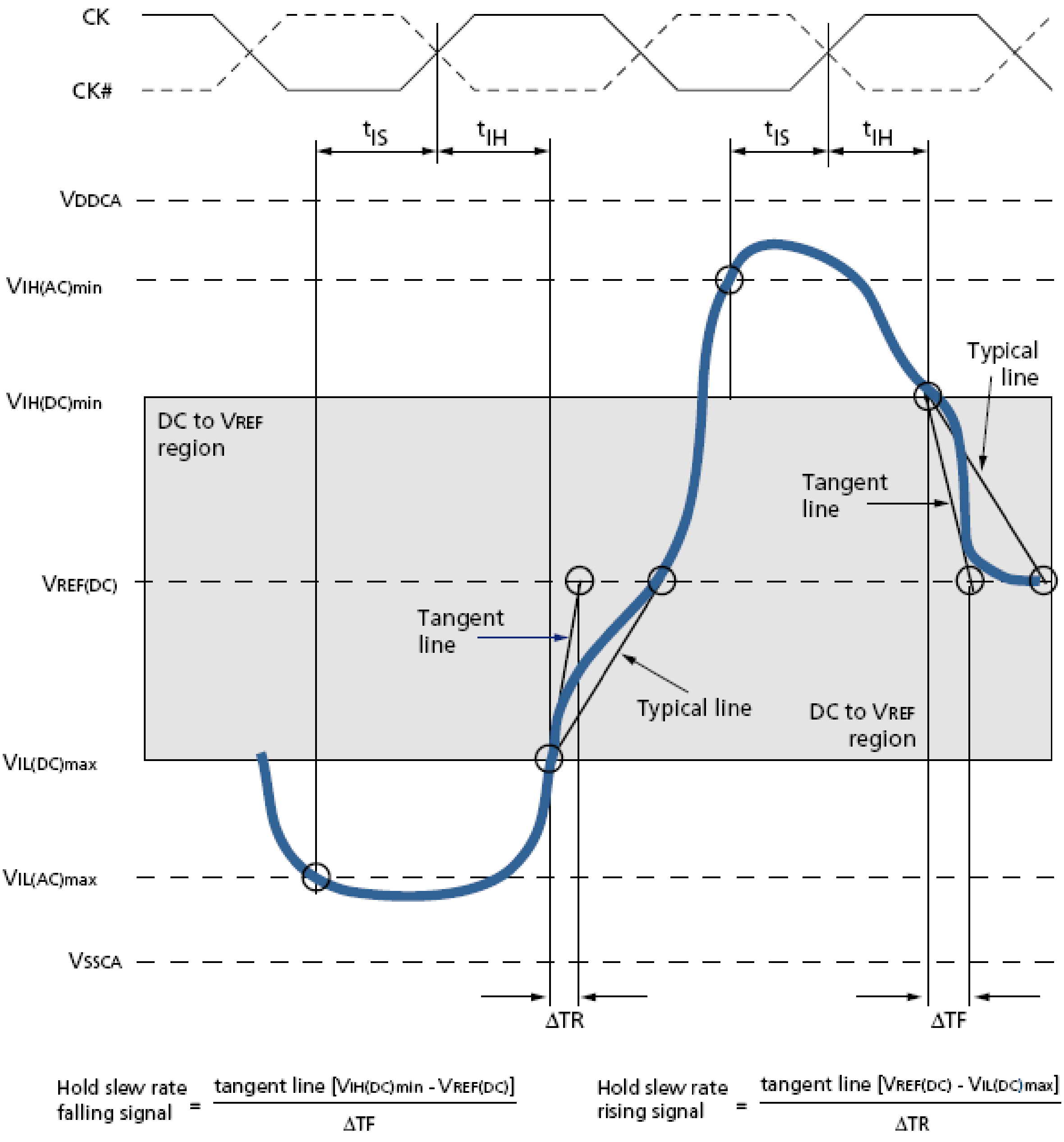


$$\text{Setup slew rate falling signal} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(AC)max}]}{\Delta TF}$$

$$\text{Setup slew rate rising signal} = \frac{\text{tangent line } [V_{IH(AC)min} - V_{REF(DC)}]}{\Delta TR}$$

Tangent Line: Tis for CA and $\overline{\text{CS}}$ Relative to Clock

CA and $\overline{CS}$ Setup Hold, and Derating (Continued)



Tangent Line: Tih for CA and $\overline{CS}$ Relative to Clock

Data Setup, Hold, and Slew Rate Derating

For all input signals (DQ, DM) calculate the total required setup time (Tds) and hold time (Tdh) by adding the data sheet Tds(base) and Tdh(base) values to the ΔtDS and ΔtDH derating values, respectively. Example: Tds = Tds(base) + ΔtDS.

The typical Tds slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC)min. The typical Tds slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIL(AC)max.

If the actual signal is consistently earlier than the typical slew rate, the area shaded gray between the VREF(DC) region and the AC region, use the typical slew rate for the derating value. If the actual signal is later than the typical slew rate line anywhere between the shaded VREF(DC) region and the AC region, the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for the derating value.

The typical Tdh slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VREF(DC). The typical Tdh slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VREF(DC).

If the actual signal is consistently later than the typical slew rate line between the shaded DC-level-to-VREF(DC) region, use the typical slew rate for the derating value. If the actual signal is earlier than the typical slew rate line anywhere between shaded DC-to-VREF(DC) region, the slew rate of a tangent line to the actual signal from the DC level to VREF(DC) level is used for the derating value.

For a valid transition, the input signal must remain above or below VIH/VIL(AC) for the specified time, Tvac. The total setup time for slow slew rates could be negative (that is, a valid input signal may not have reached VIH/VIL(AC) at the time of the rising clock transition). A valid input signal is still required to complete the transition and reach VIH/VIL(AC).

For slew rates between the values listed in derating Tables, the derating values can be obtained using linear interpolation. Slew rate values are not typically subject to production testing. They are verified by design and characterization.

Data Setup and Hold Base Values (>400 MHz, 1 V/ns slew rate)

Parameter	**Data Rate**				**Reference**
	1066	**800**	**667**	**533**	
Tds (base)	-10	50	130	210	$V_{IH}/V_{IL(AC)} = V_{REF(DC)}$ ± 220Mv
Tdh (base)	80	140	220	300	$V_{IH}/V_{IL(DC)} = V_{REF(DC)}$ ± 130Mv

Notes: AC/DC referenced for 1 V/ns DQ, DM slew rate, and 2 V/ns differential DQS, $\overline{\text{DQS}}$ slew rate.

Data Setup, Hold, and Slew Rate Derating (Continued)

Derating Values for AC/DC-based Tds/Tdh (AC220) – ΔtDS, ΔtDH derating in [ps], AC/DC-based

		DQS, DQS# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH
DQ, DM slew rate V/ns	2.0	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

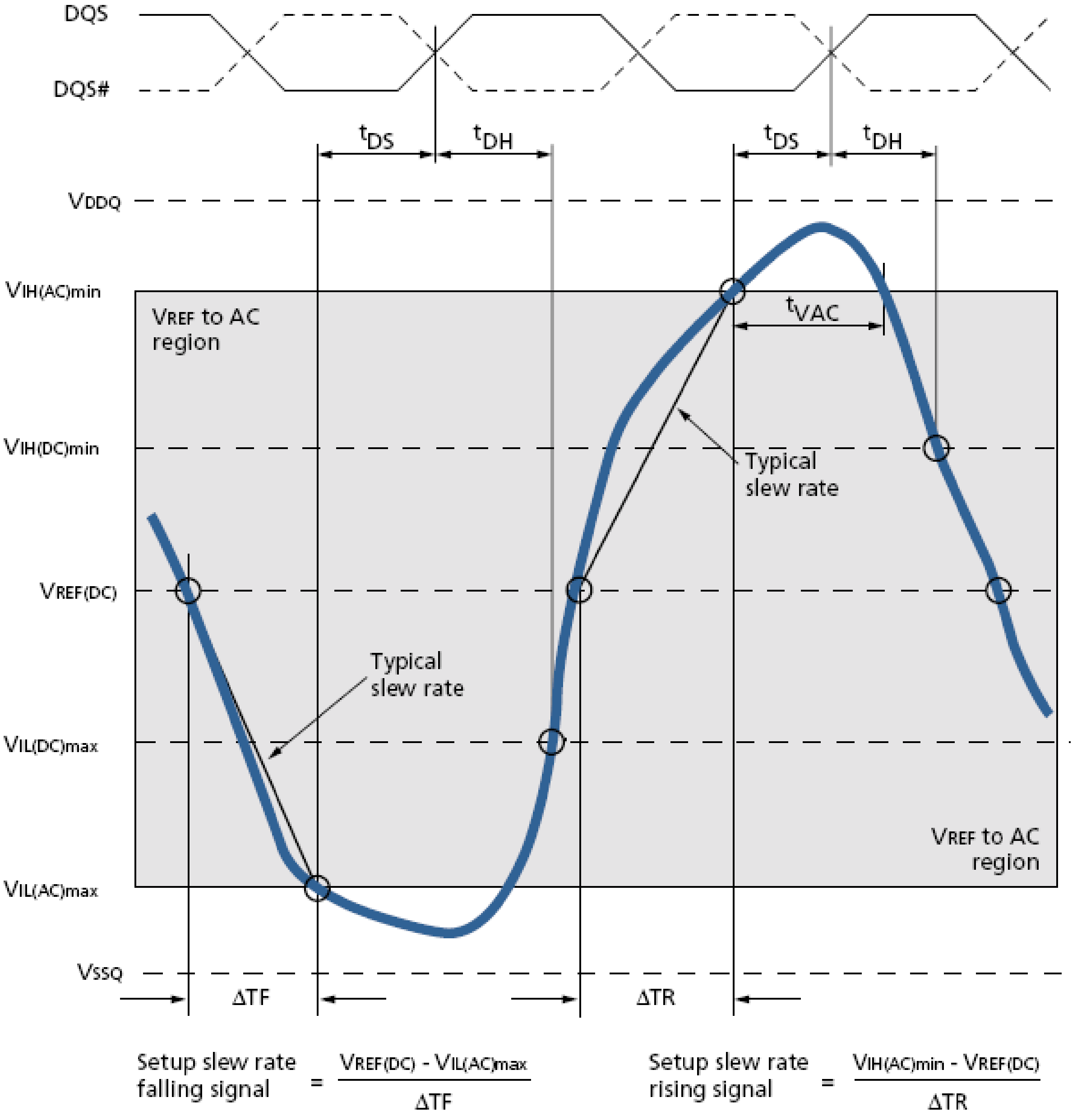
Derating Values for AC/DC-based Tds/Tdh (AC300) – ΔtDS, ΔtDH derating in [ps], AC/DC-based

		DQS, DQS# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH
DQ, DM slew rate V/ns	2.0	150	100	150	100	150	100										
	1.5	100	67	100	67	100	67	116	83								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-4	-8	-4	-8	12	8	28	24	44	40				
	0.8					-12	-20	4	-4	20	12	36	28	52	48		
	0.7							-3	-18	13	-2	29	14	45	34	61	66
	0.6									2	-21	18	-5	34	15	50	47
	0.5											-12	-32	4	-12	20	20
	0.4													-35	-40	-11	-8

Required Tvac Above VIH(AC) or Below VIL(AC) for Valid Transition

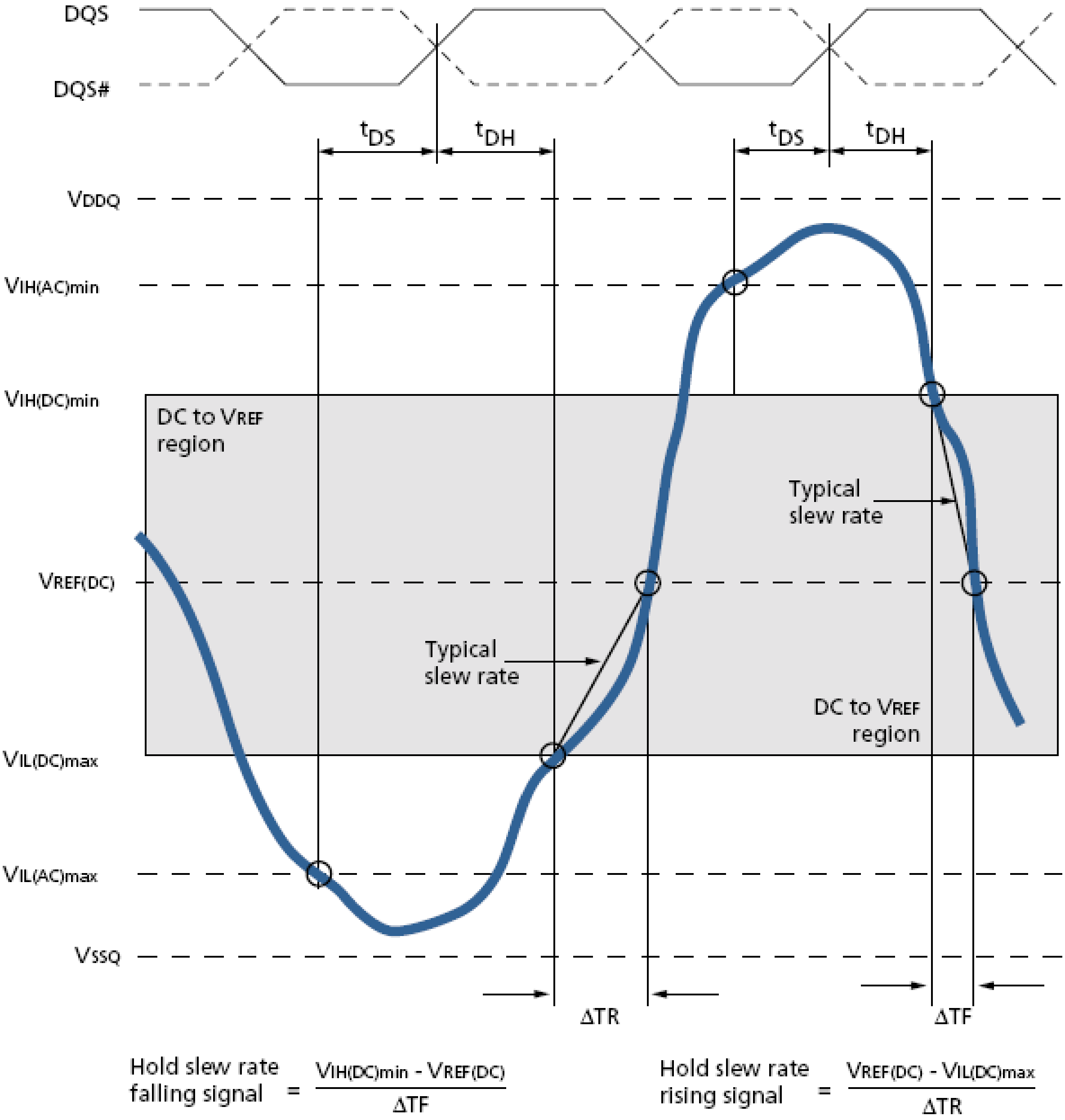
Slew Rate (V/ns)	tVAC at 300Mv (ps)		tVAC at 220Mv (ps)	
	Min	Max	Min	Max
>2.0	75	–	175	–
2	57	–	170	–
1.5	50	–	167	–
1	38	–	163	–
0.9	34	–	162	–
0.8	29	–	161	–
0.7	22	–	159	–
0.6	13	–	155	–
0.5	0	–	150	–
<0.5	0	–	150	–

Data Setup, Hold, and Slew Rate Derating (Continued)



Typical Slew Rate and Tvac: Tds for DQ Relative to Strobe

Data Setup, Hold, and Slew Rate Derating (Continued)

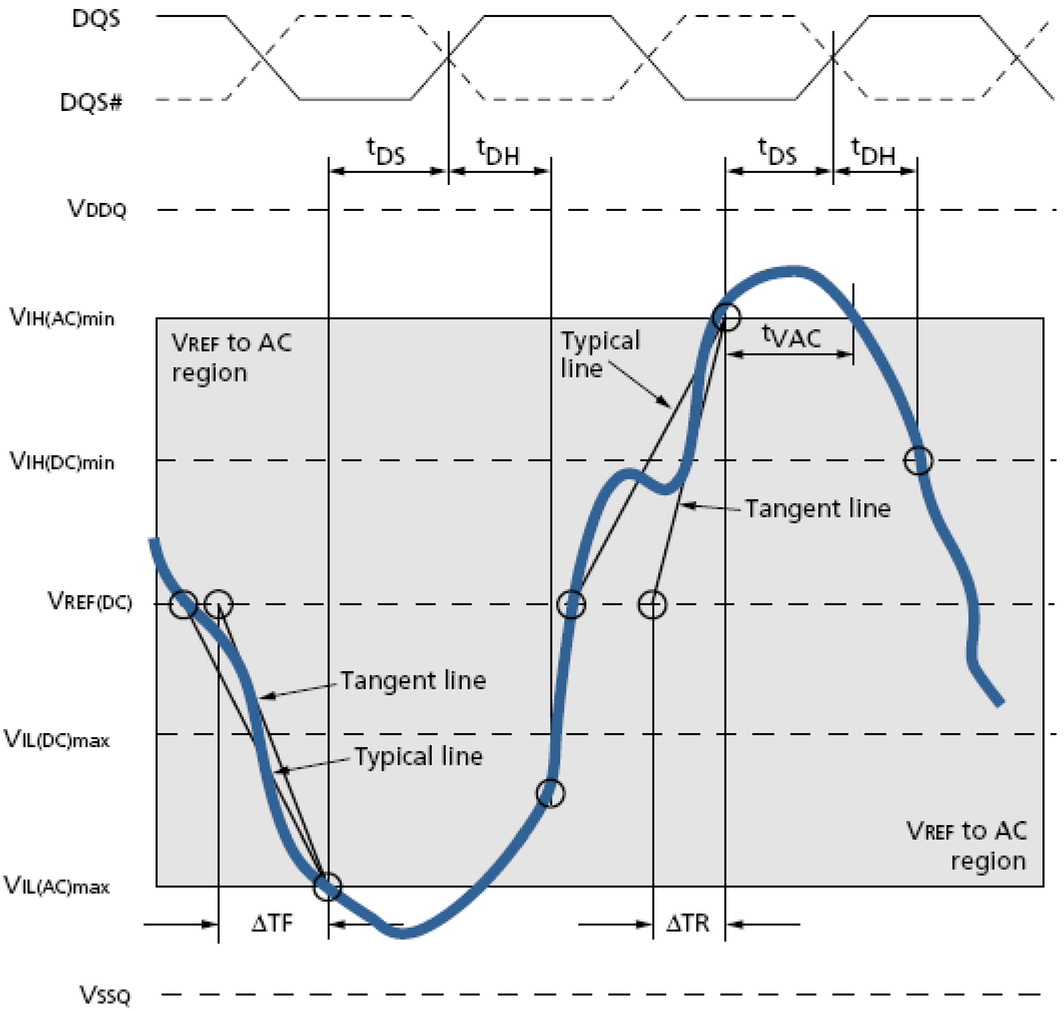


$$\text{Hold slew rate falling signal} = \frac{V_{IH(DC)min} - V_{REF(DC)}}{\Delta TF}$$

$$\text{Hold slew rate rising signal} = \frac{V_{REF(DC)} - V_{IL(DC)max}}{\Delta TR}$$

Typical Slew Rate: Tdh for DQ Relative to Strobe

Data Setup, Hold, and Slew Rate Derating (Continued)

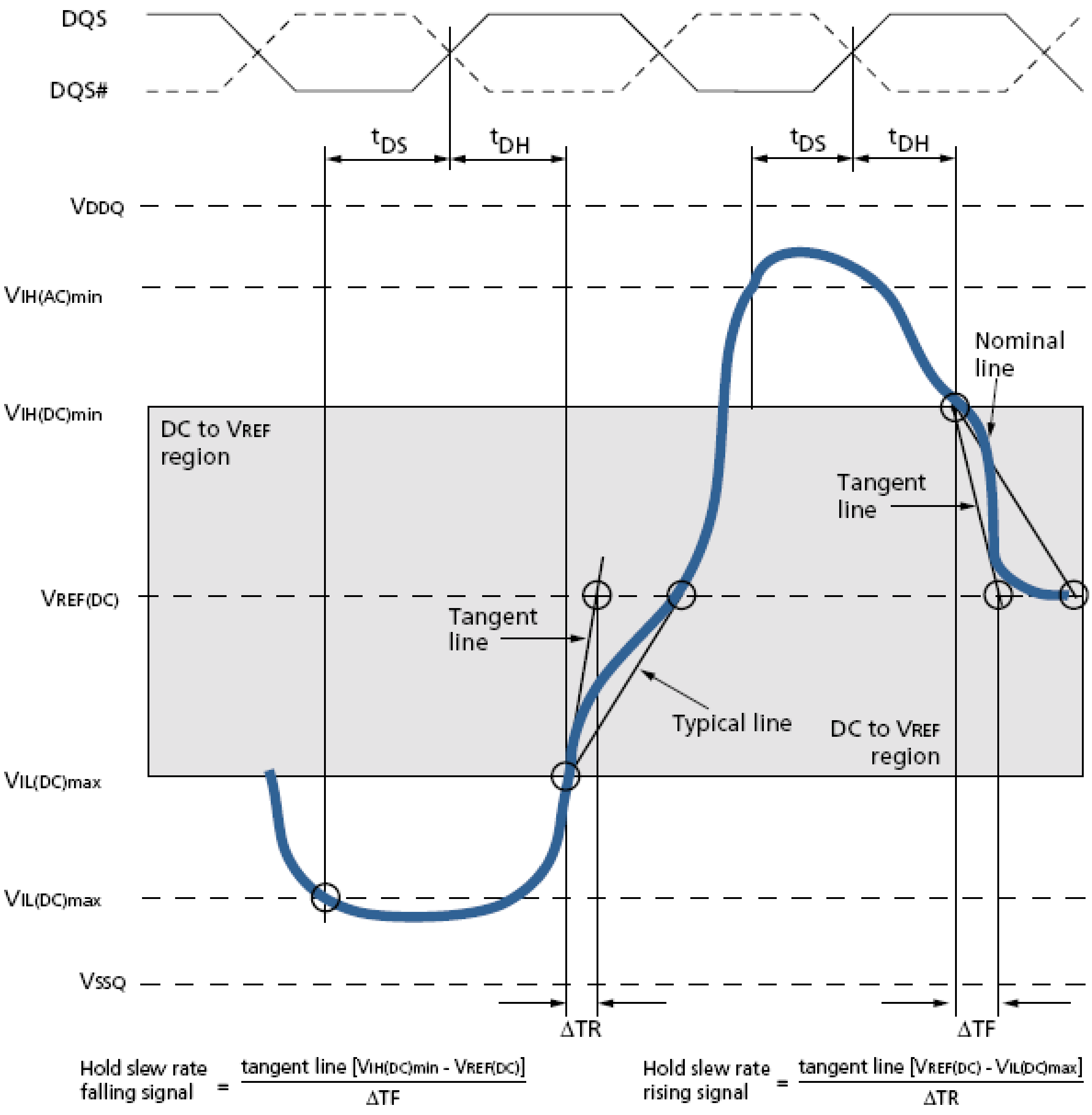


$$\text{Setup slew rate falling signal} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(AC)max}]}{\Delta TF}$$

$$\text{Setup slew rate rising signal} = \frac{\text{tangent line } [V_{IH(AC)min} - V_{REF(DC)}]}{\Delta TR}$$

Tangent Line: Tds for DQ with Respect to Strobe

Data Setup, Hold, and Slew Rate Derating (Continued)



Tangent Line: Tdh for DQ with Respect to Strobe

Basic Functionality

LPDDR2-S4 uses the double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank/Row Buffer information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

To achieve high-speed operation, our LPDDR2-S4 SDRAM uses the double data rate architecture and adopt 4n-prefetch interface designed to transfer two data per clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single 4n-bit wide, one clock cycle data transfer at the internal SDRAM core and four corresponding n-bit wide, one-half-clock-cycle data transfer at the I/O pins. Read and write accesses to the LPDDR2-S4 are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

For LPDDR2-S4 devices, accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Active command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access. As with standard DDR SDRAMs, the pipelined, multibank architecture of the LPDDR2-S4 SDRAMs supports concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power saving power-down mode. Deep power-down mode is offered to achieve maximum power reduction by eliminating the power of the memory array. Data will not be retained after device enters deep power-down mode. Two self refresh features, temperature-compensated self refresh (TCSR) and partial array self refresh (PASR), offer additional power saving. TCSR is controlled by the automatic on-chip temperature sensor. The PASR can be customized using the extended mode register settings. The two features may be combined to achieve even greater power saving. The DLL that is typically used on standard DDR devices is not necessary on the LPDDR2-S4 SDRAM. It has been omitted to save power.

Prior to normal operation, the LPDDR2-S4 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Power-Up, Initialization, and Power-Off

LPDDR2 devices must be powered up and initialized in a predefined manner. Power-up and initialization by means other than those specified will result in undefined operation.

Voltage Ramp and Device Initialization

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory and applies to devices.

1) Voltage Ramp:

While applying power (after Ta), CKE must be held LOW (≤ 0.2 × VDDCA), and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW. Following the completion of the voltage ramp (Tb), CKE must be maintained LOW. DQ, DM, DQS and DQS# voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latch up. CK, $\overline{CK}$, $\overline{CS}$, and CA input levels must be between VSSCA and VDDCA during voltage ramp to avoid latch-up. Voltage ramp power supply requirements are provided bellow.

Voltage Ramp Conditions

After…	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2—200Mv
	VDD11 and VDD2 must be greater than VDDCA—200Mv
	VDD1 and VDD2 must be greater than VDDQ—200Mv
	VREF must always be less than all other supply voltages

Notes:

1. Ta is the point when any power supply first reaches 300Mv.
2. Noted conditions apply between Ta and power-down (controlled or uncontrolled).
3. Tb is the point at which all supply and reference voltages are within their defined operating ranges. Reference voltages shall be within their respective min/max operating conditions a minimum of 5 clocks before CKE goes high.
4. Power ramp duration Tinit0 (Tb – Ta) must not exceed 20ms.
5. For supply and reference voltage operating conditions, see DC power table on page 12.
6. The voltage difference between any of VSS, VSSQ, and VSSCA pins must not exceed 100Mv.

Beginning at Tb, CKE must remain LOW for at least Tinit1 = 100 ns, after which CKE can be asserted HIGH. The clock must be stable at least Tinit2 = 5 × Tck prior to the first CKE LOW-to-HIGH transition (Tc). CKE, $\overline{CS}$, and CA inputs must observe setup and hold requirements (Tis, Tih) with respect to the first rising clock edge (as well as to subsequent falling and rising edges).

If any MRRs are issued, the clock period must be within the range defined for tCKb (18ns to 100ns). MRWs can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters (for example, Tdqsck) could have relaxed timings (such as tDQSCKb) before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least Tinit3 = 200µs (Td).

2) **RESET Command:**

After Tinit3 is satisfied, the MRW RESET command must be issued (Td). An optional PRECHARGE ALL command can be issued prior to the MRW RESET command. Wait at least Tinit4=1us while keeping CKE asserted and issuing NOP commands.

3) **MRRs and Device Auto Initialization (DAI) Polling**:

After Tinit4 is satisfied (Te), only MRR commands and power-down entry/exit commands are supported. After Te, CKE can go LOW in alignment with power-down entry and exit specifications. Use the MRR command to poll the DAI bit and report when device auto initialization is complete; otherwise, the controller must wait a minimum of Tinit5, or until the DAI bit is set before proceeding. As the memory output buffers are not properly configured by Te, some AC parameters must have relaxed timings before the system is appropriately configured. After the DAI bit (MR0, DAI) is set to zero by the memory device (DAI complete), the device is in the idle state (Tf). DAI status can be determined by issuing the MRR command to MR0. The device sets the DAI bit no later than Tinit5 after the RESET command. The controller must wait at least Tinit5 or until the DAI bit is set before proceeding.

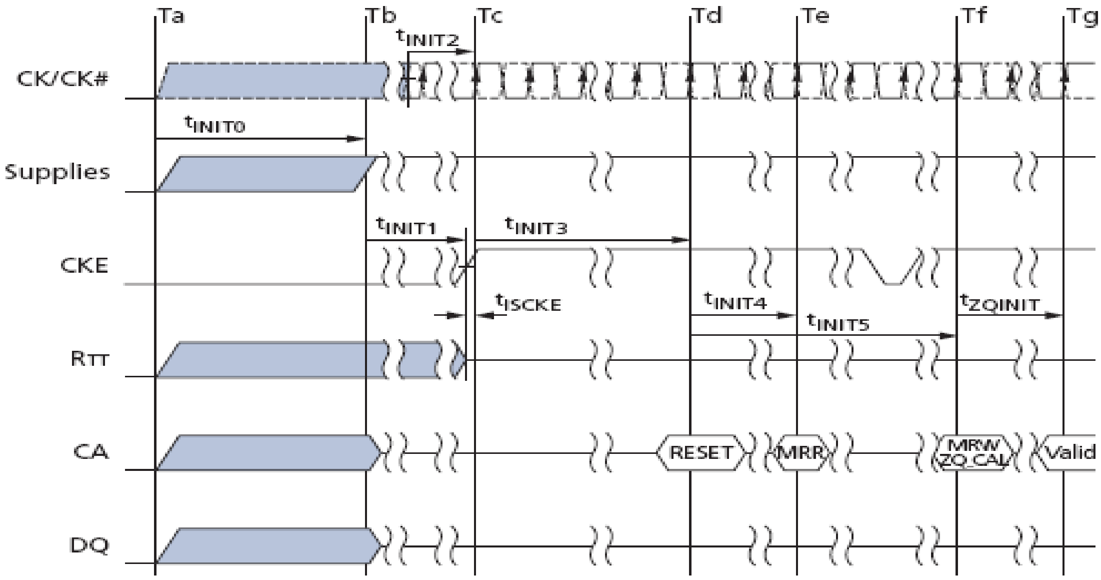
4) **ZQ Calibration**:

After Tinit5 (Tf), the MRW initialization calibration (ZQ_CAL) command can be issued to the memory (MR10). For LPDDR2 devices that do not support ZQ calibration, this command will be ignored. This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one LPDDR2 device exists on the same bus, the controller must not overlap MRW ZQ_CAL commands. The device is ready for normal operation after Tzqinit.

5) **Normal Operation**:

After Tzqinit (Tg), MRW commands must be used to properly configure the memory (for example the output buffer drive strength, latencies, etc.). Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration.After the initialization sequence is complete, the device is ready for any valid command. After Tg, the clock frequency can be changed using the procedure described in “Input Clock Frequency Changes and Clock Stop Events”.

Power Ramp and Initialization Sequence



Notes: 1. High-Z on the CA bus indicates valid NOP.   2. For Tinit values, see bellow.

Initialization Timing Parameters

Symbol	Parameter	Value		Unit
		min	max	
^{t}INIT0	Maximum Power Ramp Time	-	20	ms
^{t}INIT1	Minimum CKE low time after completion of power ramp	100	-	ns
^{t}INIT2	Minimum stable clock before first CKE high	5	-	^{t}CK
^{t}INIT3	Minimum idle time after first CKE assertion	200	-	us
^{t}INIT4	Minimum idle time after Reset command, this time will be about 2 x ^{t}RFCab + ^{t}Rpab	1	-	us
^{t}INIT5	Maximum duration of Device Auto-Initialization	-	10	us
^{t}ZQINIT	ZQ Initial Calibration	1	-	us
^{t}CKb	Clock cycle time during boot	18	100	ns

Initialization after RESET (without voltage ramp):

If the RESET command is issued before or after the power-up initialization sequence, the re-initialization procedure must begin at Td.

Power-Off Sequence

Use the following sequence to power off the device. Unless specified otherwise, this procedure is mandatory and applies to devices. While powering off, CKE must be held LOW (≤ 0.2 × VDDCA); all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW.

DQ, DM, DQS, and $\overline{DQS}$ voltage levels must be between VSSQ and VDDQ during the power-off sequence to avoid latch-up. CK, $\overline{CK}$, $\overline{CS}$, and CA input levels must be between VSSCA and VDDCA during the power-off sequence to avoid latch-up.

Tx is the point where any power supply drops below the minimum value.

Tz is the point where all power supplies are below 300Mv. After Tz, the device is powered off.

Power Supply Conditions

Between…	Applicable Conditions
Tx and Tz	VDD1 must be greater than VDD2—200Mv
Tx and Tz	VDD1 must be greater than VDDCA—200Mv
Tx and Tz	VDD1 must be greater than VDDQ—200Mv
Tx and Tz	VREF must always be less than all other supply voltages

Notes: The voltage difference between any of VSS, VSSQ, and VSSCA pins must not exceed 100Mv.

Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300Mv), the device must power off. The time between Tx and Tz must not exceed 2s. During this period, the relative voltage between power supplies is uncontrolled. VDD1 and VDD2 must decrease with a slope lower than 0.5 V/μs between Tx and Tz. An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Power-Off Timing

Symbol	Parameter	Min	Max	Unit
tpoff	Maximum power-off ramp time	-	2	s

Mode Register Definition

LPDDR2 devices contain a set of mode registers used for programming device operating parameters, reading device information and status, and for initiating special operations such as DQ calibration, ZQ calibration, and device reset.

Mode Register Assignment and Definition

Table below shows the mode registers for LPDDR2 SDRAM. Each register is denoted as “R”, if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written. Mode Register Read Command shall be used to read a register. Mode Register Write Command shall be used to write a register.

Mode Register Assignment in LPDDR2 SDRAM/NVM (Common part)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00_H	Device Info.	R	(RFU)						DI	DAI
1	01_H	Device Feature1	W	Nwr (for AP)			WC	BT	BL		
2	02_H	Device Feature2	W	(RFU)				RL & WL			
3	03_H	I/O Config-1	W	(RFU)				DS			
4	04_H	Refresh Rate	R	TUF	(RFU)				Refresh Rate		
5	05_H	Basic Config-1	R	LPDDR2 Manufacturer ID							
6	06_H	Basic Config-2	R	Revision ID1							
7	07_H	Basic Config-3	R	Revision ID2							
8	08_H	Basic Config-4	R	I/O width		Density				Type	
9	09_H	Test Mode	W	Vendor-Specific Test Mode							
10	$0A_H$	IO Calibration	W	Calibration Code							
11~15	$0B_H$~$0F_H$	(reserved)		(RFU)							

Mode Register Assignment in LPDDR2 SDRAM/NVM (SDRAM part)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
16	10_H	PASR_BANK	W	Bank Mask							
17	11_H	PASR_Seg	W	Segment Mask							
18-19	12_H-13_H	(Reserved)		(RFU)							

Mode Register Assignment in LPDDR2 SDRAM/NVM (NVM part)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
20-31	18_{H}-$1F_{H}$	Reserved for NVM									

Mode Register Assignment in LPDDR2 SDRAM/NVM (Reset Command & RFU part)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
32	20_{H}	DQ calibration pattern A	R	See “Data Calibration Pattern Description”							
33-39	21_{H}-27_{H}	(Do Not Use)									
40	28_{H}	DQ calibration pattern B	R	See “Data Calibration Pattern Description”							
41-47	29_{H}-$2F_{H}$	(Do Not Use)									
48-62	30_{H}-$3E_{H}$	(Reserved)		(RFU)							
63	$3F_{H}$	Reset	W	X							
64-126	40_{H}-$7E_{H}$	(Reserved)		(RFU)							
127	$7F_{H}$	(Do Not Use)									
128-190	80_{H}-BE_{H}	(Reserved for Vendor Use)		(RFU)							
191	BF_{H}	(Do Not Use)									
192-254	$C0_{H}$-FE_{H}	(Reserved for Vendor Use)		(RFU)							
255	FF_{H}	(Do Not Use)									

Notes:

1. RFU bits shall be set to “0” during Mode Register writes.
2. RFU bits shall be read as “0” during Mode Register reads.
3. All Mode Registers from that are specified as RFU or write-only shall return undefined data when read and DQS shall be toggled.
4. All Mode Registers that are specified as RFU shall not be written.
5. Writes to read-only registers shall have no impact on the functionality of the device.

MR0_Devcie Information (MA<7:0> = 00_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
(RFU)						DI	DAI	

OP1	DI (Device Information)	Read-only	0_B: S2 or S4 SDRAM 1_B: Do Not Use
OP0	DAI (Device Auto-Initialization Status)	Read-only	0_B: DAI complete 1_B: DAI still in progress

MR1_Devcie Feature 1 (MA<7:0> = 01_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Nwr (for AP)			WC	BT	BL			

OP<2:0>	BL (Burst Length)	Write-only	010_B: BL4 (default) 011_B: BL8 100_B: BL16 All others: reserved
OP3	BT[*1] (Burst Type)	Write-only	0_B: Sequential (default) 1_B: Interleaved
OP4	WC (Wrap)	Write-only	0_B: Wrap (default) 1_B: No wrap (allowed for SDRAM BL4 only)
OP<7:5>	Nwr[*2]	Write-only	001_B: Nwr=3 (default) 010_B: Nwr=4 011_B: Nwr=5 100_B: Nwr=6 101_B: Nwr=7 110_B: Nwr=8 All others: reserved

Notes:

1. BL16, interleaved is not an official combination to be supported.
2. Programmed value in Nwr register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(^{t}WR/^{t}CK).

Burst Sequence by BL, BT, and WC

C3	C2	C1	C0	WC	BT	BL	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
x	x	0_B	0_B	wrap	any	4	0	1	2	3												
x	x	1_B	0_B				2	3	0	1												
x	x	x	0_B	nw	any		y	y+1	y+2	y+3												
C3	**C2**	**C1**	**C0**	**WC**	**BT**	**BL**	**Burst Cycle Number and Burst Address Sequence**															
							1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**
x	0_B	0_B	0_B	wrap	seq	8	0	1	2	3	4	5	6	7								
x	0_B	1_B	0_B				2	3	4	5	6	7	0	1								
x	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
x	1_B	1_B	0_B				6	7	0	1	2	3	4	5								
x	0_B	0_B	0_B		int		0	1	2	3	4	5	6	7								
x	0_B	1_B	0_B				2	3	0	1	6	7	4	5								
x	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
x	1_B	1_B	0_B				6	7	4	5	2	3	0	1								
x	x	x	0_B	nw	any		illegal (not allowed)															
0_B	0_B	0_B	0_B	wrap	seq	16	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0_B	0_B	1_B	0_B				2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
0_B	1_B	0_B	0_B				4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
0_B	1_B	1_B	0_B				6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
1_B	0_B	0_B	0_B				8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1_B	0_B	1_B	0_B				A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
1_B	1_B	0_B	0_B				C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
1_B	1_B	1_B	0_B				E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
x	x	x	0_B		int		illegal (not allowed)															
x	x	x	0_B	nw	any		illegal (not allowed)															

Notes:
1. C0 input is not present on CA bus. It is implied zero.
2. For BL=4, the burst address represents C1~C0.
3. For BL=8, the burst address represents C2~C0.
4. For BL=16, the burst address represents C3~C0.
5. For no-wrap, BL4, the burst must not cross the page boundary or the sub-page boundary. The variable *y* can start at any address with C0 equal to 0, but must not start at any address shown bellow.

Non-Wrap Restrictions

Width	64Mb	128Mb/256Mb	512Mb/1Gb/2Gb	4Gb/8Gb
Cannot cross full page boundary				
X16	FE, FF, 00, 01	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001	7FE, 7FF, 000, 001
X32	7E, 7F, 00, 01	FE, FF, 00, 01	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001
Cannot cross sub-page boundary				
X16	7E, 7F, 80, 81	0FE, 0FF, 100, 101	1FE, 1FF, 200, 201	3FE, 3FF, 400, 401
X32	none	none	None	none

Notes: Non-wrap BL= 4 data orders shown are prohibited.

MR2_Devcie Feature 2 (MA<7:0> = 02$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
(RFU)				RL & WL				

OP<3:0>	RL & WL (Read Latency & Write Latency)	Write-only	0001$_B$: RL3 / WL1 (default) 0010$_B$: RL4 / WL2 0011$_B$: RL5 / WL2 0100$_B$: RL6 / WL3 0101$_B$: RL7 / WL4 0110$_B$: RL8 / WL4 All others: reserved

MR3_I/O Configuration 1 (MA<7:0> = 03$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
(RFU)				DS				

OP<3:0>	DS (Drive Strength)	Write-only	0000$_B$: reserved 0001$_B$: 34.3 ohm typical 0010$_B$: 40.0 ohm typical (default) 0011$_B$: 48.0 ohm typical 0100$_B$: 60.0 ohm typical 0101$_B$: reserved 0110$_B$: 80.0 ohm typical All others: reserved

MR4_Device Temperature (MA<7:0> = 04_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
TUF	(RFU)				SDRAM Refresh Rate			

OP<2:0>	SDRAM Refresh Rate	Read-only	000_B: 4 x t_{REFI}, SDRAM Low Temp. operating limit exceeded 001_B: 4 × Trefi, 4 × tREFIpb, 4 × Trefw 010_B: 2 × Trefi, 2 × tREFIpb, 2 × Trefw, 011_B: 1 × Trefi, 1 × tREFIpb, 1 × Trefw (<= 85C) 100_B: RFU 101_B: 0.25 × Trefi, 0.25 × tREFIpb, 0.25 × Trefw, don't re-rate SDRAM AC timing 110_B: 0.25 × Trefi, 0.25 × tREFIpb, 0.25 × Trefw, derate SDRAM AC timing 111_B: SDRAM High temperature operating limit exceeded
OP7	TUF (Temperature Update Flag)	Read-only	0_B: OP<2:0> value has not changed since last read of MR4. 1_B: OP<2:0> value has changed since last read of MR4.

Notes:

1. A Mode Register Read from MR4 will reset OP7 to "0".
2. OP7 is reset to "0" at power-up.
3. If OP2 equals "1", the device temperature is greater than 85C.
4. OP7 is set to "1", if OP2~OP0 has changed at any time since the last read of MR4.
5. LPDDR2 might not operate properly when OP<2:0> = 000_B or 111_B.
6. For specified operating temperature range and maximum operating temperature.
7. LPDDR2 devices must be derated by adding 1.875ns to the following core timing parameters: Trcd, Trc, Tras, Trp, and Trrd. The Tdqsck parameter must be derated .. Prevailing clock frequency specifications and related setup and hold timings remain unchanged.
8. The recommended frequency for reading MR4 is provided in "Temperature Sensor".

MR5_Basic Configuration 1 (MA<7:0> = 05$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
LPDDR2 Manufacturer ID								

OP<7:0>	Manufacturer ID	Read-only	0000 0000$_B$: Reserved 0000 0001$_B$: Samsung 0000 0010$_B$: Qimonda 0000 0011$_B$: Elpida 0000 0100$_B$: Etron 0000 0101$_B$: Nanya 0000 0110$_B$: Hynix 0000 0111$_B$: Mosel 0000 1000$_B$: Winbond 0000 1001$_B$: ESMT 0000 1010$_B$: Reserved 0000 1011$_B$: Spansion 0000 1100$_B$: SST 0000 1101$_B$: ZMOS 0000 1110$_B$: Intel 1111 1110$_B$: Numonyx 1111 1111$_B$: Micron All Others : Reserved

MR6_Basic Configuration 2 (MA<7:0> = 06$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Revision ID1								

OP<7:0>	Revision ID1	Read-only	00000000$_B$: A-version

MR7_Basic Configuration 3 (MA<7:0> = 07$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Revision ID2								

OP<7:0>	Revision ID2	Read-only	00000000$_B$: A-version

MR8_Basic Configuration 4 (MA<7:0> = 08_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
I/O width		Density				Type		

OP<1:0>	Type	Read-only	00_B: S4 SDRAM 01_B: S2 SDRAM 10_B: N NVM 11_B: Reserved
OP<5:2>	Density	Read-only	0000_B: 64Mb 0001_B: 128Mb 0010_B: 256Mb 0011_B: 512Mb 0100_B: 1Gb 0101_B: 2Gb 0110_B: 4Gb 0111_B: 8Gb 1000_B: 16Gb 1001_B: 32Gb All others: reserved
OP<7:6>	I/O width	Read-only	00_B: x32 01_B: x16 10_B: x8 11_B: not used

MR9_Test Mode (MA<7:0> = 09_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Vendor-specific Test Mode								

MR10_Calibration (MA<7:0> = $0A_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Calibration Code								

OP<7:0>	Calibration Code	Write-only	0Xff: Calibration command after initialization 0Xab: Long calibration 0x56: Short calibration 0Xc3: ZQ Reset All others: Reserved

Notes:

1. Host processor shall not write MR10 with “Reserved” values.
2. LPDDR2 devices shall ignore calibration command, when a “Reserved” values is written into MR10.
3. See AC timing table for the calibration latency.
1. If ZQ is connected to VSSCA through RZQ, either the ZQ calibration function (see “MRW ZQ Calibration Command”) or default calibration (through the ZQ RESET command) is supported. If ZQ is connected to VDDCA, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection must not change after power is supplied to the device.
5. Devices that do not support calibration ignore the ZQ calibration command.

MR11:15_(Reserved) (MA<7:0> = $0B_H$- $0F_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
RFU								

MR16_PASR_Bank Mask (MA<7:0> = 010_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Bank Mask (4-Bank or 8-Bank)								

OP<7:0>	Bank Mask Code	Write-only	0_B: refresh enable to the bank (=unmasked, default) 1_B: refresh blocked (=masked)

OP	Bank Mask	4 Bank	8 Bank
0	XXXXXXX1	Bank 0	Bank 0
1	XXXXXX1X	Bank 1	Bank 1
2	XXXXX1XX	Bank 2	Bank 2
3	XXXX1XXX	Bank 3	Bank 3
4	XXX1XXXX	-	Bank 4
5	XX1XXXXX	-	Bank 5
6	X1XXXXXX	-	Bank 6
7	1XXXXXXX	-	Bank 7

Notes: For 4-bank S4 SDRAM, only OP<3:0> are used.

MR17_PASR_Segment Mask (MA<7:0> = 011$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Segment Mask								

OP<7:0>	Segment Mask Code	Write-only	0$_B$: refresh enable to the bank (=unmasked, default) 1$_B$: refresh blocked (=masked)

Segment	OP	Bank Mask	1Gb	2Gb, 4Gb	8Gb
			R12:10	R13:11	R14:12
0	0	XXXXXXX1	000$_B$		
1	1	XXXXXX1X	001$_B$		
2	2	XXXXX1XX	010$_B$		
3	3	XXXX1XXX	011$_B$		
4	4	XXX1XXXX	100$_B$		
5	5	XX1XXXXX	101$_B$		
6	6	X1XXXXXX	110$_B$		
7	7	1XXXXXXX	111$_B$		

Notes: This table indicates the range of row addresses in each masked segment. X is don’t care for a particular segment.

MR18:19_(Reserved) (MA<7:0> = 012$_H$- 013$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
RFU								

MR20:31_(Do Not Use) (MA<7:0> = 014_H- $01F_H$):								
OP7	**OP6**	**OP5**	**OP4**	**OP3**	**OP2**	**OP1**	**OP0**	
Do Not Use								

MR32_(Do Not Use) (MA<7:0> = 020_H):								
OP7	**OP6**	**OP5**	**OP4**	**OP3**	**OP2**	**OP1**	**OP0**	
Reads to MR32 return DQ calibration pattern A								

MR33:39_(Do Not Use) (MA<7:0> = 021_H- 027_H):								
OP7	**OP6**	**OP5**	**OP4**	**OP3**	**OP2**	**OP1**	**OP0**	
Do Not Use								

MR40_(Do Not Use) (MA<7:0> = 028_H):								
OP7	**OP6**	**OP5**	**OP4**	**OP3**	**OP2**	**OP1**	**OP0**	
Reads to MR32 return DQ calibration pattern A								

MR41:47_(Do Not Use) (MA<7:0> = 029_H- $02F_H$):								
OP7	**OP6**	**OP5**	**OP4**	**OP3**	**OP2**	**OP1**	**OP0**	
Do Not Use								

MR48:62_(Reserved) (MA<7:0> = 030_H- $03E_H$):								
OP7	**OP6**	**OP5**	**OP4**	**OP3**	**OP2**	**OP1**	**OP0**	
RFU								

MR63_Reset (MA<7:0> = 03F$_H$): MRW only								
OP7	**OP6**	**OP5**	**OP4**	**OP3**	**OP2**	**OP1**	**OP0**	
X								

Notes: For additional information on MRW RESET, see “Mode Register Write Command” on Timing Spec.

MR64:126_(Reserved) (MA<7:0> = 040$_H$- 07E$_H$):								
OP7	**OP6**	**OP5**	**OP4**	**OP3**	**OP2**	**OP1**	**OP0**	
RFU								

MR127_(Do Not Use) (MA<7:0> = 07F$_H$):								
OP7	**OP6**	**OP5**	**OP4**	**OP3**	**OP2**	**OP1**	**OP0**	
Do Not Use								

MR128:190_(Reserved for Vendor Use) (MA<7:0> = 080$_H$- 0BE$_H$):								
OP7	**OP6**	**OP5**	**OP4**	**OP3**	**OP2**	**OP1**	**OP0**	
RFU								

MR191_(Do Not Use) (MA<7:0> = 0BF$_H$):								
OP7	**OP6**	**OP5**	**OP4**	**OP3**	**OP2**	**OP1**	**OP0**	
Do Not Use								

MR192:254_(Reserved for Vendor Use) (MA<7:0> = 0C0$_H$- 0FE$_H$):								
OP7	**OP6**	**OP5**	**OP4**	**OP3**	**OP2**	**OP1**	**OP0**	
RFU								

MR255_(Do Not Use) (MA<7:0> = $0FF_H$):

OP7	**OP6**	**OP5**	**OP4**	**OP3**	**OP2**	**OP1**	**OP0**	
Do Not Use								

LPDDR2-S4 SDRAM Truth Table

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

Command Truth Table

	SDR Command Pins			DDR CA pins (10)										
SDRAM command	CKE		CS_n	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CK EDGE
	CK_t(n-1)	CK_t(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
				MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
				MA6	MA7	x								↓
Refresh (per bank)[11]	H	H	L	L	L	H	L	x						↑
				x										↓
Refresh (all bank)	H	H	L	L	L	H	H	x						↑
				x										↓
Enter Self Refresh	H	L	L	L	L	H	x							↑
				x										↓
Activate (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	↑
				R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	↓
Write (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
				AP[3,4]	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Read (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
				AP[3,4]	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Precharge (bank)	H	H	L	H	H	L	H	AB	x		BA0	BA1	BA2	↑
				x										↓
BST	H	H	L	H	H	L	L	x						↑
				x										↓
Enter Deep Power Down	H	L	L	H	H	L	x							↑
				x										↓
NOP	H	H	L	H	H	H	x							↑
				x										↓
Maintain PD, SREF, DPD (NOP)	L	L	L	H	H	H	x							↑
				x										↓
NOP	H	H	H	x										↑
				x										↓
Maintain PD, SREF, DPD (NOP)	L	L	H	x										↑
				x										↓
Enter Power Down	H	L	H	x										↑
				x										↓
Exit PD, SREF, DPD	L	H	H	x										↑
				x										↓

Notes:

1. All LPDDR2ccommands are defined by states of CS_n, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
2. For LPDDR2 SDRAM, Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon.
3. AP “high” during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.

4. “x” means “H or L (but a defined logic level)”.
5. Self refresh exit and Deep Power Down exit are asynchronous.
6. V_{REF} must be between 0 and V_{DDQ} during Self Refresh and Deep Down operation.
7. Caxr refers to command/address bit “x” on the rising edge of clock.
8. Caxf refers to command/address bit “x” on the rising edge of clock.
9. CS_n and CKE are sampled at the rising edge of clock.
10. Per Bank Refresh is only allowed in devices with 8 banks.
11. The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.

CKE Truth Table

Device Current State[*3]	CKE$_{n-1}$[*1]	CKE$_n$[*1]	CS_n[*2]	Command n[*4]	Operation n[*4]	Device Next State	Notes
Active Power Down	L	L	x	x	Maintain Active Power Down	Active Power Down	
	L	H	H	NOP	Exit Active Power Down	Active	6,9
Idle Power Down	L	L	x	x	Maintain Idle Power Down	Idle Power Down	
	L	H	H	NOP	Exit Idle Power Down	Idle	6,9
Resetting Power Down	L	L	x	x	Maintain Resertting Power Down	Resetting Power Down	
	L	H	H	NOP	Exit Resetting Power Down	Idle or Resetting	6,9,12
Deep Power Down	L	L	x	x	Maintain Deep Power Down	Deep Power Down	
	L	H	H	NOP	Exit Deep Power Down	Power On	8
Self Refresh	L	L	x	x	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	7,10
Bank(s) Active	H	L	H	NOP	Enter Active Power Down	Active Power Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power Down	Idle Power Down	
	H	L	L	Enter Self-Refresh	Enter Self Refresh	Self Refresh	
	H	L	L	Enter Self-Refresh	Enter Deep Power Down	Deep Power Down	
Resetting	H	L	H	NOP	Enter Resetting Power Down	Resetting Power Down	
Other states	H	H	Refer to the Command Truth Table				

Notes:

1. “CKE$_n$” is the logic state of CKE at clock edge n; “CKE$_{n-1}$” was the logic state of CKE at previous clock edge.
2. “CS_n” is the logic state of CS_n at the clock rising edge n;
3. “Current state” is the state of the LPDDR2 device immediately prior to clock edge n.
4. “Command n” is the command registered at clock edge N, and “Operation n” is a result of “Command n”.
5. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
6. Power Down exit time (^{t}XP) should elapse before a command other than NOP is issued.
7. Self-Refresh exit time (^{t}XSR) should elapse before a command other than NOP is issued.
8. The Deep Power-Down exit procedure must be followed as discussed in the DPD section of the Functional Description.
9. The clock must toggle at least once during the ^{t}XP period.
10. The clock must toggle at least once during the ^{t}XSR period.
11. “x” means “Don’t care”.
12. Upon exiting Resetting Power Down, the device will return to the idle state if ^{t}INIT5 has expired.

Current State Bank n – Command to Bank n

Current State	Command	Operation	Next State	Notes
Any	NOP	Continue previous operation	Current State	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (Per Bank)	Begin to refresh	Refreshing (Per Bank)	6
	Refresh (All Bank)	Begin to refresh	Refreshing (AllBank)	7
	MRW	Load value from Mode Register	MR Writing	7
	MRR	Read value from Mode Register	Idle / MR Reading	
	Reset	Begin Device Auto-initialization	Resetting	7,8
	Precharge	Deactivate row in bank or banks	Precharging	9,15
Row Active	Read	Select column, and start read burst	Reading	
	Write	Select column, and start write burst	Writing	
	MRR	Read value from Mode Register	Active / MR Reading	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading	Read	Select column, and start new read burst	Reading	10,11
	Write	Select column, and start write burst	Writing	10,11,12
	BST	Read burst terminate	Active	13
Writing	Write	Select column, and start new write burst	Writing	10,11
	Read	Select column, and start read burst	Reading	10,11,14
	BST	Write burst terminate	Active	13
Power On	Reset	Begin Device Auto-initialization	Resetting	7,9
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Notes:

1. The table applies when both CKE_{n-1} and CKE_n are HIGH, and after ^tXSR or ^tXP has been met, if the previous state was Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current State definitions:

State	Definition
Idle	The bank or banks have been precharged, and ᴛrp has been met.
Active	A row in the bank has been activated, and ᴛrcd has been met. No data bursts or accesses and no register accesses are in progress.
Reading	A READ burst has been initiated with auto precharge disabled, and has not yet terminated or been terminated.
Writing	A WRITE burst has been initiated with auto precharge disabled, and has not yet terminated or been terminated.

4. The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other bank should been issued on any clock edge occurring during these states.

State	Starts with	Ends when	Notes
Refreshing (per bank)	Registration of a REFRESH (per bank) command	tRFCpb is met	After tRFCpb is met, the bank is in the idle state.
Refreshing (all banks)	Registration of a REFRESH (allbank) command	tRFCab is met	After tRFCab is met, the device is in the all-banksidle state.
Iele MR reading	Registration of the MRR command	Tmrr is met	After Tmrr is met, the device is in the all-banksidle state..
Resetting MR reading	Registration of the MRR command	Tmrr is met	After Tmrr is met, the device is in the all-banksidle state.
Active MR reading	Registration of the MRR command	Tmrr is met	After Tmrr is met, the bank is in the active state.
MR writing	Registration of the MRW command	Tmrw is met	After Tmrw is met, the device is in the all-banksidle state.
Precharge all	Registration of a PRECHARGE ALL command	Trp is met	After Trp is met, the device is in the all-banksidle state.

5. The states listed below must not be interrupted by any executable command. NOP commands must be applied to each positive clock edge during these states.

State	Starts with	Ends when	Notes
Precharging	Registration of a PRECHARGE command	Trp is met	After Trp is met, the bank is in the idle state.
Row Active	Registration of an ACTIVATE command	Trcd is met	After Trcd is met, the bank is in the active state.
READ with AP enable	Registration of a READ command with auto precharge enabled	Trp is met	After Trp is met, the bank is in the idle state.
WRITE with AP enable	Registration of a WRITE command with auto precharge enabled	Trp is met	After Trp is met, the bank is in the idle state.

6. Bank-specific; requires that the bank is idle and no bursts are in progress.

7. Not bank-specific; requires that all banks are idle and no bursts are in progress.

8. Not bank-specific reset command is achieved through Mode Register Write command.

9. This command may or may not be bank specific. If all banks are being precharged, the must be in a valid state for precharging.

10. A command other than NOP should not be issued to the same bank while a READ or WRITE burst with auto precharge is enabled.

11. The new READ or WRITE command could be auto precharge enabled or auto precharge disabled.

12. A WRITE command can be issued after the completion of the READ burst; otherwise, a BST must be issued to end the READ prior to asserting a WRITE command.

13. Not bank-specific. The BST command affects the most recent READ/WRITE burst started by the most recent READ/WRITE command, regardless of bank.

14. A READ command can be issued after completion of the WRITE burst; otherwise, a BST must be used to end the WRITE prior to asserting another READ command.

15. If a PRECHARGE command is issued to a bank in the idle state, Trp still applies.

Current State Bank n – Command to Bank m

Current State of Bank n	Command for Bank m	Operation	Next State for Bank m	Notes
Any	NOP	Continue previous operation	Current State of Bank m	
Idle	Any	Any command allowed to Bank m	-	18
Row Activating, Active, or Precharging	Activate	Select and activate row in Bank m	Active	7
	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8
	Precharge	Deactivate row in bank or banks	Precharging	9
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Reading	10,11,13
	BST	Read or Write burst terminate an ongoing Read/Write from/to Bank m	Active	18
Reading (AP disabled)	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8,14
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing (AP disabled)	Read	Select column, and start read burst from Bank m	Reading	8,16
	Write	Select column, and start write burst to Bank m	Writing	8
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading with Auto-Precharge	Read	Select column, and start read burst from Bank m	Reading	8,15
	Write	Select column, and start write burst to Bank m	Writing	8,14,15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing with Auto-Precharge	Read	Select column, and start read burst from Bank m	Reading	8,15,16
	Write	Select column, and start write burst to Bank m	Writing	8,15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Power On	Reset	Begin Device Auto-initialization	Resetting	12,17
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Notes:

1. The table applies when both CKE_{n-1} and CKE_n are HIGH, and after ^tXSR or ^tXP has been met, if the previous state was Self Refresh or Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current State definitions:
    3.1) Idle: the bank has been precharged, and Trp has been met
    3.2) Active: a row in the bank has been activated, and Trcd has been met. No data bursts/accesses and no register accesses are in progress.
    3.3) Reading: a Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
    3.4) Writing: a Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4. Refresh, Self-Refresh, and Mode Register Write commands may only be issued when all bank are idle.
5. A Burst Terminate (BST) command can not be issued to another bank; it applies to the bank represented by the current state only.
6. The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:
    6.1) Idle MR Reading: starts with the registration of a MRR command and ends when T_{mrr} has been met. Once T_{mrr} has been met,The bank will be in the Idle state.
    6.2) Resetting MR Reading: starts with the registration of a MRR command and ends when T_{mrr} has been met. Once T_{mrr} has been met, the bank will be in the Resetting state.
    6.3) Active MR Reading: starts with the registration of a MRR command and ends when T_{mrr} has been met. Once T_{mrr} has been met, the bank will be in the Active state.
    6.4) MR Writing: starts with the registration of a MRW command and ends when T_{mrw} has been met. Once T_{mrw} has been met, the bank will be in the Idle state.

7.Trrd must be met between the ACTIVATE command to bank *n* and any subsequent ACTIVATE command to bank *m*.

8. READs or WRITEs listed in the command column include READs and WRITEs with or without auto precharge enabled.

9. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.

10. MRR is supported in the row-activating state.

11. MRR is supported in the precharging state.

12. Not bank-specific; requires that all banks are idle and no bursts are in progress.

13. The next state for bank *m* depends on the current state of bank *m* (idle, row-activating, precharging, or active).

14. A WRITE command can be issued after the completion of the READ burst; otherwise a BST must be issued to end the READ prior to asserting a WRITE command.

15. A READ with auto precharge enabled or a WRITE with auto precharge enabled can be followed by any valid command to other banks with timing restriction.

16. A READ command can be issued after the completion of the WRITE burst; otherwise, a BST must be issued to end the WRITE prior to asserting another READ command.

17. RESET command is achieved through MODE REGISTER WRITE command.

18. BST is supported only if a READ or WRITE burst is ongoing.

DM Operation Truth Table

Function	DM	DQ	Notes
Write Enable	L	Valid	1
Write Inhibit	H	X	1

Notes:

1. Used to mask write data, provided coincident with the corresponding data.

COMMAND Definitions and Timing Diagrams

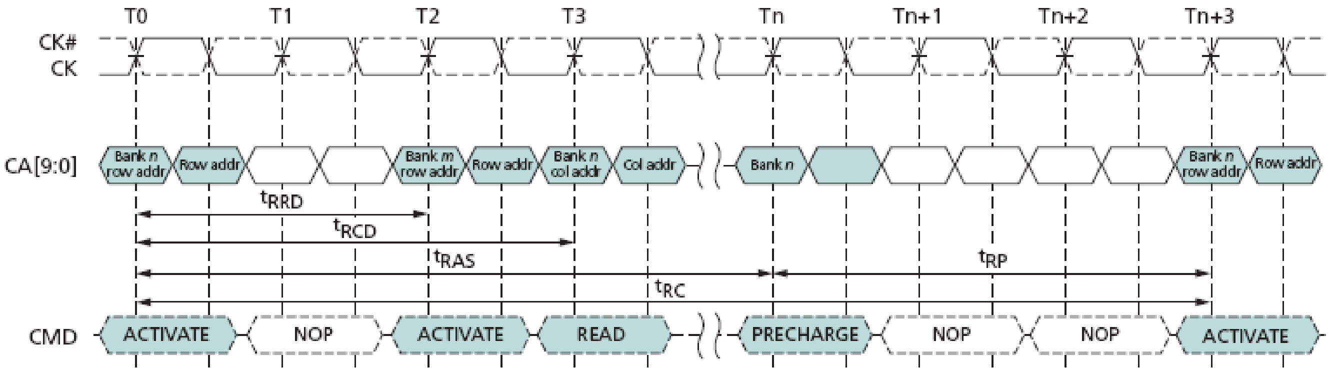
ACTIVE

The Active command is issued by holding CS_n LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA0-BA2 are used to select the desired bank. The row addresses R0-R14 is used to determine which row in the selected bank. The Active command must be applied before any Read or Write operation can be executed. The LPDDR2 SDRAM can accept a read or write command at time ^{t}RCD after the active command is sent. Once a bank has been active, it must be precharged before another Active command can be applied to the same bank. The bank active and precharge times are defined as ^{t}RAS and ^{t}RP, respectively. The minimum time interval between two successive ACTIVE commands on the same bank is determined by the RAS cycle time of the device (^{t}RC). The minimum time interval between two successive ACTIVE commands on different banks is defined by ^{t}RRD.

Certain restriction on operation of the 8 bank devices must be observed. One for restricting the number of sequential Active commands that can be issued and another for allowing more time for RAS precharge for a Precharge All command. The rules are as follows:

8 bank device Sequential Bank Activation Restriction: No more than 4 banks may be activated (or refreshed, in the case of REF_{pb}) in a rolling ^{t}FAW window. Converting to clocks is done by diving Tfaw[ns] by ^{t}CK[ns], and rounding up to the next integer value. A an example of the rolling window, if RU{(^{t}FAW / ^{t}CK)} is 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued at or between clock N+1 and N+9. REF_{pb} also counts as bank-activation for the purposes of ^{t}FAW.

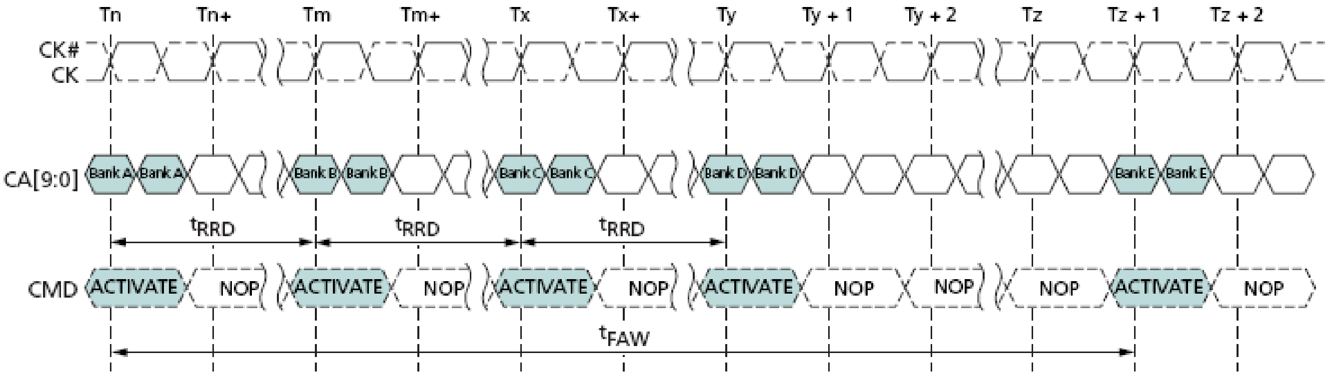
8 bank device Precharge All allowance: ^{t}RP for a Precharge All command for an 8 Bank device shall equal to $^{t}\text{RP}_{ab}$, which is greater than $^{t}\text{RP}_{pb}$.



Activate command cycle: Trcd=3, Trp=3, Trrd=2

Notes:

1. A Precharge-All command uses tRPab timing, while a Single Bank Precharge command uses tRPpb timing. In this figure, Trp is used to denote either an All-bank Precharge or a Single Bank Precharge.

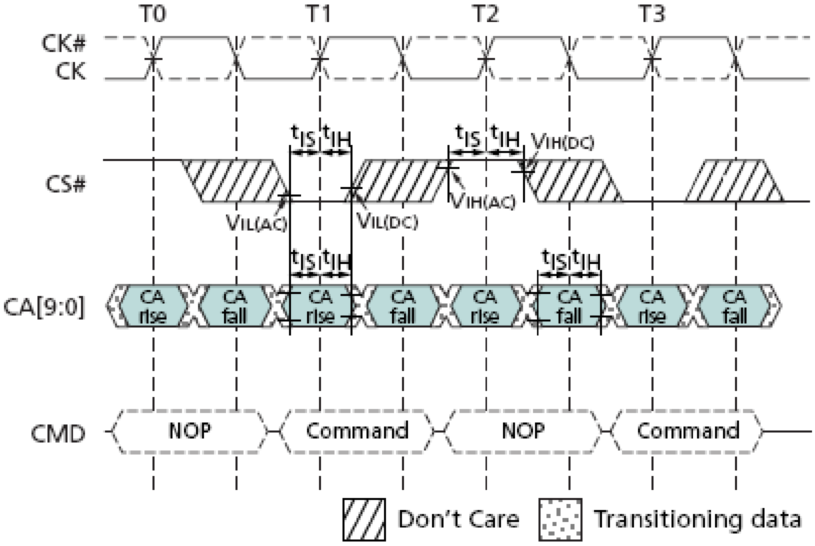


Tfaw timing

Notes:

1. Exclusively for 8-bank devices. No more than 4 banks may be activated in a rolling Tfaw window.

Command Input Signal Timing Definition



Command Input Setup and Hold Timing

Notes:

1. Setup and hold conditions also apply to the CKE pin.

Read and Write access modes

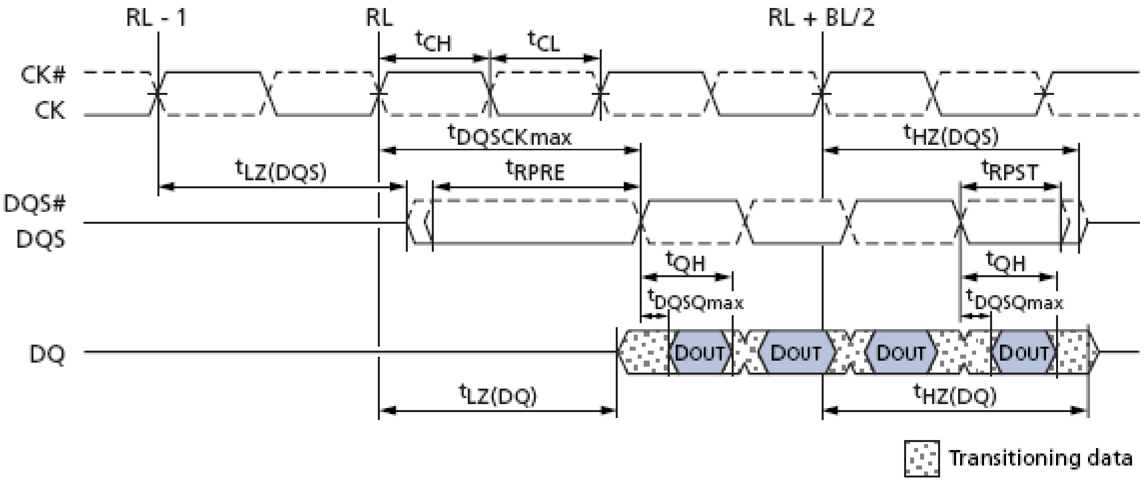
After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting CS_n LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a read operation (CA2 HIGH) or a write operation (CA2 LOW).

The LPDDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a burst read or write operation on successive clock cycles.

For LPDDR2-S4 devices, a new burst access must not interrupt the previous 4-bit burst operation, in case of BL=4 setting. In case of BL=8 and BL=16 settings, Reads may be interrupted by Reads, and Writes may be interrupted by Writes provided that this occurs on even clock cycles after the Read or Write command and that ^{t}CCD is met. The minimum CAS to CAS delay is defined by ^{t}CCD.

Burst Read

The Burst Read command is initiated by having CS_n LOW, CA0 HIGH, CA1 LOW and CA2 HIGH at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. The Read Latency (RL) is defined from the rising edge of the clock on which the Read Command is issued to the rising edge of the clock from which the ^{t}DQSCK delay is measured. The first valid datum is available RL * ^{t}CK + ^{t}DQSCK + ^{t}DQSQ after the rising edge of the clock where the Read Command is issued. The data strobe output is driven LOW ^{t}RPRE before the first rising valid strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin edge aligned with the data strobe. The RL is programmed in the mode registers. Timings for the data strobe are measured relative to the crosspoint of DQS and its complement, DQS_c.

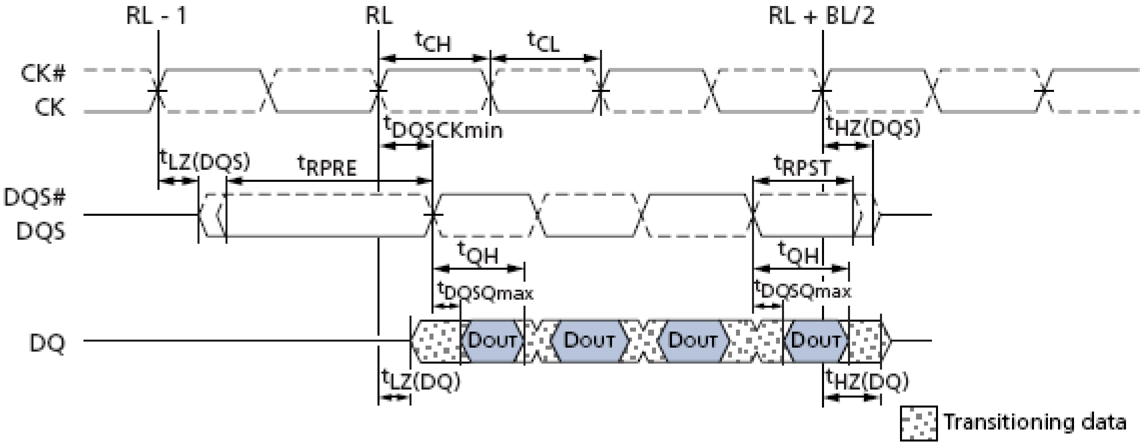


Data output (Read) timing (tDQSCKmax)

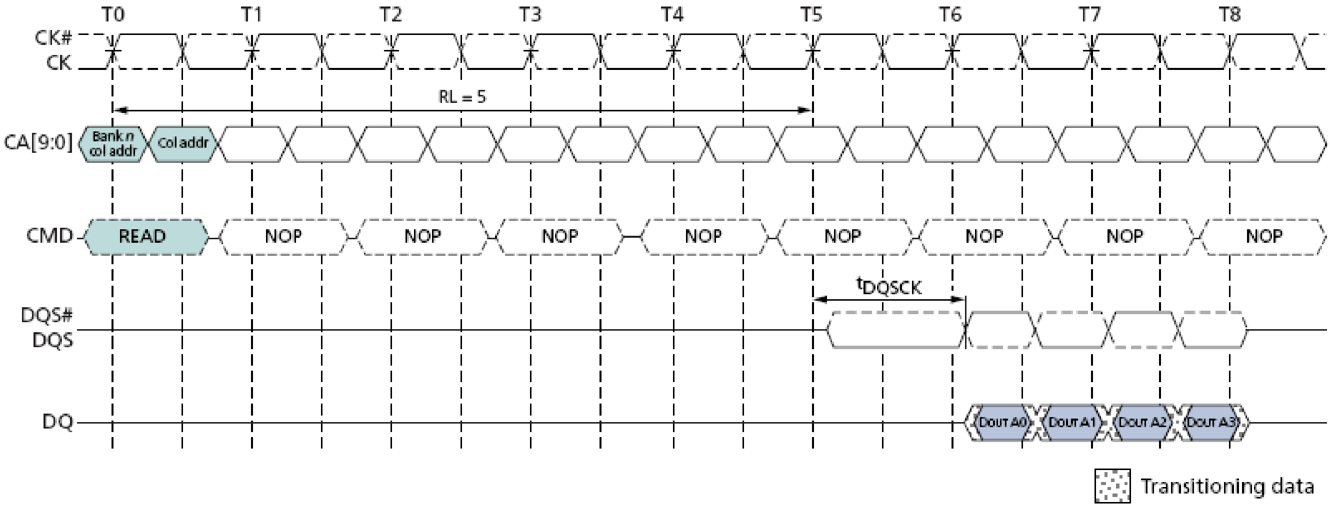
Notes:

1. Tdqsck can span multiple clock periods.
2. An effective Burst Length of 4 is shown.

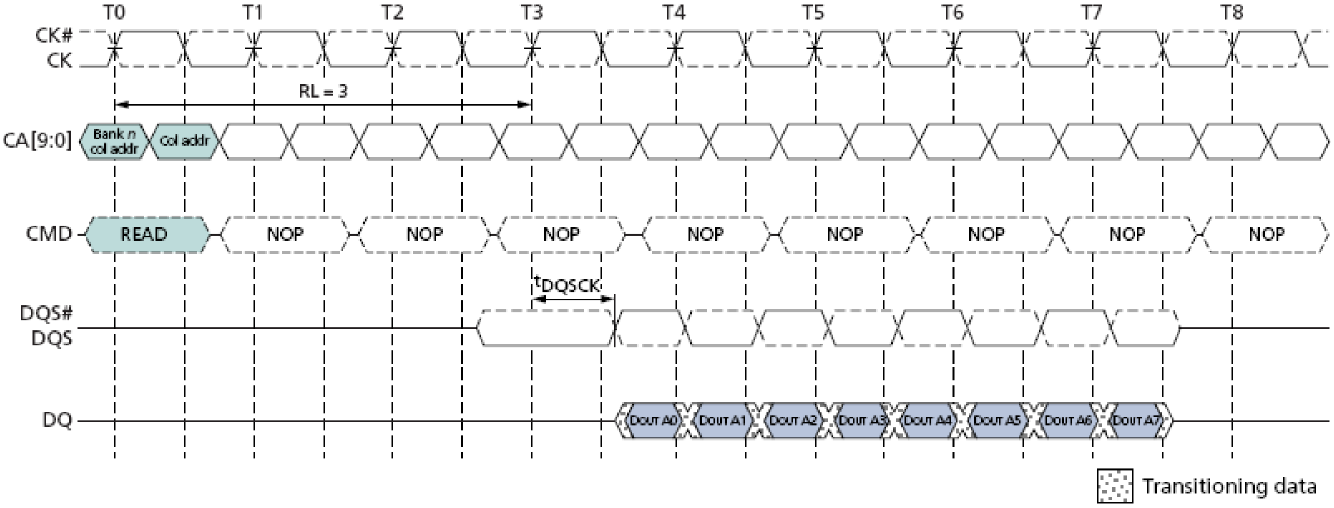
Burst Read (Continued)



Data output (Read) timing (tDQSCKmin), BL=4

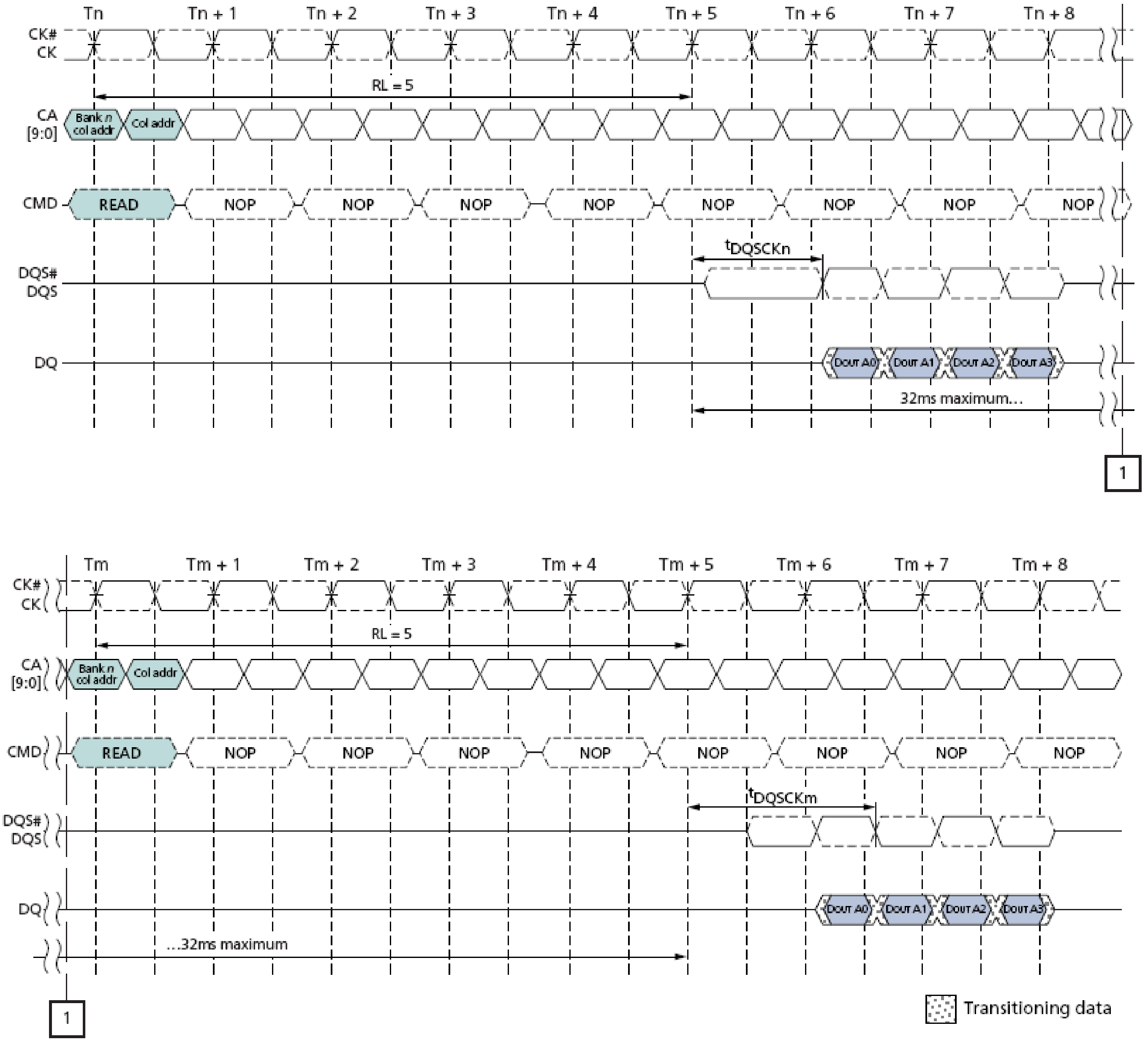


Burst Read: RL=5, BL=4, Tdqsck > Tck



Burst Read: RL=3, BL=8, Tdqsck < Tck

Burst Read (Continued)

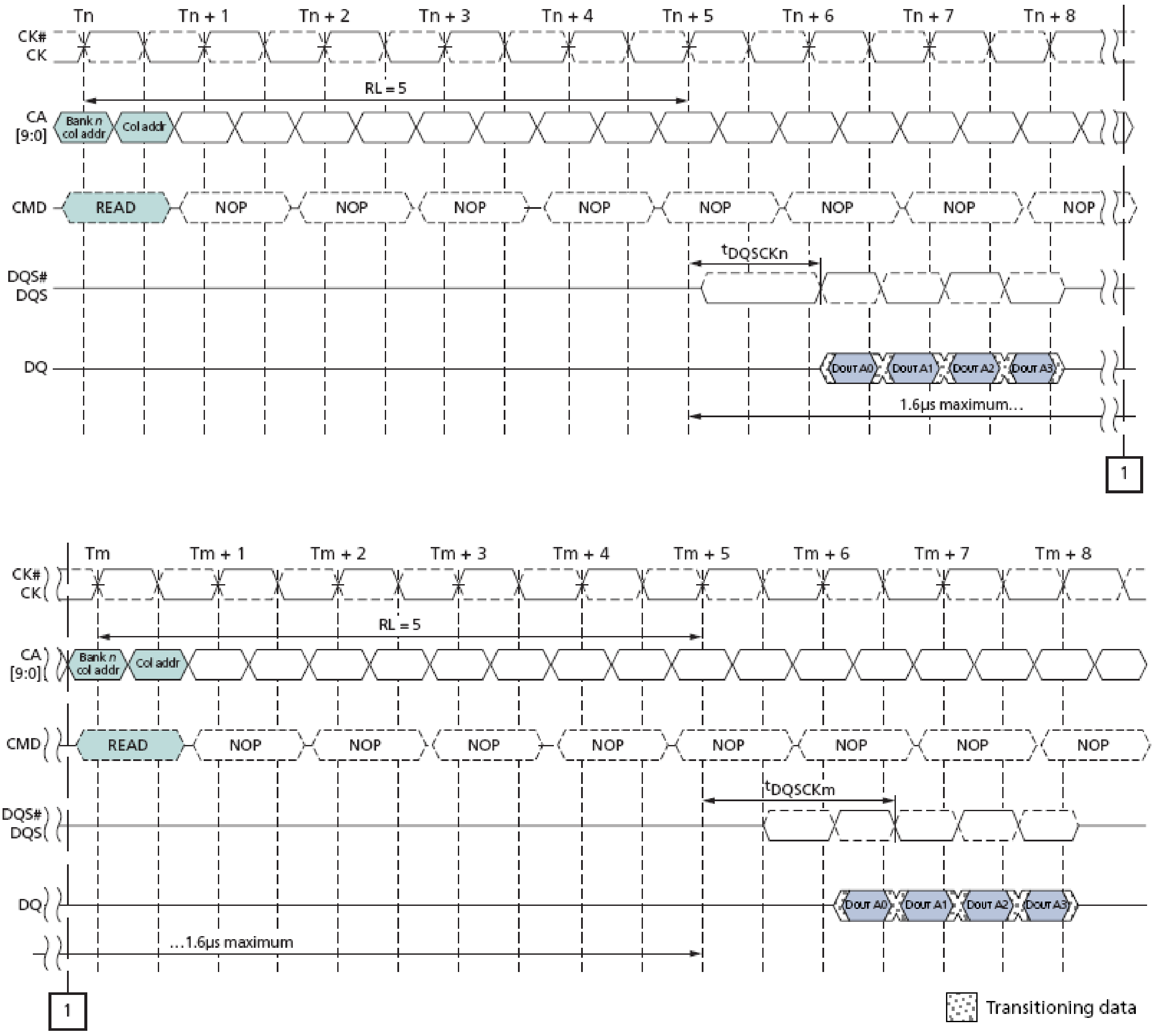


Tdqsckdl timing : Tdqsckdl = |tDQSCKn – tDQSCKm| within any 32ms rolling window

Notes:

2. tDQSCKDLmax is defined as the maximum of ABS(tDQSCKn – tDQSCKm) for any { tDQSCKn – tDQSCKm} pair within any 32ms rolling window.

Burst Read (Continued)

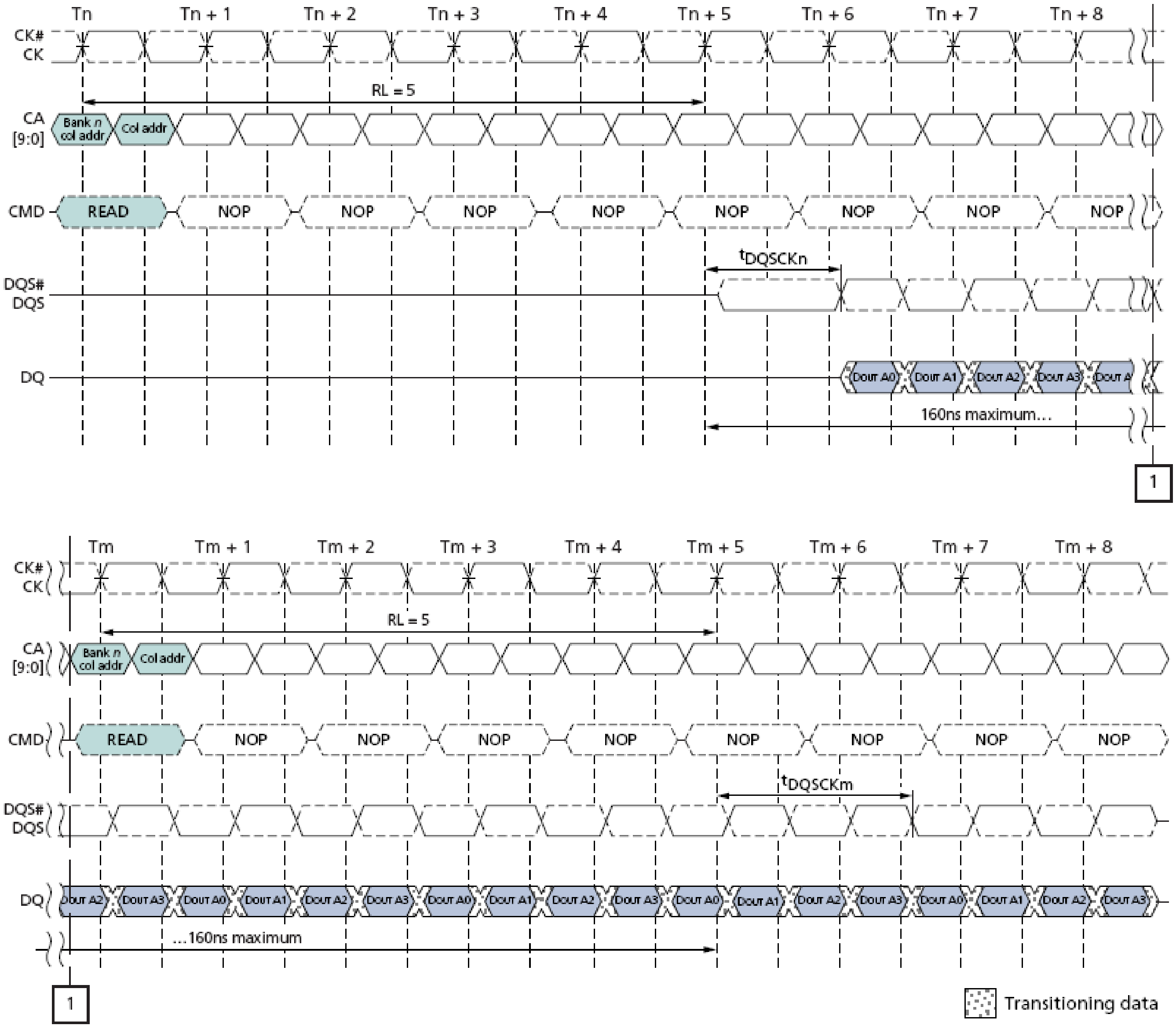


Tdqsckdm timing : Tdqsckdm= |tDQSCKn – tDQSCKm| within any 1.6us rolling window

Notes:

3. tDQSCKDMmax is defined as the maximum of ABS(tDQSCKn – tDQSCKm) for any { tDQSCKn – tDQSCKm} pair within any 1.6us rolling window.

Burst Read (Continued)

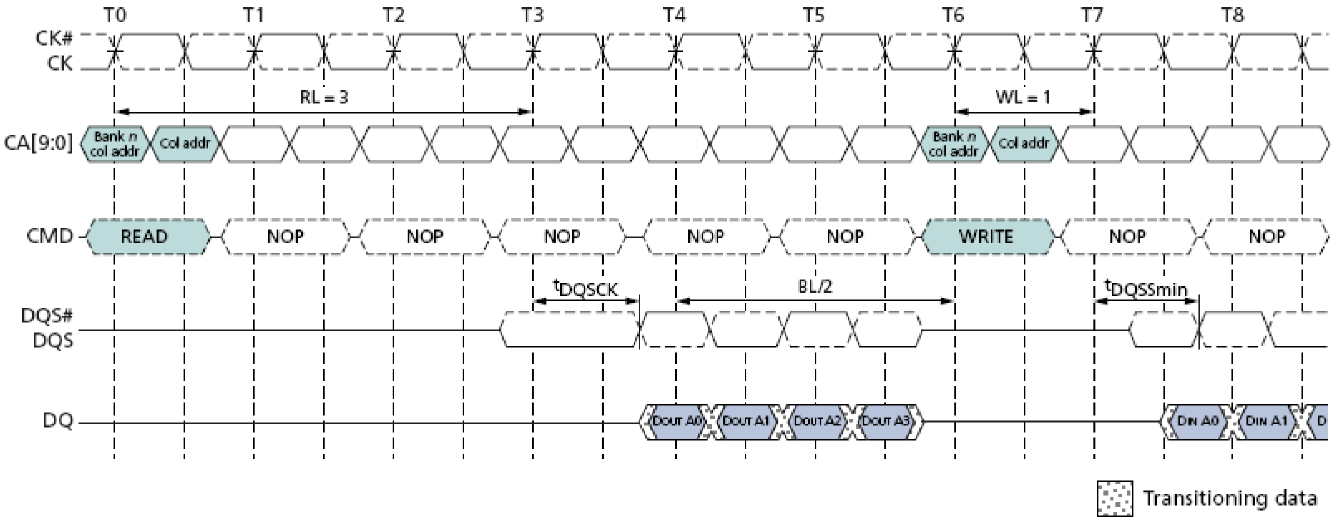


Tdqsckds timing : Tdqsckds = |tDQSCKn – tDQSCKm| within a consecutive burst within any 160ns rolling window

Notes:

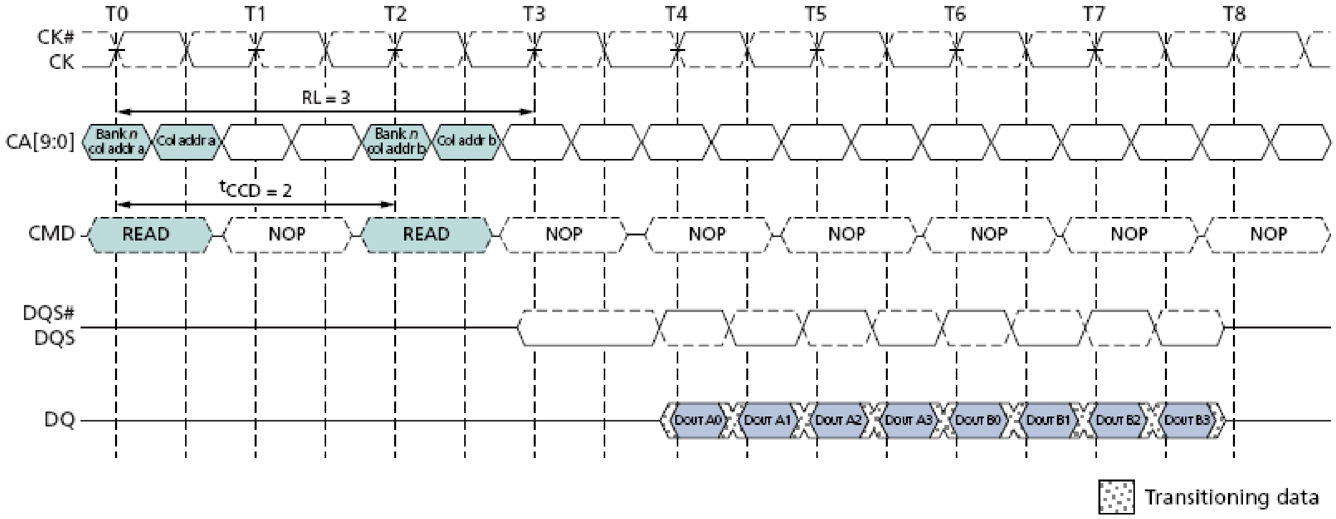
1. tDQSCKDSmax is defined as the maximum of ABS(tDQSCKn – tDQSCKm) for any { tDQSCKn – tDQSCKm} pair for reads within a consecutive burst within any 160ns rolling window.

Burst Read (Continued)



Burst Read followed by burst write: RL=3, WL=1, BL=4

The minimum time from the burst READ command to the burst WRITE command is defined by the read latency (RL) and the burst length (BL). Minimum READ-to-WRITE latency is RL + RU(Tdqsck(MAX)/Tck) + BL/2 + 1 – WL clock cycles. Note that if a READ burst is truncated with a burst TERMINATE (BST) command, the effective burst length of the truncated READ burst should be used as “BL” to calculate the minimum READ-to-WRITE delay.

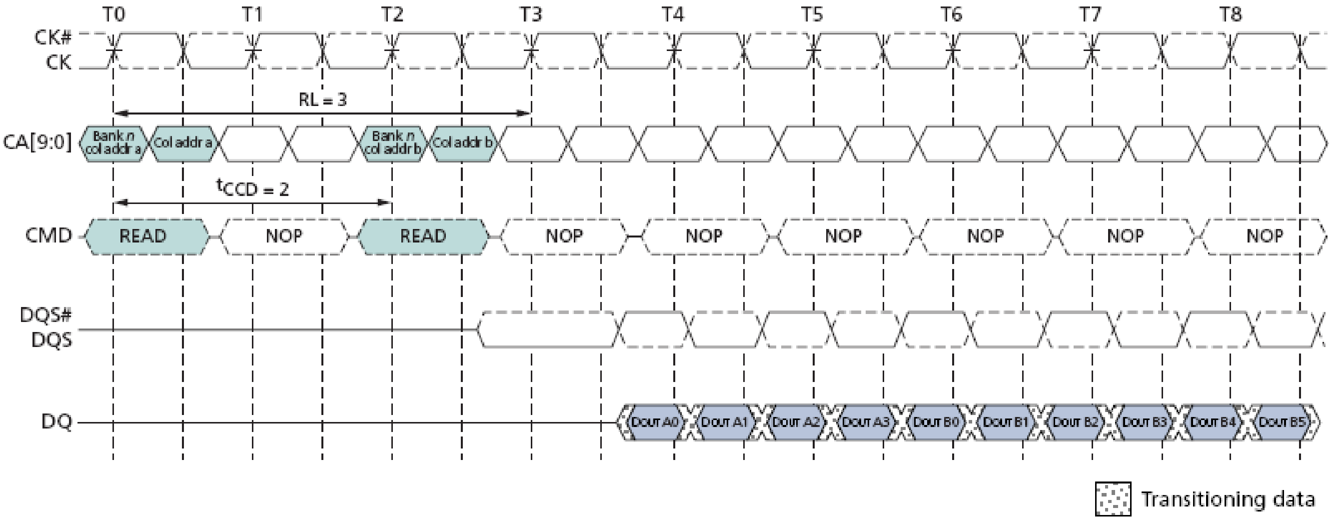


Seamless Burst Read: RL=3, BL=4, Tccd=2

The seamless burst READ operation is supported by enabling a READ command at every other clock cycle for BL = 4 operation, every fourth clock cycle for BL = 8 operation, and every eighth clock cycle for BL=16 operation. This operation is supported as long as the banks are activated, whether the accesses read the same or different banks.

Burst Read (Continued)

For LPDDR2-S4 devices, burst read can be interrupted by another read on even clock cycles after the Read command, provided that ^{t}CCD is met. For LPDDR2-S2 devices, burst reads may be interrupted by other reads on any subsequent clock, provided that ^{t}CCD is met.



Read burst interrupt example: RL=3, BL=8, ^{t}CCD=2

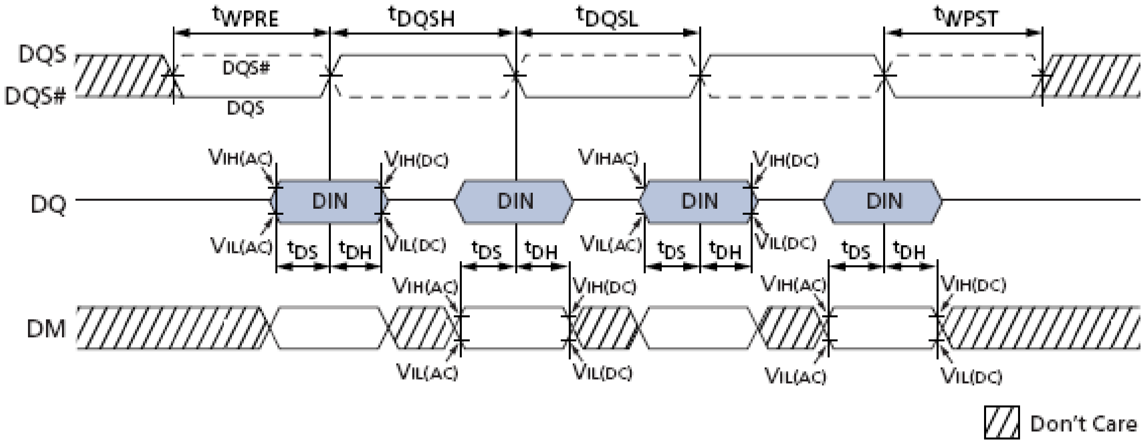
Notes:

1. Reads can only be interrupted by other reads or the BST command.
2. The effective burst length of the first read equals two times the number of clock cycles between the first read and the interrupting read.

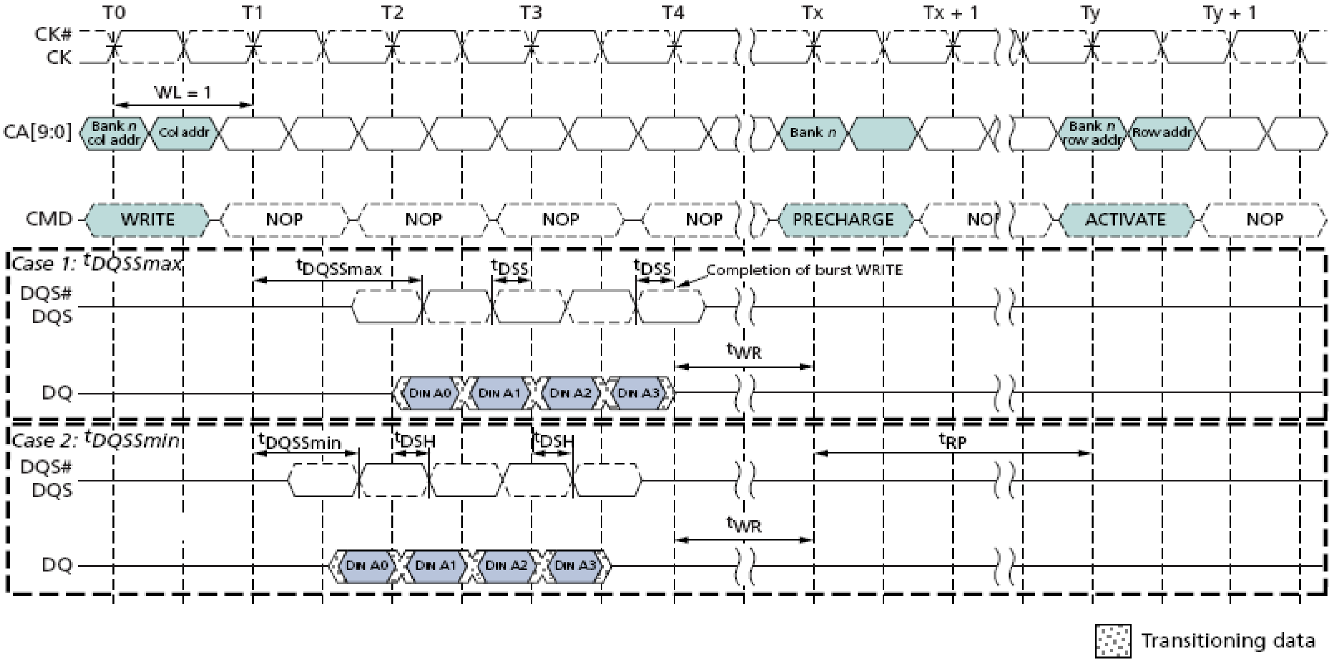
Burst Write

The burst WRITE command is initiated with $\overline{\text{CS}}$ LOW, CA0 HIGH, CA1 LOW, and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r–CA6r and CA1f–CA9f, determine the starting column address for the burst. Write latency (WL) is defined from the rising edge of the clock on which the WRITE command is issued to the rising edge of the clock from which the Tdqss delay is measured. The first valid data must be driven WL × Tck + Tdqss from the rising edge of the clock from which the WRITE command is issued. The data strobe signal (DQS) must be driven LOW Twpre prior to data input. The burst cycle data bits must be applied to the DQ pins Tds prior to the associated edge of the DQS and held valid until Tdh after that edge. Burst data is sampled on successive edges of the DQS until the 4-, 8-, or 16-bit burst length is completed. After a burst WRITE operation, Twr must be satisfied before a PRECHARGE command to the same bank can be issued.

Pin input timings are measured relative to the cross point of DQS and its complement, $\overline{\text{DQS}}$.

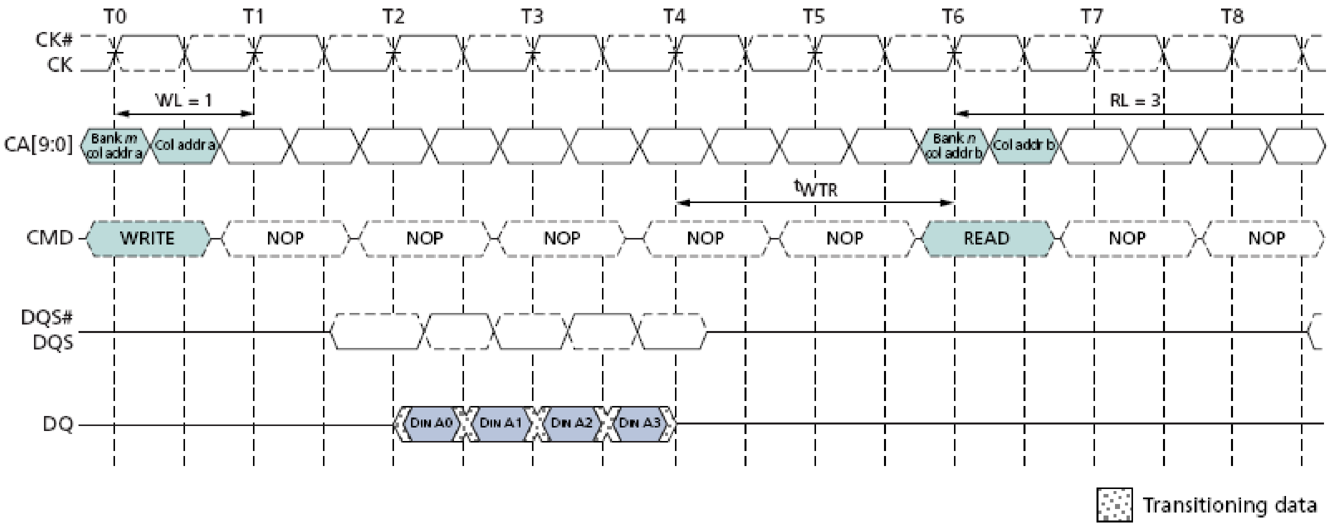


Data input (Write) timing



Burst write: WL=1, BL=4

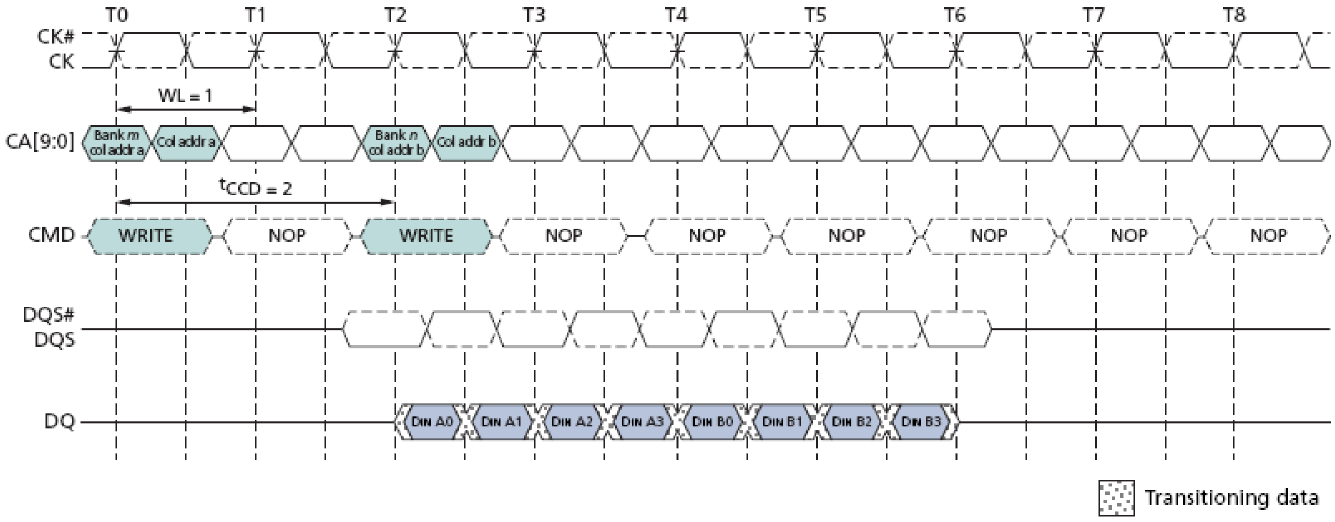
Burst Write (Continued)



Burst write followed by burst read: RL=3, WL=1, BL=4

Notes:

1. The minimum number of clock cycles from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU (Twtr / Tck)].
2. Twtr starts at the rising edge of the clock after the last valid input datum.
3. If a write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated write burst should be used as “BL” to calculate the minimum write to read delay.

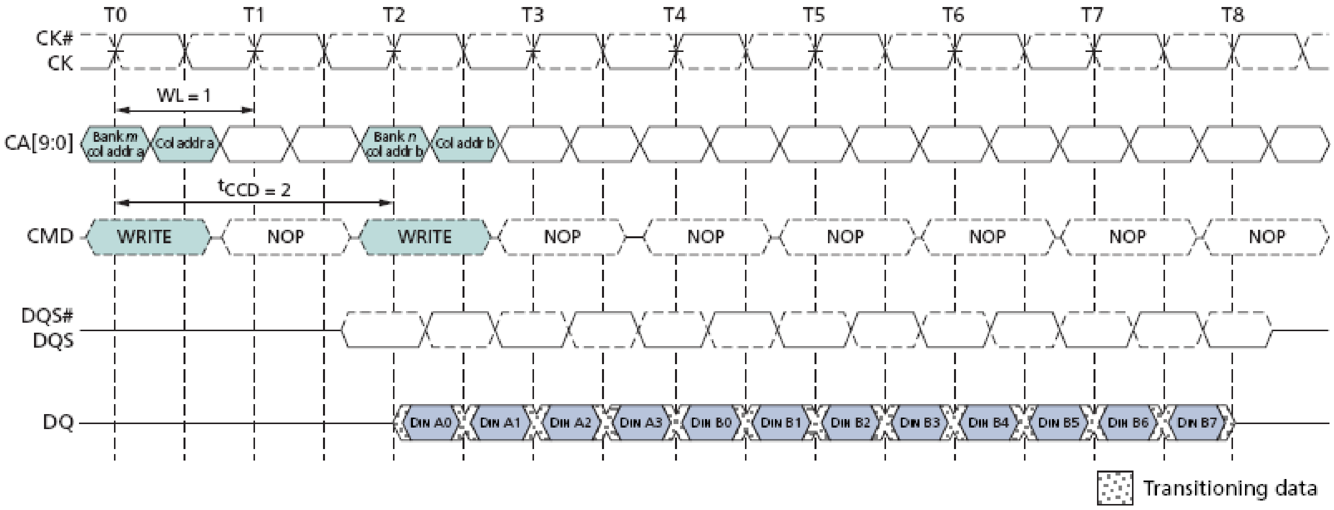


Seamless Burst write: WL=1, BL=4, Tccd=2

Notes:

1. The seamless burst write operation is supported by enabling a write command every other clock for BL=4 operation, every four clocks for BL=8 operation, or every eight clocks for BL=16 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Burst Write (Continued)



Write burst interrupt timing: WL=1, BL=8, Tccd=2

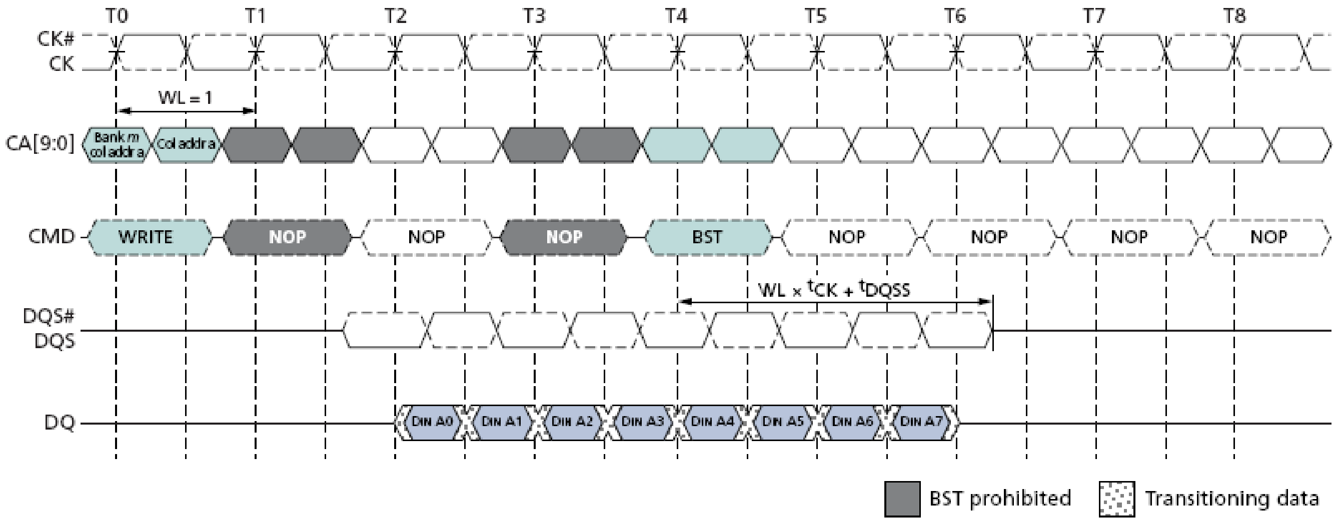
Notes:

1. WRITEs can only be interrupted by other WRITEs or the BST command.
2. For LPDDR2-S4 devices, write burst interrupt function is only allowed on burst of 8 and burst of 16.
3. For LPDDR2-S4 devices, write burst interrupt may only occur on even clock cycles after the previous write commands, provided that Tccd(min) is met.
4. Write burst interruption is allowed to any bank inside DRAM.
5. Write burst with Auto-Precharge is not allowed to be interrupted.
6. The effective burst length of the first WRITE equals two times the number of clock cycles between the first WRITE and the interrupting WRITE.

Burst Terminate [BST]

The BST command is initiated with $\overline{CS}$ LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 LOW at the rising edge of the clock. A BST command can only be issued to terminate an active READ or WRITE burst. Therefore, a BST command can only be issued up to and including BL/2 – 1 clock cycles after a READ or WRITE command. The effective burst length of a READ or WRITE command truncated by a BST command is as follows:

- Effective burst length = 2 × (number of clock cycles from the READ or WRITE command to the BST command).
- If a READ or WRITE burst is truncated with a BST command, to calculate the minimum READ-to-WRITE or WRITE-to-READ delay, the effective burst length of the truncated burst should be used as the value for BL.
- The BST command only affects the most recent READ or WRITE command. The BST command truncates an ongoing READ burst RL × Tck + Tdqsck + Tdqsq after the rising edge of the clock where the BST command is issued. The BST command truncates an on-going write burst WL × Tck + Tdqss after the rising edge of the clock where the BST command is issued.
- For LPDDR2-S4 devices, the 4-bit prefetch architecture enables BST command assertion on even clock cycles following a WRITE or READ command. The effective burst length of a READ or WRITE command truncated by a BST command is thus an integer multiple of 4.

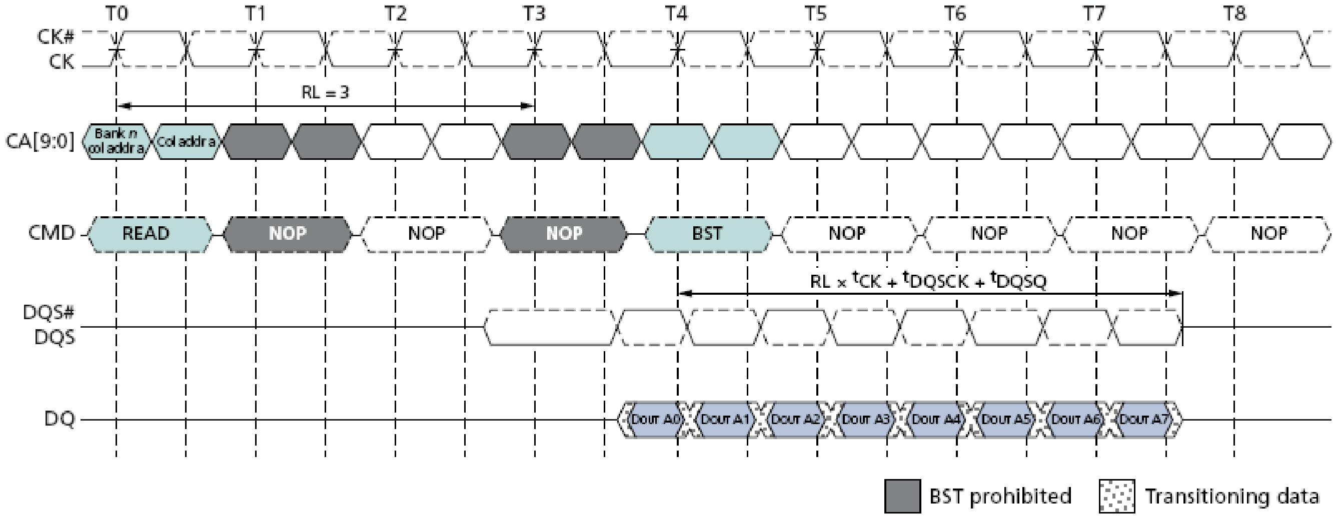


Burst Write truncated by BST: WL=1, BL=16

Notes:

1. The BST command truncates an ongoing write burst WL * ^{t}CK + ^{t}DQSS after the rising edge of the clock where the Burst Terminate command is issued.
2. For LPDDR2-S4 devices, BST can only be issued an even number of clock cycles after the Write command.
3. Additional BST commands are not allowed after T4, and may not be issued until after the next Read or Write command.

Burst Terminate [BST] (Continued)



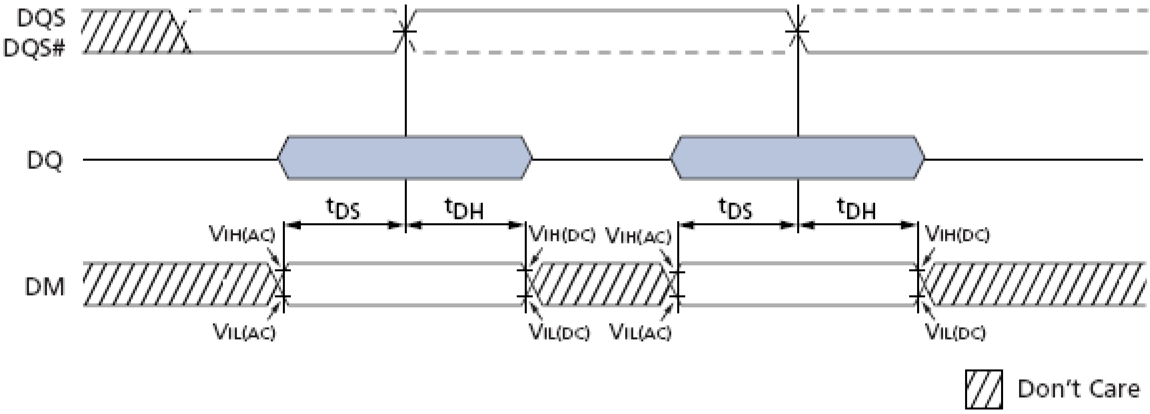
Burst Read truncated by BST: RL=3, BL=16

Notes:

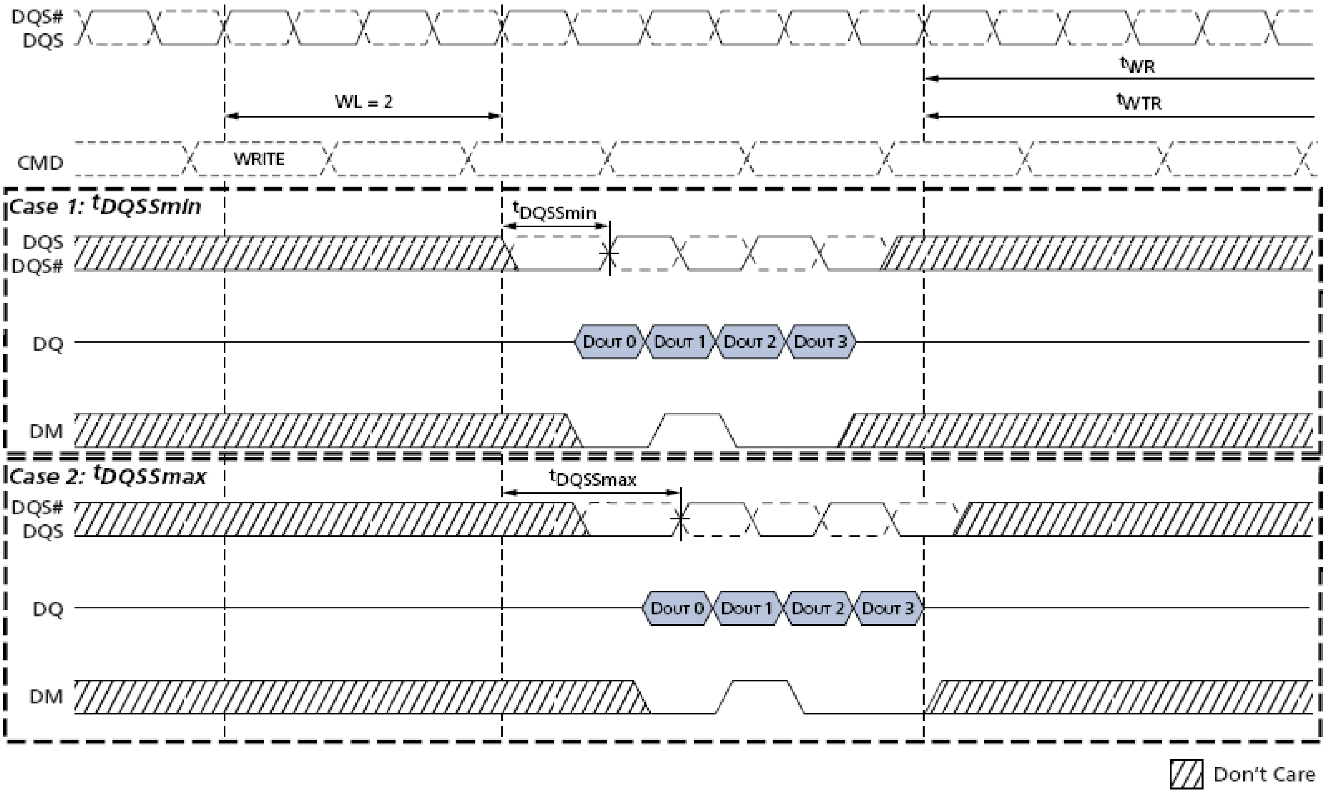
1. The BST command truncates an ongoing read burst RL * ^{t}CK + ^{t}DQSCK + ^{t}DQSQ after the rising edge of the clock where the Burst Terminate command is issued.
2. For LPDDR2-S4 devices, BST can only be issued an even number of clock cycles after the Read command.
3. Additional BST commands are not allowed after T4, and may not be issued until after the next Read or Write command.

Write data Mask

One write data mask (DM) pin for each data byte (DQ) will be supported on LPDDR2 devices, consistent with the implementation on LPDDR SDRAMs. Each data mask (DM) may mask its respective data byte (DQ) for any given cycle of the burst. Data mask has identical timings on write operations as the data bits, though used as input only, is internally loaded identically to data bits to insure matched system timing.



Data Mask Timing



Write data mask: WL=2, BL=4, second DQ masked

Notes: For the data mask function, WL=2, BL=4 is shown; the second data bit is masked.

Precharge

The Precharge command is used to precharge or close a bank that has been activated. The Precharge command is initiated by having CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. For 4-bank devices, the AB flag, and the bank address bits, BA0 and BA1, are used to determine which bank(s) to precharge. For 8-bank devices, the AB flag, and the bank address bits, BA0, BA1, and BA2, are used to determine which bank(s) to precharge. The bank(s) will be available for a subsequent row access $^tRP_{ab}$ after an All-Bank Precharge command is issued and $^tRP_{pb}$ after a Single-Bank Precharge command is issued.

In order to ensure that 8-bank devices do not exceed the instantaneous current supplying capability of 4-bank devices, the Row Precharge time (^tRP) for an All-Bank Precharge for 8-bank devices ($^tRP_{ab}$) will be longer than the Row Precharge time for a Single-Bank Precharge ($^tRP_{pb}$). For 4-bank devices, the Row Precharge time (^tRP) for an All-Bank Precharge ($^tRP_{ab}$) is equal to the Row Precharge time for a Single-Bank Precharge ($^tRP_{pb}$).

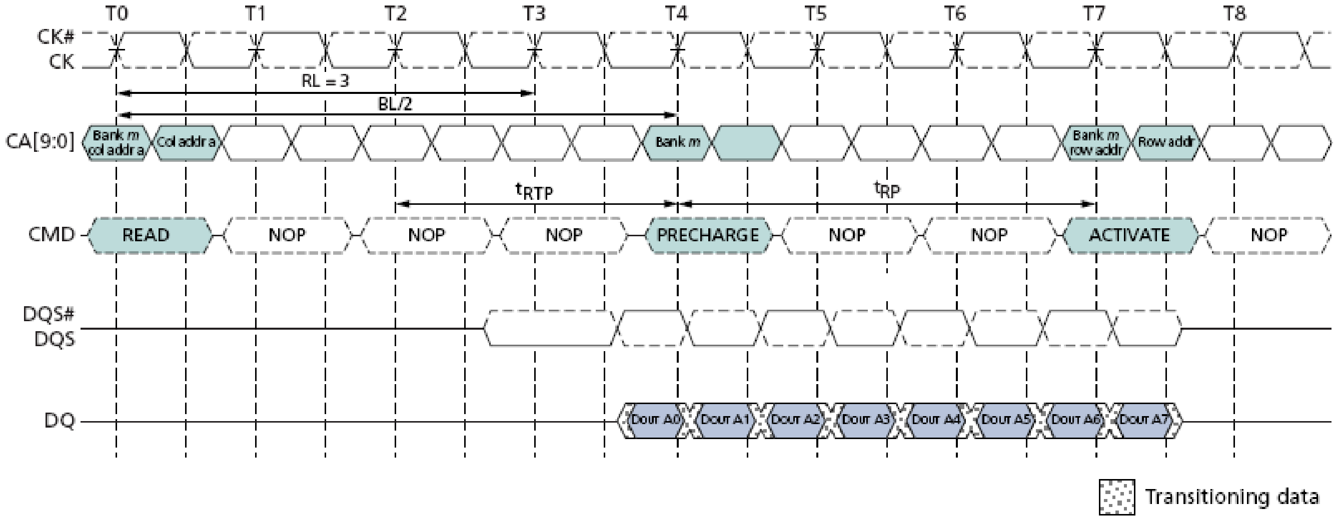
AB (CA4r)	BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s) 4-bank device	Precharged Bank(s) 8-bank device
0	0	0	0	Bank 0 only	Bank 0 only
0	0	0	1	Bank 1 only	Bank 1 only
0	0	1	0	Bank 2 only	Bank 2 only
0	0	1	1	Bank 3 only	Bank 3 only
0	1	0	0	Bank 0 only	Bank 4 only
0	1	0	1	Bank 1 only	Bank 5 only
0	1	1	0	Bank 2 only	Bank 6 only
0	1	1	1	Bank 3 only	Bank 7 only
1	Don't care	Don't care	Don't care	All Banks	All Banks

Bank selection for Precharge by address bits

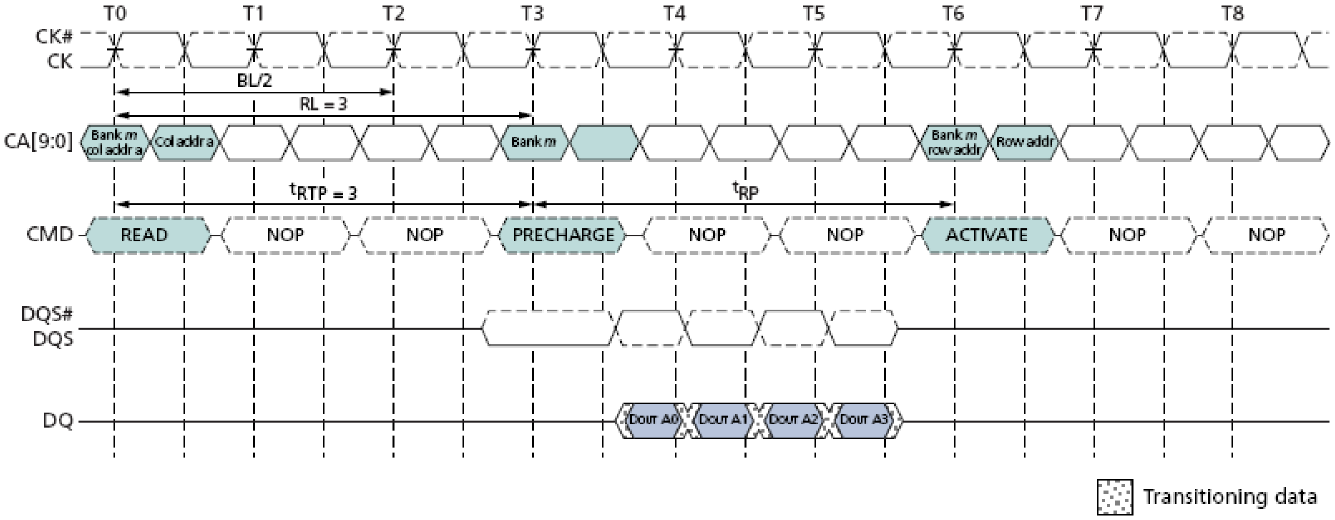
Burst Read followed by precharge

For the earliest possible precharge, the precharge command may be issued BL/2 clock cycles after a Read command. A new bank active (command) may be issued to the same bank after the Row Precharge time (^{t}RP). A precharge command can not be issued until after ^{t}RAS is satisfied.

For LPDDR2-S4 devices, the minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising cloak edge that initiates the last 4-bit precharge of a Read command. This time is called ^{t}RTP (Read to Precharge). For LPDDR2-S4 devices, ^{t}RTP begins BL/2 – 2 clock cycles after the Read command. If the burst is truncated by a BST command, the effective “BL” ahsll be used to calculate when ^{t}RTP begins.



Burst Read followed by Precharge: RL=3, BL=8, RU(^{t}RTP(min)/^{t}CK)=2



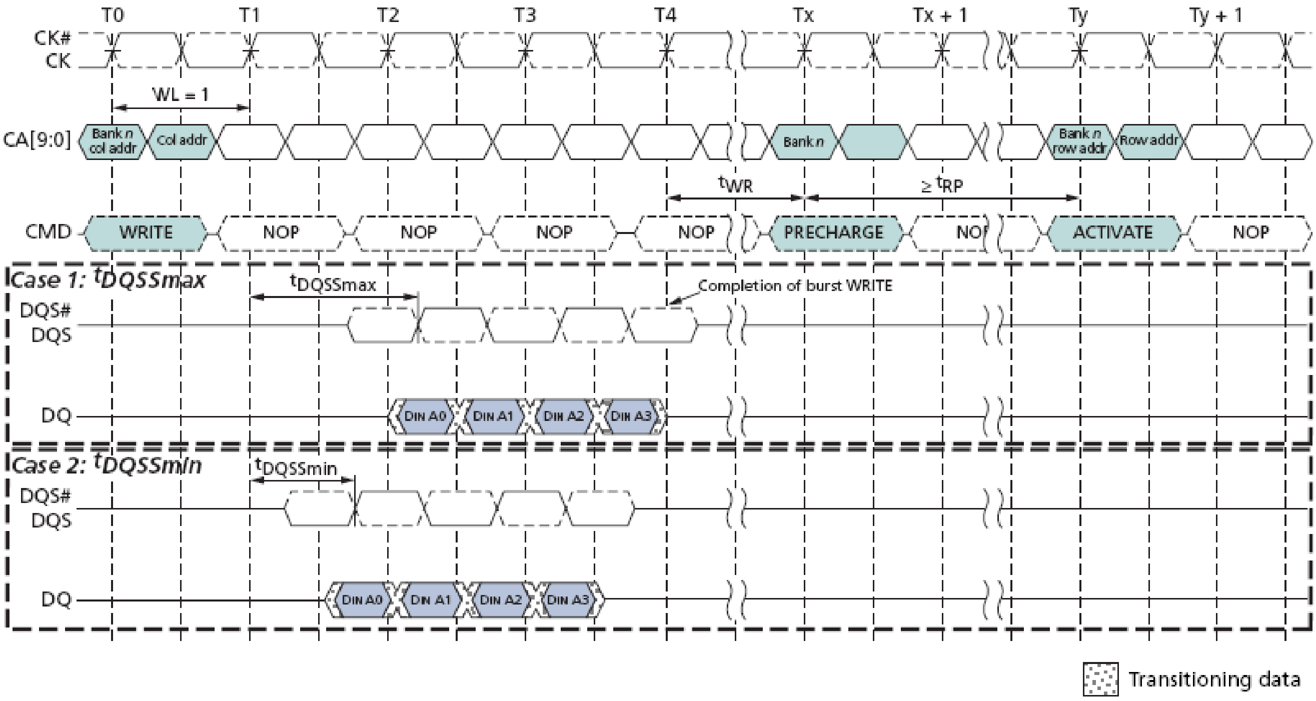
Burst Read followed by Precharge: RL=3, BL=4, RU(^{t}RTP(min)/^{t}CK) = 3

Burst Write followed by precharge

For write cycles, a delay must be satisfied from the time of the last valid burst input data until the Precharge command may be issued. This delay is known as the write recovery time (^{t}WR) referenced from the completion of the burst write to the Precharge command. No Precharge command to the same bank should be issued prior to the ^{t}WR delay.

LPDDR2-S2 devices write data to the array in prefetch pairs (prefetch = 2) and LPDDR2-S4 devices write data to the array in prefetch quadruples (prefetch = 4). The beginning of an internal write operation may only begin after a prefetch group has been completely. Therefore, the write recovery time (^{t}WR) starts different boundaries for LPDDR2-S2 and LPDDR2-S4 devices.

For LPDDR2-S2 devices, minimum Write to Precharge command spacing to the same bank is WL + RU(BL/2) + 1 + RU(^{t}WR/^{t}CK) clock cycles. For LPDDR2-S4 devices, minimum Write to Precharge command spacing to the same bank is WL + BL/2 + 1+ RU (^{t}WR/^{t}CK) clock cycles. For an untruncated burst, BL is the value from the Mode Register. For a truncated burst, BL is the effective burst length.



Burst Write followed by Precharge: WL=1, BL=4

Auto Precharge

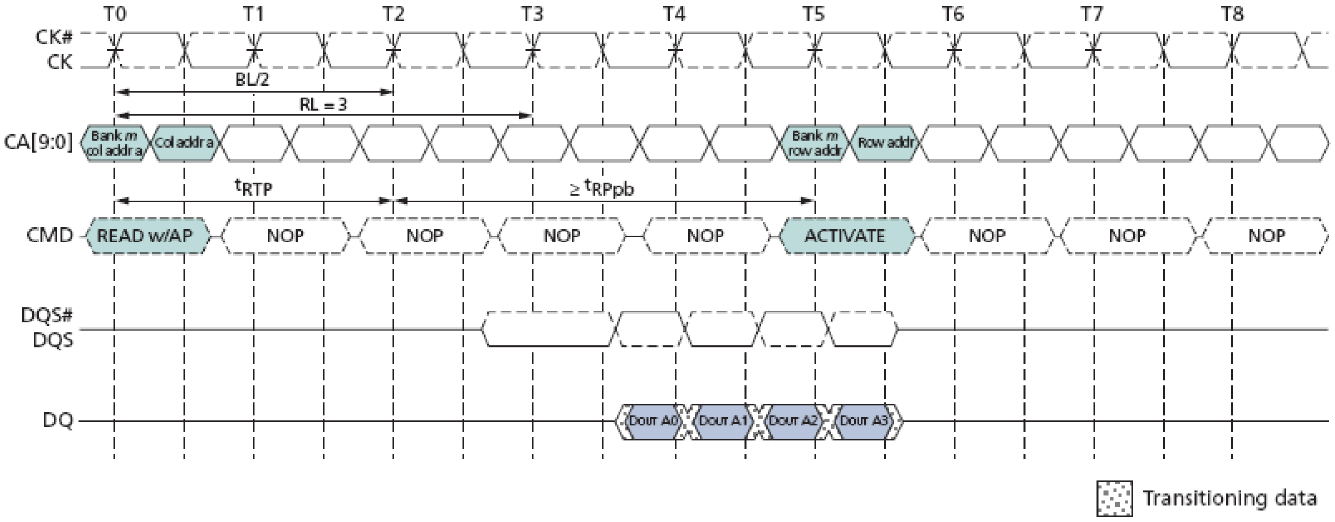
Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge command or the auto-precharge function. When a Read or a Write command is given to the LPDDR2 SDRAM, the AP bit (CA0f) may be set to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If AP is LOW when the Read or Write command is issued, the normal Read or Write burst operation is executed and the bank remains active at the completion of the burst. If AP is HIGH when the Read or Write command is issued, then the auto-precharge function is engaged. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon Read or Write latency) thus improving system performance for random data access.

Burst Read with Auto Precharge

If AP (CA0f) is HIGH when a Read Command is issued, the Read with Auto-Precharge function is engaged. LPDDR2-S4 devices start an Auto-Precharge operation on the rising edge of the clock BL/2 or BL/2 – 2 + RU(^{t}RTP/^{t}CK) clock cycles later than the Read with AP command, whichever is greater.

A new bank Activate command may be issued to the same bank if both of the following two conditions are satisfied simultaneously:

- The RAS precharge time (^{t}RP) has been satisfied from the clock at which the auto-precharge begins.
- The RAS cycle time (^{t}RC) from the previous bank activation has been satisfied.



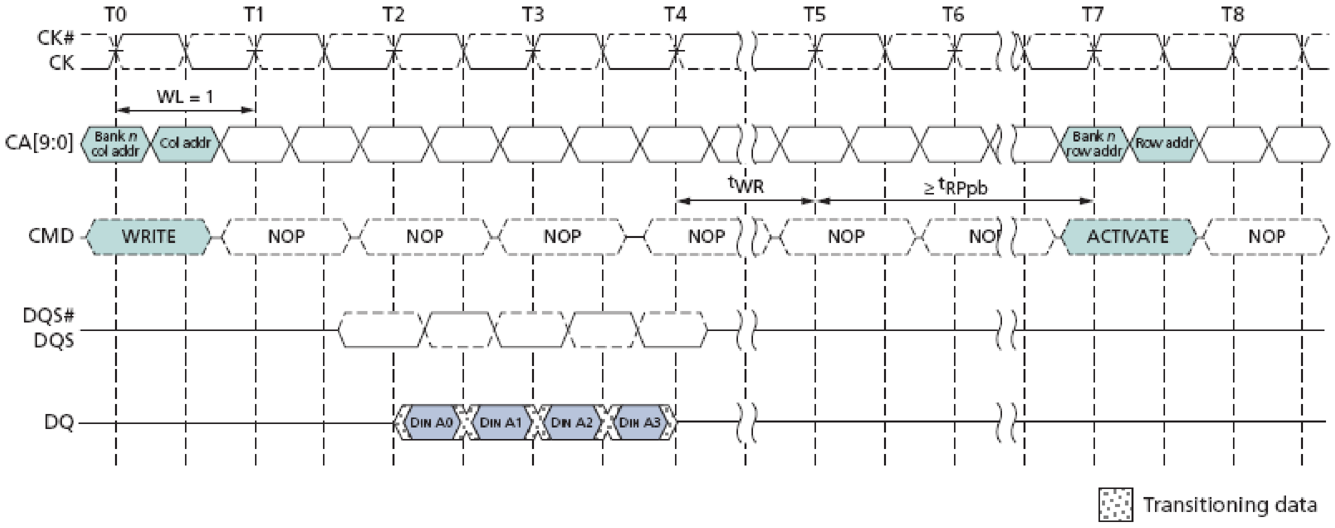
Burst Read with Auto-Precharge: RL=3, BL=4, RU(^{t}RTP(min)/^{t}CK)=2

Burst Write with Auto Precharge

If AP (CA0f) is HIGH when a Write Command is issued, the Write with Auto-Precharge function is engaged. The LPDDR2 SDRAM starts an Auto-precharge operation on the rising edge which is Twr cycles after the completion of the burst write.

A new bank Activate command may be issued to the same bank if both of the following two conditions are satisfied:

- The RAS precharge time (Trp) has been satisfied from the clock at which the auto-precharge begins.
- The RAS cycle time (Trc) from the previous bank activation has been satisfied.



Burst Write with Auto-Precharge: WL=1, BL=4

LPDDR2-S4: Precharge & Auto Precharge clarification

From Command	To Command	Minimum Delay between "From Command" to "To Command"	Unit	Notes
Read	Precharge (to same Bank as Read)	BL/2 + max(2, RU(^{t}RTP/^{t}CK)) - 2	clks	1
	Precharge All	BL/2 + max(2, RU(^{t}RTP/^{t}CK)) - 2	clks	1
BST (for Reads)	Precharge (to same Bank as Read)	1	clks	1
	Precharge All	1	clks	1
Read w/AP	Precharge (to same Bank as Read w/AP)	BL/2 + max(2, RU(^{t}RTP/^{t}CK)) - 2	clks	1,2
	Precharge All	BL/2 + max(2, RU(^{t}RTP/^{t}CK)) - 2	clks	1
	Activate (to same Bank as Read w/AP)	BL/2 + max(2, RU(^{t}RTP/^{t}CK)) - 2 + RU(^{t}RP/^{t}CK)	clks	1
	Write or Write w/AP (same bank)	illegal	clks	3
	Write or Write w/AP (different bank)	RL + BL/2 + RU(^{t}DQSCKmax/^{t}CK) - WL + 1	clks	3
	Read or Read w/AP (same bank)	illegal	clks	3
	Read or Read w/AP (different bank)	BL/2	clks	3
Write	Precharge (to same Bank as Write)	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	clks	1
	Precharge All	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	clks	1
BST (for Writes)	Precharge (to same Bank as Write)	WL + RU(^{t}WR/^{t}CK) + 1	clks	1
	Precharge All	WL + RU(^{t}WR/^{t}CK) + 1	clks	1
Write w/AP	Precharge (to same Bank as Write w/AP)	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	clks	1
	Precharge All	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	clks	1
	Activate (to same Bank as Write w/AP)	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1 + RU(^{t}RP$_{pb}$/^{t}CK)	clks	1
	Write or Write w/AP (same bank)	illegal	clks	3
	Write or Write w/AP (different bank)	BL/2	clks	3
	Read or Read w/AP (same bank)	illegal	clks	3
	Read or Read w/AP (different bank)	WL + BL/2 + RU(^{t}WTR/^{t}CK) + 1	clks	3
Precharge	Precharge (to same Bank as Precharge)	1	clks	1
	Precharge All	1	clks	1
Precharge All	Precharge	1	clks	1
	Precharge All	1	clks	1

Notes:

1. For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after ^{t}RP depending on the latest precharge command issued to that bank.
2. Any command issued during the minimum delay time as specified above table is illegal.
3. After Read with AP, seamless read operations to different banks are supported. After Write with AP, seamless write operations to different banks are supported. Read w/AP and Write a/AP may not be interrupted or truncated.

Refresh Command

The Refresh Command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of clock. Per Bank Refresh is initiated by having CA3 LOW at the rising edge of the clock and All Bank Refresh is initiated by having CA3 HIGH at the rising edge of clock. Per Bank Refresh is only allowed in devices with 8 banks.

A Per Bank Refresh Command, REFpb performs a refresh operation to the bank which is scheduled by the bank counter in the memory device. The bank sequence of Per Bank Refresh is fixed to be a sequential round-robin: “0-1-2-3-4-5-6-7-0-1-…”. The bank count is synchronized between the controller and the SDRAM upon issuing a RESET command or at every exit from self refresh, by resetting bank count to zero. The bank addressing for the Per Bank Refresh count is the same as established in the single-bank Precharge command.

A bank must be idle before it can be refreshed. It is the responsibility of the controller to track the bank being refreshed by the Per Bank Refresh command. The REFpb command may not be issued to the memory until the following conditions are met:
- tRFCab has been satisfied after the prior REFab command.
- tRFCpb has been satisfied after the prior REFpb command.
- Trp has been satisfied after the prior Precharge command to that given bank.

Trrd has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than affected by the REFpb command. The target bank is inaccessible during the Per Bank Refresh cycle (tRFCpb), however other banks within the device are accessible and may be addressed during the Per Bank Refresh cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in active state or accessed by a read or a write command.

When the Per Bank Refresh cycle has completed, the affected bank will be in the idle state. As shown in the table, after issuing REFpb:
- tRFCpb must be satisfied before issuing a REFab command.
- tRFCpb must be satisfied before issuing an ACTIVE command to a same bank.
- Trrd must be satisfied before issuing an ACTIVE command to a different bank.
- tRFCpb must be satisfied before issuing another REFpb command.

An All Bank Refresh command, REFab performs a refresh operation to all banks. All banks have to be in idle state when REFab is issued (for instance, by Precharge All Bank command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. As shown in the table, the REFab command may not be issued to the memory until the following conditions have been met:
- tRFCab has been satisfied after the prior REFab command.
- tRFCpb has been satisfied after the prior REFpb command.
- Trp has been satisfied after the prior Precharge commands.

When the All Bank Refresh cycle has completed, all banks will be in the idle state. As shown in the table, after issuing REFab:
- the tRFCab latency must be satisfied before issuing an ACTIVATE command.
- the tRFCab latency must be satisfied before issuing a REFab or REFpb command.

Command Scheduling Separations related to Refresh			
Symbol	**minimum delay from**	**to**	**Notes**
^{t}RFC$_{ab}$	REF$_{ab}$	REF$_{ab}$	
		Activate cmd to *any* bank .	
		REF$_{pb}$	
^{t}RFC$_{pb}$	REF$_{pb}$	REF$_{ab}$	
		Activate cmd to *same* bank as REF$_{pb}$	
		REF$_{pb}$	
^{t}RRD	REF$_{pb}$	Activate cmd to *different* bank than REF$_{pb}$	
	Activate	REF$_{pb}$ affecting an idle bank (different bank than Activate)	1
		Activate cmd to *different* bank than prior Activate	

Notes:

1. A bank must be in the idle state before it is refreshed. Therefore, after Activate, REFab is not allowed and REFpb is allowed only if it affects a bank which is in the idle state.

Refresh Requirement

(1) Minimum number of Refresh commands:

LPDDR2 requires a minimum number, R, of REFRESH (REFab) commands within any rolling refresh window (Trefw = 32 ms @ MR4[2:0] = 011 or TC ≤ 85°C). For actual values per density, and the resulting average refresh interval (Trefi) is given in the table below.

Symbol	**Parameter**	**4Gb**	**8Gb**	**Unit**
	Number of banks	8		
Trefw	Refresh window: TCASE ≤ 85°	32		ms
Trefw	Refresh window: 85°C < TCASE ≤ 105°C	8		ms
R	Required number of REFRESH commands (MIN)	8192	8192	
Trefi	Average time between REFRESH commands (for reference only) TCASE ≤ 85°C	3.9	3.9	us
tREFIpb		0.4875	0.4875	us
tRFCab	Refresh cycle time	130	210	ns
tRFCpb	Per-bank REFRESH cycle time	60	90	ns
Trefbw	Burst REFRESH window = 4 × 8 × tRFCab	4.16	6.72	us

And see Mode Register 4 information for Trefw and Trefi refresh multipliers at different MR4 settings.

For devices supporting per-bank REFRESH, a REFab command can be replaced by a full cycle of eight REFpb commands.

Refresh Requirement (Continued)

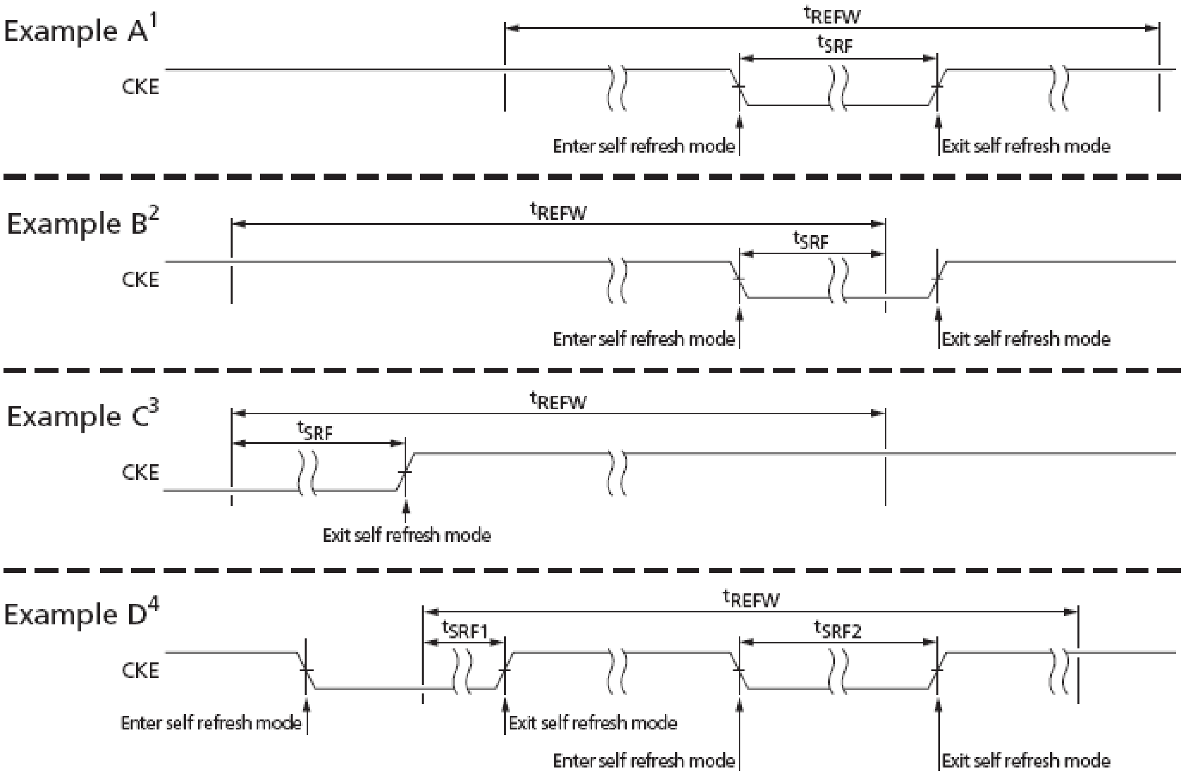
(2) Burst Refresh limitation:

To limit maximum current consumption, a maximum of 8 REFab commands may be issued in any rolling Trefbw (Trefbw = 4 x 8 x tRFCab). This condition does not apply if REFpb commands are used.

(3) Refresh Requirements and Self-Refresh:

If any time within a refresh window is spent in Self-Refresh Mode, the number of required Refresh commands in this particular window is reduced to:

R*=R – RU{Tsrf/Trefi} =R-RU{R*Tsrf/Trefw }, where RU stands for the round-up function.



LPDDR2 S4: Definition of Tsrf

NOTE: Above examples are several cases on how to Tsrf is calculated

1. (Example A): Time in self refresh mode is fully enclosed in the refresh window (Trefw)
2. (Example B): At self refresh entry.
3. (Example C): At self refresh exit.
4. (Example D): Several intervals in self refresh during one Trefw interval. In this example, Tsrf = Tsrf1 + Tsrf2.

Refresh Requirement (Continued)

The LPDDR2 devices provide significant flexibility in scheduling REFRESH commands as long as the boundary conditions are met. In the most straightforward implementations, a REFRESH command should be scheduled every Trefi. In this case, self refresh can be entered at any time.

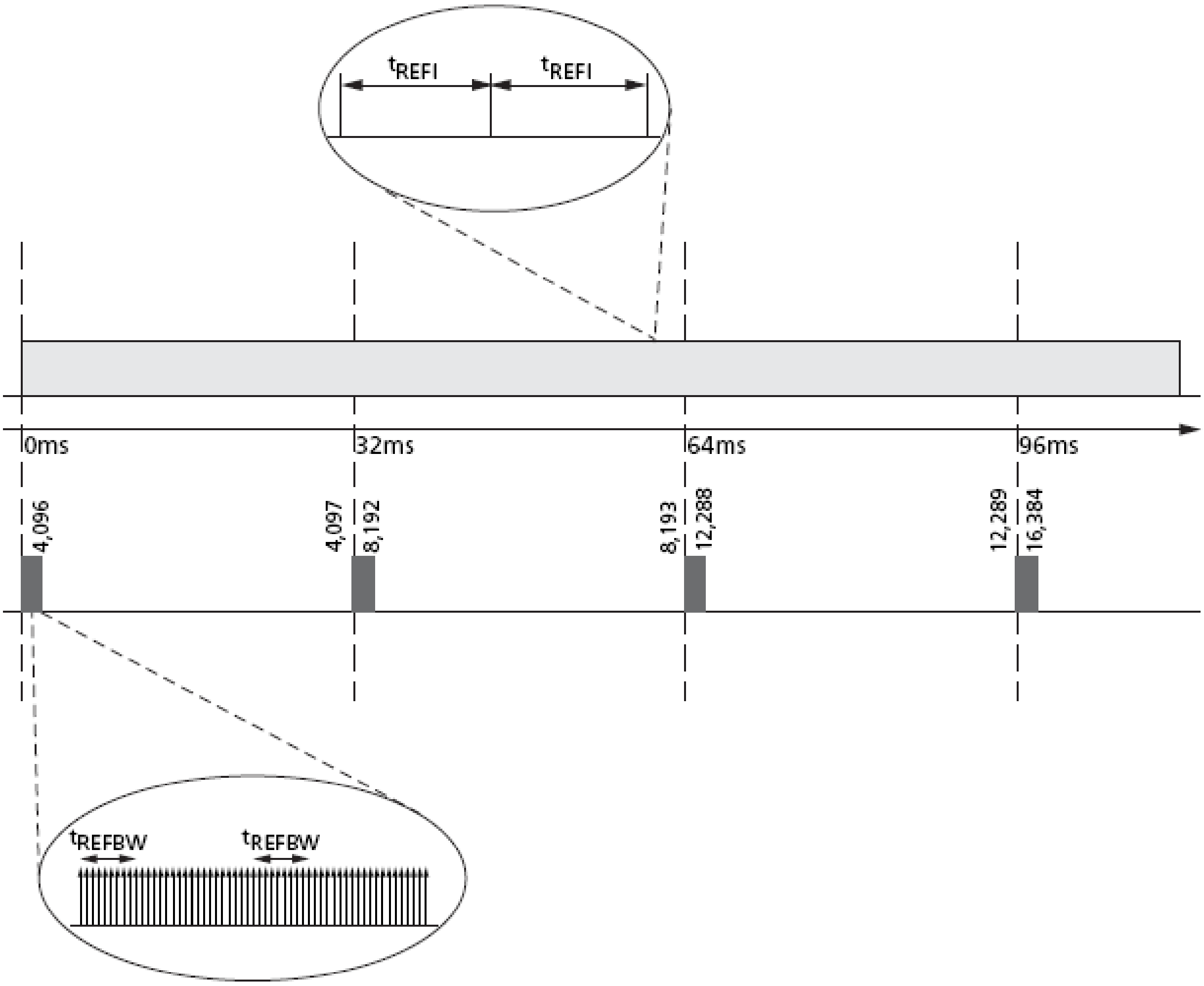
Users may choose to deviate from this regular refresh pattern, for example, to enable a period where no refreshes are required. In the extreme (e.g., LPDDR2-S4 1Gb), the user can choose to issue a refresh burst of 4096 REFRESH commands at the maximum supported rate (limited by Trefbw), followed by an extended period without issuing any REFRESH commands, until the refresh window is complete. The maximum supported time without REFRESH commands is calculated as follows: Trefw – (R/8) × Trefbw = Trefw – R × 4 × tRFCab.

For example, a 1Gb LPDDR2-S4 device at TC ≤ 85°C can be operated without REFRESH commands up to 32ms – 4096 × 4 × 130ns ≈ 30 ms. Both the regular and the burst/pause patterns can satisfy refresh requirements if they are repeated in every 32ms window. It is critical to satisfy the refresh requirement in every rolling refresh window during refresh pattern transitions. The supported transition from a burst pattern to a regular distributed pattern. If this transition occurs immediately after the burst refresh phase, all rolling Trefw intervals will meet the minimum required number of refreshes.

A non-supported transition –In this example, the regular refresh pattern starts after the completion of the pause phase of the burst/pause refresh pattern. For several rolling Trefw intervals, the minimum number of REFRESH commands is not satisfied.

Understanding this pattern transition is extremely important, even when only one pattern is employed. In self refresh mode, a regular distributed-refresh pattern must be assumed. It is recommended entering self refresh mode immediately following the burst phase of a burst/pause refresh pattern; upon exiting self refresh, begin with the burst phase.

Refresh Requirement (Continued)

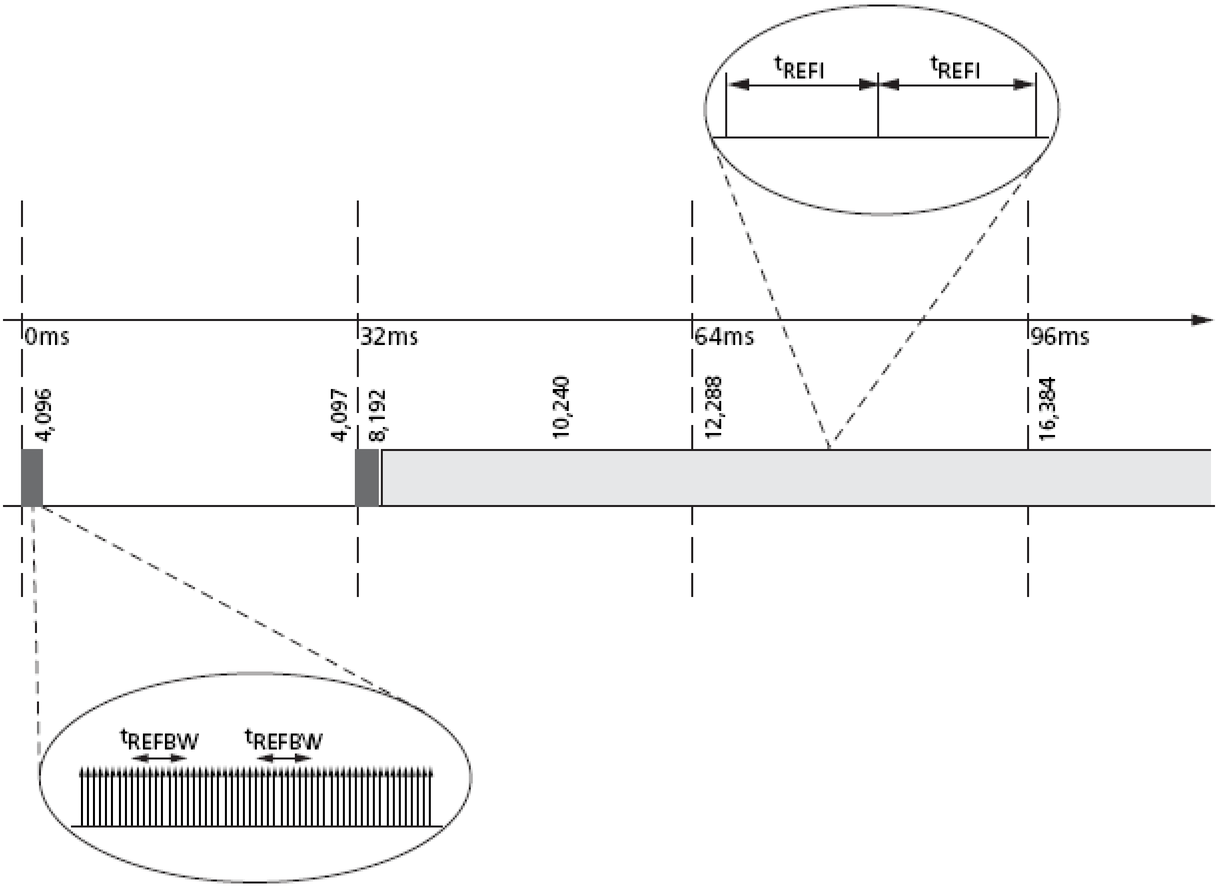


Regular, Distributed REFRESH Pattern

Notes:

1. Compared to repetitive burst REFRESH with subsequent REFRESH pause.
2. As an example, in a 1Gb LPDDR2-S4 device at TC ≤ 85°C, the distributed refresh pattern has one REFRESH command per 7.8µs; the burst refresh pattern has one refresh command per 0.52µs, followed by ≈ 30ms without any REFRESH command.

Refresh Requirement (Continued)

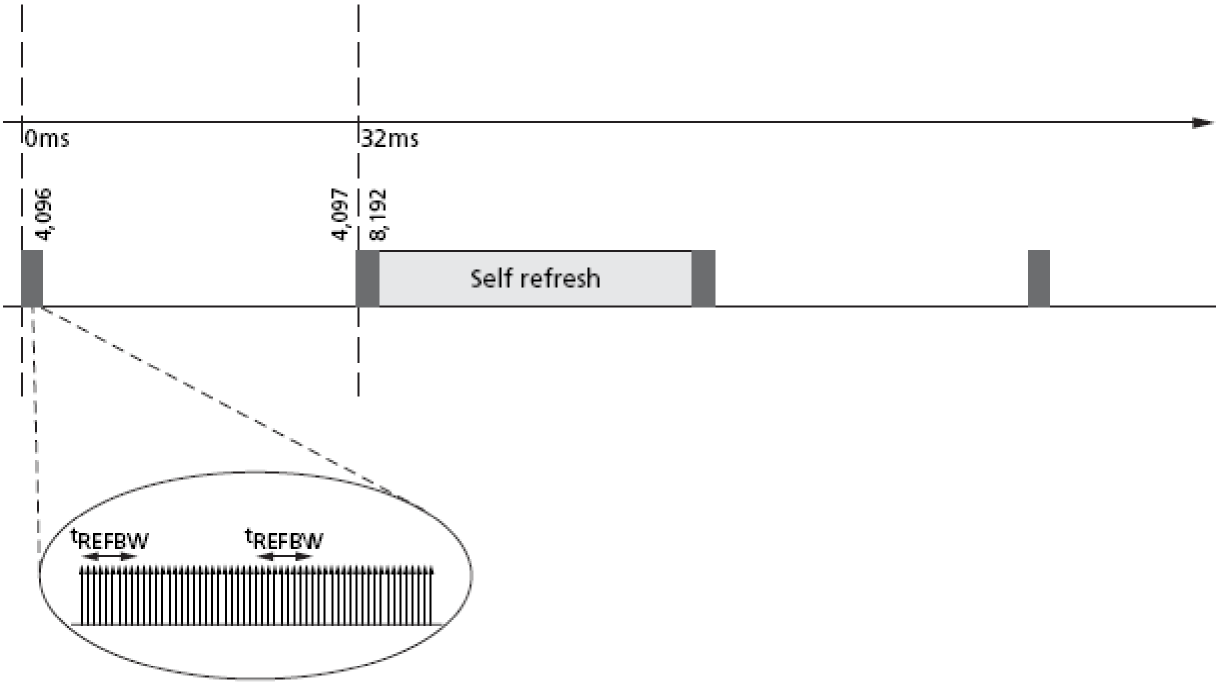


Supported Transition from Repetitive Burst REFRESH

Notes:

1. Shown with subsequent REFRESH pause to regular, distributed-refresh pattern.
2. As an example, in a 1Gb LPDDR2-S4 device at TC ≤ 85°C, the distributed refresh pattern has one REFRESH command per 7.8µs; the burst refresh pattern has one refresh command per 0.52µs, followed by ≈ 30ms without any REFRESH command.

Refresh Requirement (Continued)

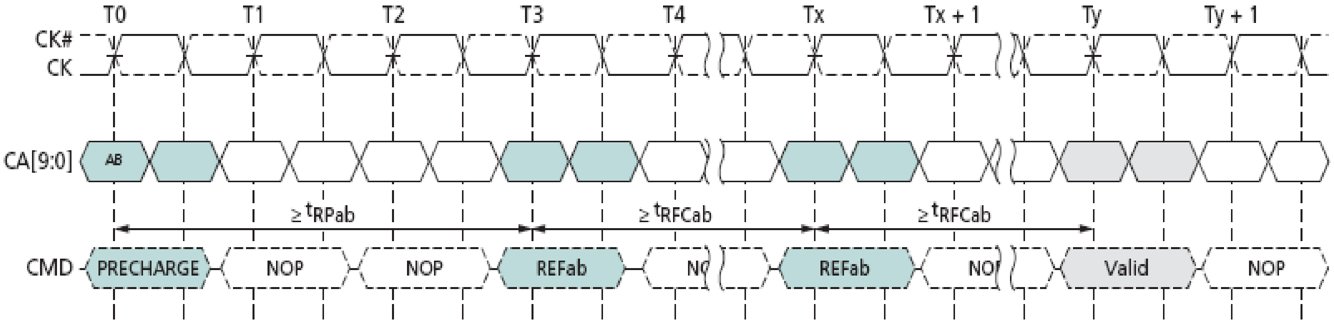


Recommended Self Refresh Entry and Exit

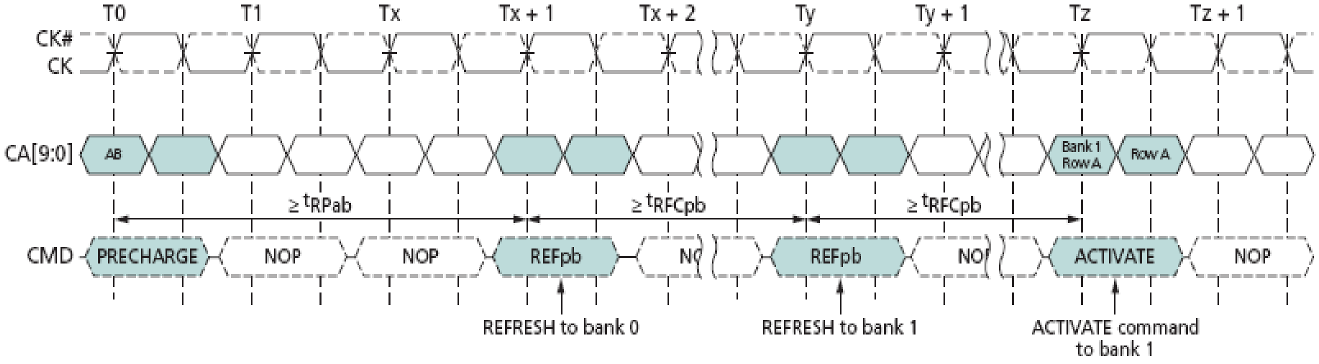
Notes:

4. In conjunction with a burst/pause refresh pattern.

Refresh Requirement (Continued)



All Bank Refresh Operation



Per-Bank Refresh Operation

Notes:

1. In the beginning of this example, the REFpb bank is pointing to Bank 0.
2. Operations to other banks than the bank being refreshed are allowed during the tREFpb period.

Self Refresh Operation

The Self Refresh command can be used to retain data in the LPDDR2 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the LPDDR2 SDRAM retains data without external clocking. The LPDDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having CKE LOW, CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. CKE must be HIGH during the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. Once the command is registered, CKE must be held LOW to keep the device in Self Refresh mode.

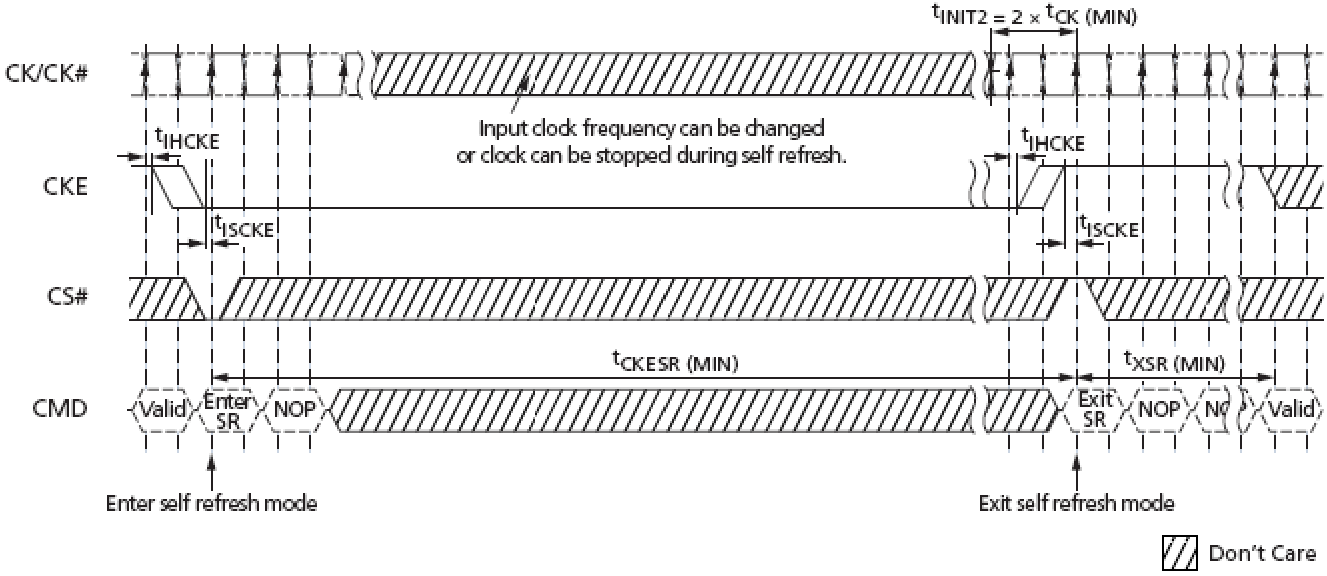
LPDDR2-S4 devices can operate in Self Refresh in both the Standard or Extended Temperature Ranges. LPDDR2-S4 devices will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperature and higher at high temperature.

Once the LPDDR2 SDRAM has entered Self Refresh mode, all of the external signals except CKE, are “don’t care”. For proper self refresh operation, power supply pins (VDD1, VDD2, and VDDCA) must be at valid levels. VDDQ may be turned off during Self-Refresh. Prior to exiting Self-Refresh, VDDQ must be within specified limits. VrefQD and VrefCA may be at any level within minimum and maximum levels. However prior to exiting Self-Refresh, VrefDQ and VrefCA must be within specified limits. The SDRAM initiates a minimum of one all-bank refresh command internally within Tckesr period, once it enters Self Refresh mode. The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the LPDDR2 SDRAM must remain in Self Refresh mode is Tckesr. The user may change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit Self Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock shall be stable and within specified limits for a minimum of 2 clock cycles prior to CKE going back HIGH. Once Self Refresh Exit is registered, a delay of at least Txsr must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period Txsr for proper operation except for self refresh re-entry. NOP commands must be registered on each positive clock edge during the Self Refresh exit interval Txsr.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, it is required that at least one Refresh command (8 per-bank or 1 all-bank) is issued before entry into a subsequent Self Refresh.

Self Refresh Operation (Continued)



Self Refresh Operation

Notes:

1. Input clock frequency may be changed or stopped during self-refresh, provided that upon exiting self-refresh, a minimum of 2 clocks (Tinit2) of stable clock are provided and the clock frequency is between the minimum and maximum frequency for the particular speed grade.
2. Device must be in the “All banks idle” state prior to entering Self Refresh mode.
3. Txsr begins at the rising edge of the clock after CKE is driven HIGH.
4. A valid command may be issued only after Txsr is satisfied. NOPs shall be issued during Txsr.

Partial Array Self-Refresh: Bank Masking

LPDDR2-S4 SDRAM has 4 or 8 banks. For LPDDR2-S4 devices, 64Mb to 512Mb LPDDR2 SDRAM has 4 banks, while 1Gb and higher density has 8. Each bank of LPDDR2 SDRAM can be independently configured whether a self refresh operation is taking place. One mode register unit of 8 bits accessible via MRW command is assigned to program the bank masking status of each bank up to 8 banks. For bank masking bit assignments, see Mode Register 16.

The mask bit to the bank controls a refresh operation of entire memory within the bank. If a bank is masked via MRW, a refresh operation to entire bank is not blocked and data retention by a bank is not guaranteed in self refresh mode. To enable a refresh operation to a bank, a coupled mask bit has to be programmed, “unmasked”. When a bank mask bit is unmasked, the array space being refreshed within that bank is determinate by the programmed status of the segment mask bit.

Partial Array Self-Refresh: Segment Masking

Segment Programming segment mask bits is similar to programming bank mask bits. For densities 1Gb and higher, 8 segments are used for masking. Mode register 17 is used for programming segment mask bits up to 8 bits. For densities less than 1Gb, segment masking is not supported.

When the mask bit to an address range (represented as a segment) is programmed as "masked," a REFRESH operation to that segment is blocked. Conversely, when a segment mask bit to an address range is unmasked, refresh to that segment is enabled. A segment-masking scheme can be used in place of or in combination with a bank masking scheme in LPDDR2-S4 SDRAM. Each segment-mask bit setting is applied across all banks.

	Segment Mask (MR17)	**Bnak 0**	**Bank 1**	**Bank 2**	**Bank 3**	**Bnak 4**	**Bank 5**	**Bank 6**	**Bank 7**
Bank Mask (MR16)		0	1	0	0	0	0	0	1
Segment 0	0		M						M
Segment 1	0		M						M
Segment 2	1	M	M	M	M	M	M	M	M
Segment 3	0		M						M
Segment 4	0		M						M
Segment 5	0		M						M
Segment 6	0		M						M
Segment 7	1	M	M	M	M	M	M	M	M

Example of Bank and Segment Masking use in LPDDR2-S4 devices

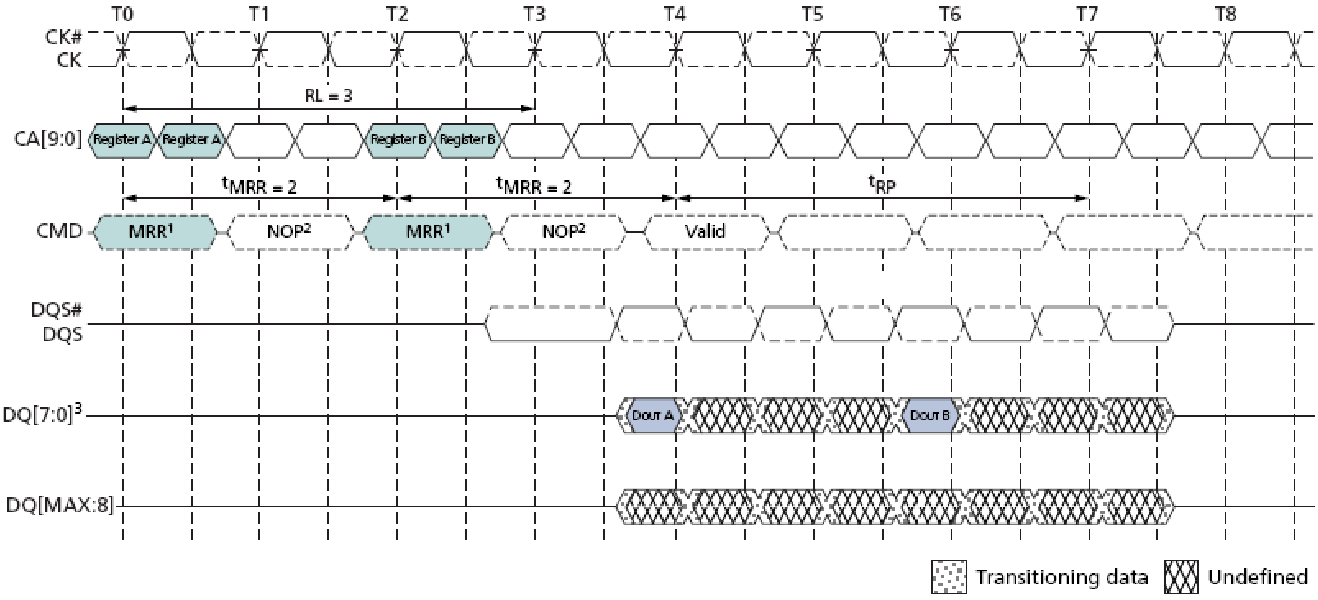
Notes:

1. This table illustrates an example of an 8-bank LPDDR2-S4 device, when a refresh operation to bank 1 and bank 7, as well as segment 2 and segment 7 are masked.

Mode Register Read Command

The Mode Register Read command is used to read configuration and status data from mode registers for LPDDR SDRAM. The Mode Register Read (MRR) command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r-CA4r}. The mode register contents are available on the first data beat of DQ0-DQ7, RL * Tck + Tdqsck + Tdqsq after the rising edge of the clock where the Mode Register Read Command is issued. Subsequent data beats contain valid, but undefined content, except in the case of the DQ Calibration function DQC, where subsequent data beats contain valid content as described in "DQ Calibration". All DQS shall be toggled for the duration of the Mode Register Read burst. The MRR command has a burst length of four. The Mode Register Read operation (consisting of the MRR command and the corresponding data traffic) shall not be interrupted. The MRR command period (Tmrr) is 2 clock cycles. Mode Register Reads to reserved and write-only registers shall return valid, but undefined content on all data beats and DQS shall be toggled.

Mode Register Read Command (Continued)



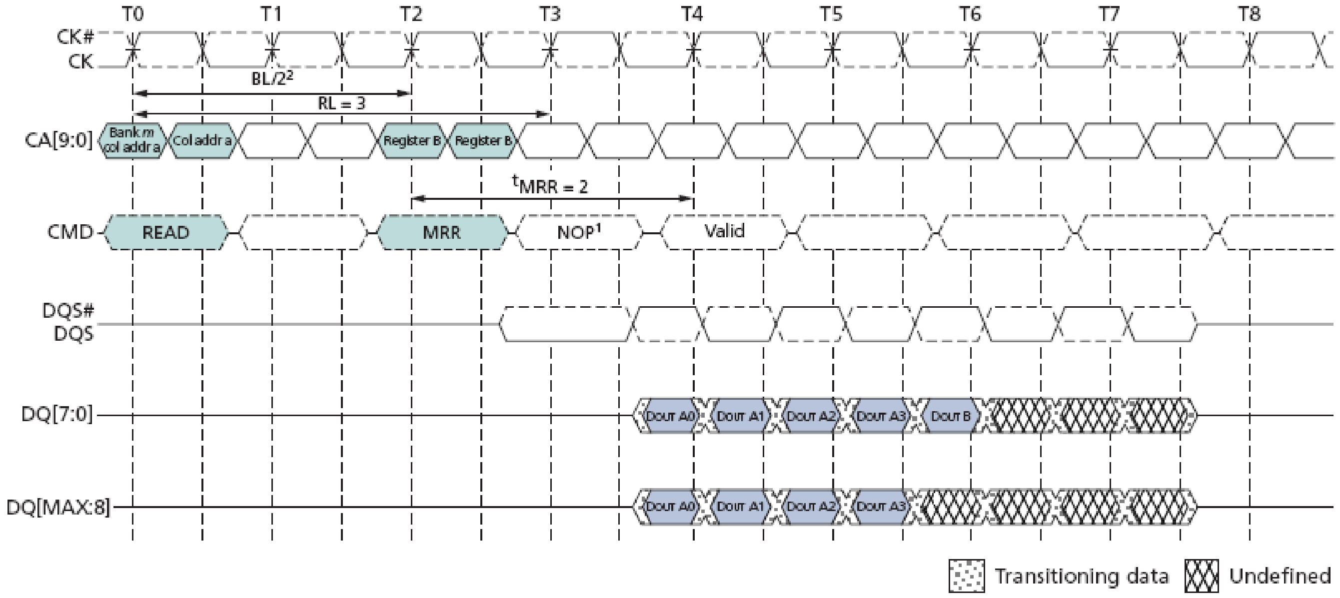
Mode Register Read timing example: RL=3, Tmrr=2

Notes:

1. Mode Register Read has a burst length of four
2. Mode Register Read operation shall not be interrupted
3. MRRs to DQ calibration registers MR32 and MR40 are described in “DQ Calibration”.
4. Only the NOP command is supported during Tmrr.
5. Mode register data is valid only on DQ[7:0] on the first beat. Subsequent beats contain valid but undefined data.
   DQ[MAX:8] contain valid but undefined data for the duration of the MRR burst.
6. Minimum Mode Register Read to write latency is RL+RU(Tdqsck,max/Tck)+4/2+1-WL clock cycles
7. Minimum Mode Register Read to Mode Register Write Latency is RL+RU(Tdqsck,max/Tck)+4/2+1 clock cycles

After a prior READ command, the MRR command must not be issued earlier than BL/2 clock cycles, or WL + 1 + BL/2 + RU(Twtr/Tck) clock cycles after a prior WRITE command, as READ bursts and WRITE bursts must not be truncated by MRR. Note that if a READ or WRITE burst is truncated with a BST command, the effective burst length of the truncated burst should be used for the value BL.

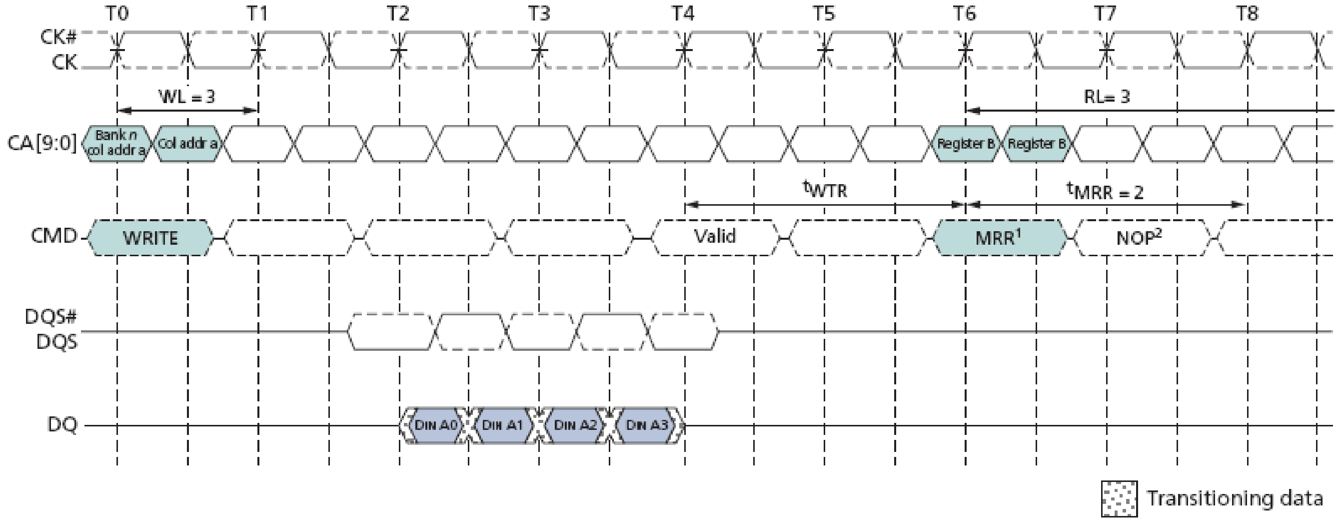
Mode Register Read Command (Continued)



Read to MRR timing example: RL=3, Tmrr=2

Notes:

1. The minimum number of clocks from the burst read command to the Mode Register Read command is BL/2.
2. Only the NOP command is supported during Tmrr.



Burst Write Followed by MRR: RL=3, WL=1, BL=4

Notes:

1. The minimum number of clock cycles from the burst write command to the Mode Register Read command is [WL + 1 + BL/2 + RU(Twtr/Tck)].
2. Only the NOP command is supported during Tmrr.

Temperature Sensor

LPDDR2 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing derating is required in the extended temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device operating temperature can be used to determine if operating temperature requirements are being met.

Temperature sensor data may be read from MR4 using the Mode Register Read protocol.

When using the temperature sensor, the actual device case temperature may be higher than the operating temperature specification that applies for the standard or extended temperature ranges. For example, TCASE could be above 85°C when MR4[2:0] equals 011B.

To assure proper operation using the temperature sensor, applications must accommodate the specifications shown in bellow.

Temperature Sensor Definitions and Operating Considerations

Parameter	Symbol	Max/Min	Value	Unit	Notes
System Temperature Gradient	TempGradient	Max	System Dependent	C/s	Maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2°C.
MR4 Read Interval	ReadInterval	Max	System Dependent	ms	Time period between MR4 READs from the system.
Temperature Sensor Interval	^{t}TSI	Max	32	ms	Maximum delay between internal updates of
System Response Delay	SysRespDelay	Max	System Dependent	ms	Maximum response time from an MR4 READ to the system response.
Device Temperature Margin	TempMargin	Max	2	C	Margin above maximum temperature to support controller response.

These devices accommodate the 2 degree Celsius temperature margin between the point at which the device temperature enters the extended temperature range and point at which the controller re-configures the system accordingly. To determine the required MR4 polling frequency, the system must use the maximum TempGradient and the maximum response time of the system using the following equation:

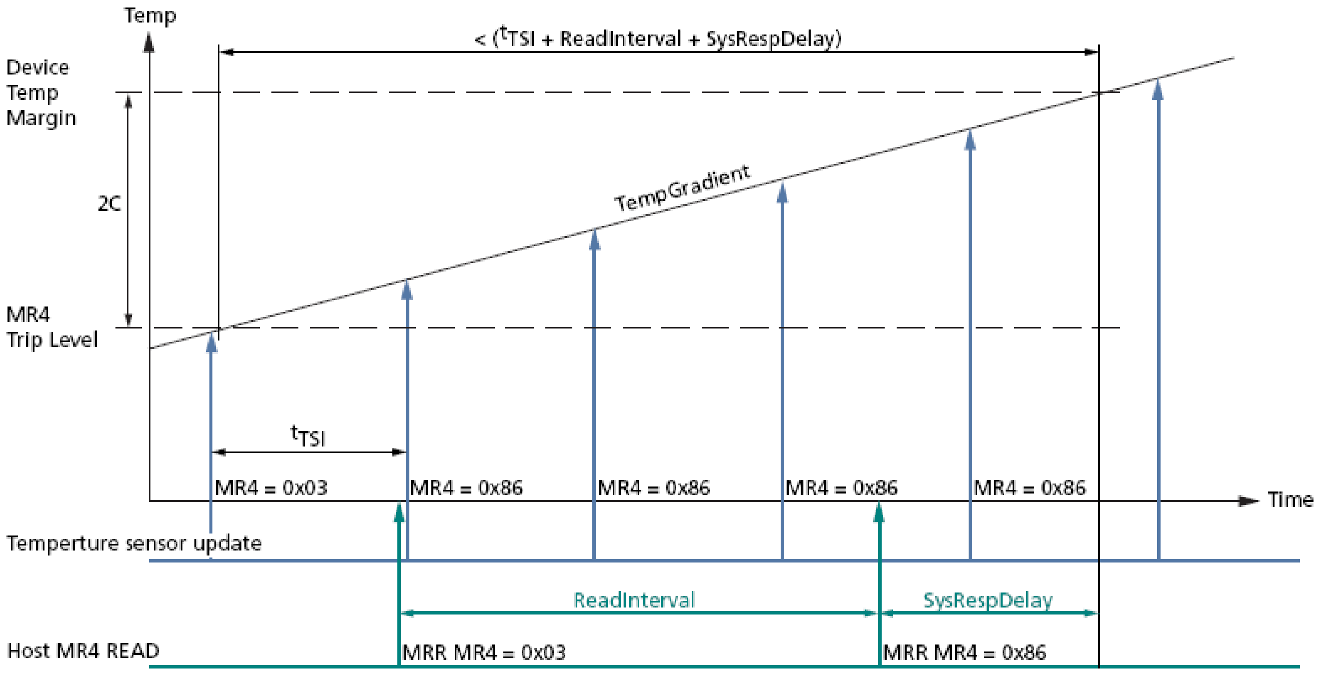
$$TempGradient \times (ReadInterval + {}^{t}TSI + SysRespDelay) \leq 2^{\circ}C$$

For example, if TempGradient is 10°C/s and the SysRespDelay is 1ms:

$$\frac{10^{\circ}C}{s} \times (ReadInterval + 16ms + 1ms) \leq 2^{\circ}C$$

In this case, ReadInterval must not exceed 183ms

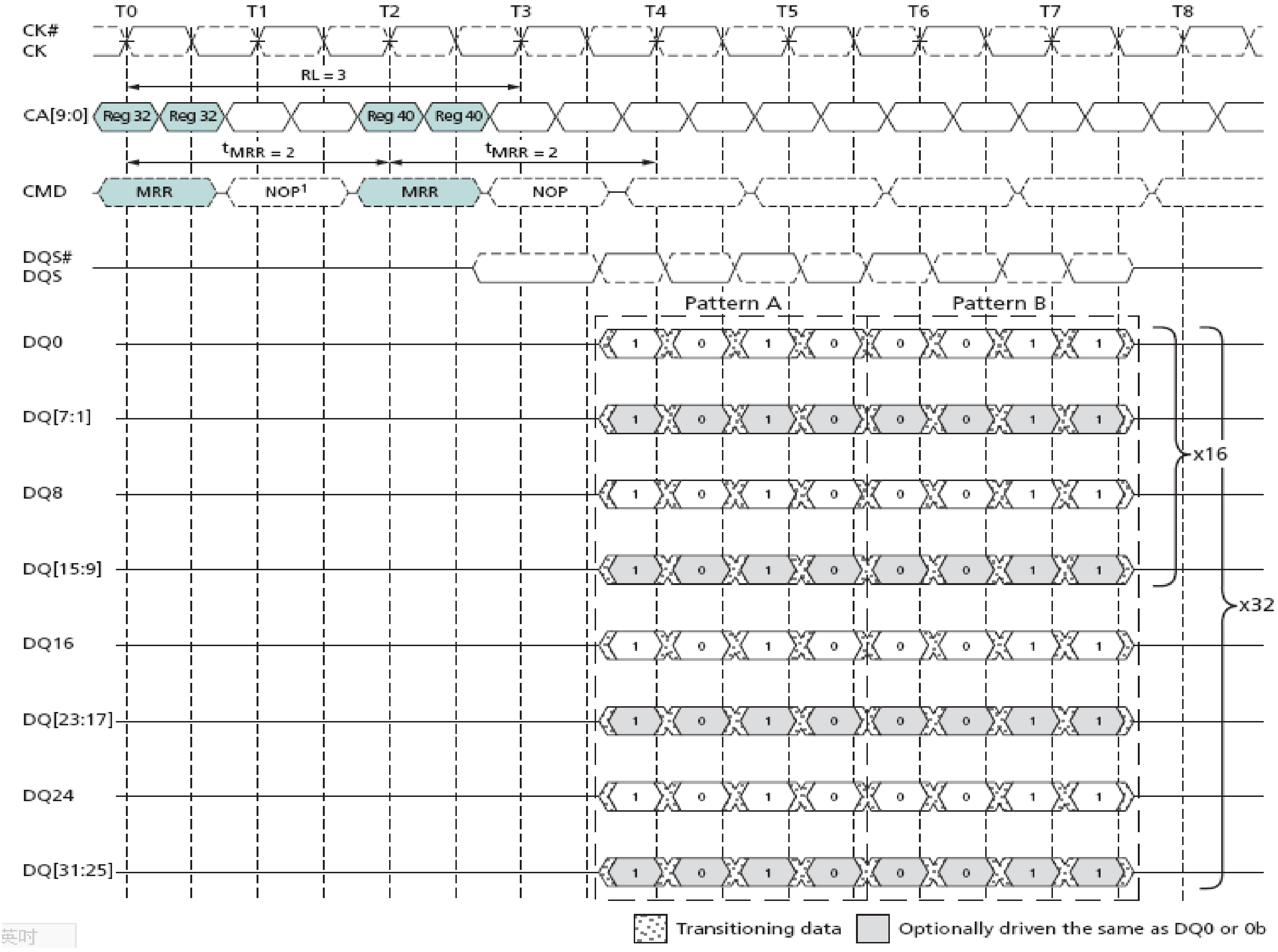
Temperature Sensor (Continued)



Temp Sensor Timing

DQ Calibration

LPDDR2 devices feature a DQ calibration function that outputs one of two predefined system-timing calibration patterns. MRR to MR32 (pattern A) or MRR to MR40 (pattern B) will return the specified pattern on DQ0 and DQ8 for x16 devices and DQ0, DQ8, DQ16, and DQ24 for x32 devices. For x16 devices, DQ[7:1] and DQ[15:9] drive the same information as DQ0 during the MRR burst. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] drive the same information as DQ0 during the MRR burst. MRR DQ calibration commands can occur only in the idle state.



DQ MR32 and MR40 DQ Calibration timing, example: RL=3, ^{t}MRR=2

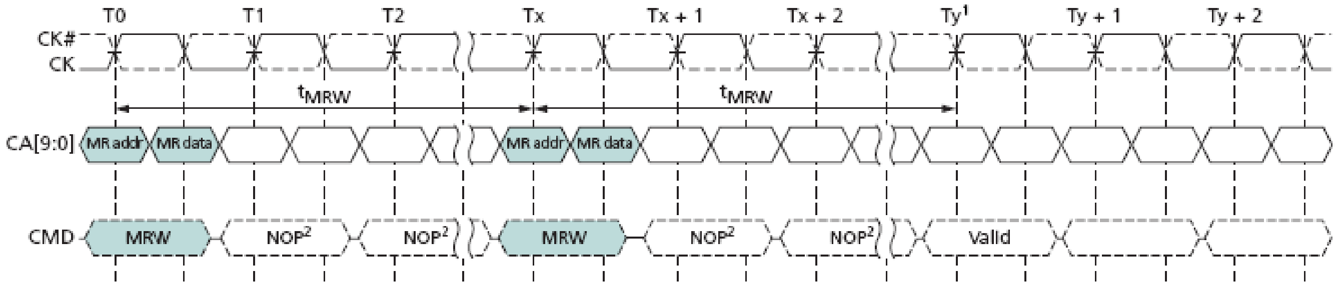
Notes: Only the NOP command is supported during Tmrr. Mode Register Read has BL4 and shall not be interrupted

Data Calibration Pattern Description

Pattern	MR#	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3	Notes
Pattern A	MR32	1	0	1	0	Reads to MR32 return DQ callib
Pattern B	MR40	0	0	1	1	Reads to MR32 return DQ callib

Mode Register Write (MRW)

The MRW command is used to write configuration data to mode registers. The MRW command is initiated with $\overline{CS}$ LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by CA1f-CA0f, CA9r-CA4r. The data to be written to the mode register is contained in CA9f-CA2f. The MRW command period is defined by Tmrw. Mode register WRITEs to read-only registers have no impact on the functionality of the device.



Mode Register Write timing, example: RL=3, Tmrw=5

Notes:

1. Only the NOP command is supported during Tmrw.
2. At time Ty, the device is in the idle state.

The MRW can only be issued when all banks are in the idle precharge state. One method of ensuring that the banks are in this state is to issue a PRECHARGE-ALL command.

Current State	Command	Intermediate State	Next State
All Banks idle	MRR	Mode Register Reading (All Banks idle)	All Banks idle
	MRW	Mode Register Writing (All Banks idle)	All Banks idle
	MRW (Reset)	Restting (Device Auto-Init)	All Banks idle
Bank(s) Active	MRR	Mode Register Reading (Bank(s) idle)	Bank(s) Active
	MRW	Not Allowed	Not Allowed
	MRW (Reset)	Not Allowed	Not Allowed

Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)

Mode Register Write Reset (MRW Reset)

The MRW RESET command brings the device to the device auto-initialization (resetting) state in the power-on initialization sequence. The MRW RESET command can be issued from the idle state. This command resets all mode registers to their default values. Only the NOP command is supported during Tinit4. After MRW RESET, boot timings must be observed until the device initialization sequence is complete and the device is in the idle state. Array data is undefined after the MRW RESET command.

Mode Register Write ZQ Calibration command

The MRW command is used to initiate the ZQ calibration command. This command is used to calibrate the output driver impedance across process, temperature, and voltage. LPDDR2-S4 devices support ZQ calibration.

There are four ZQ calibration commands and related timings: Tzqinit, Tzqreset, Tzqcl, and Tzqcs. Tzqinit is for initialization calibration; Tzqreset is for resetting ZQ to the default output impedance; Tzqcl is for long calibration(s); and Tzqcs is for short calibration(s).

The initialization ZQ calibration (ZQINIT) must be performed for LPDDR2-S4. ZQINIT provides an output impedance accuracy of ±15 percent. After initialization, the ZQ calibration long (ZQCL) can be used to recalibrate the system to an output impedance accuracy of ±15 percent. A ZQ calibration short (ZQCS) can be used periodically to compensate for temperature and voltage drift in the system.

The ZQ reset command (ZQRESET) resets the output impedance calibration to a default accuracy of ±30% across process, voltage, and temperature. This command is used to ensure output impedance accuracy to ±30% when ZQCS and ZQCL commands are not used.

One ZQCS command can effectively correct at least 1.5% (ZQ correction) of output impedance errors within Tzqcs for all speed bins, assuming the maximum sensitivities specified are met. The appropriate interval between ZQCS commands can be determined from using these tables and system-specific parameters.

LPDDR2 devices are subject to temperature drift rate (TdriftrateE) and voltage drift rate (Vdriftrate) in various applications. To accommodate drift rates and calculate the necessary interval between ZQCS commands, apply the following formula:

$$\frac{ZQ_{correction}}{(T_{sens} \times T_{driftrate}) + (V_{sens} \times V_{driftrate})}$$

where Tsens = max(dRONdT) and Vsens = max(dRONdV), define the LPDDR2 temperature and voltage sensitivities.

For example, if Tsens = 0.75% / C, Vsens = 0.20% / Mv, Tdriftrate = 1 C / sec and Vdriftrate = 15 Mv / sec, then the interval between ZQCS commands is calculated as:

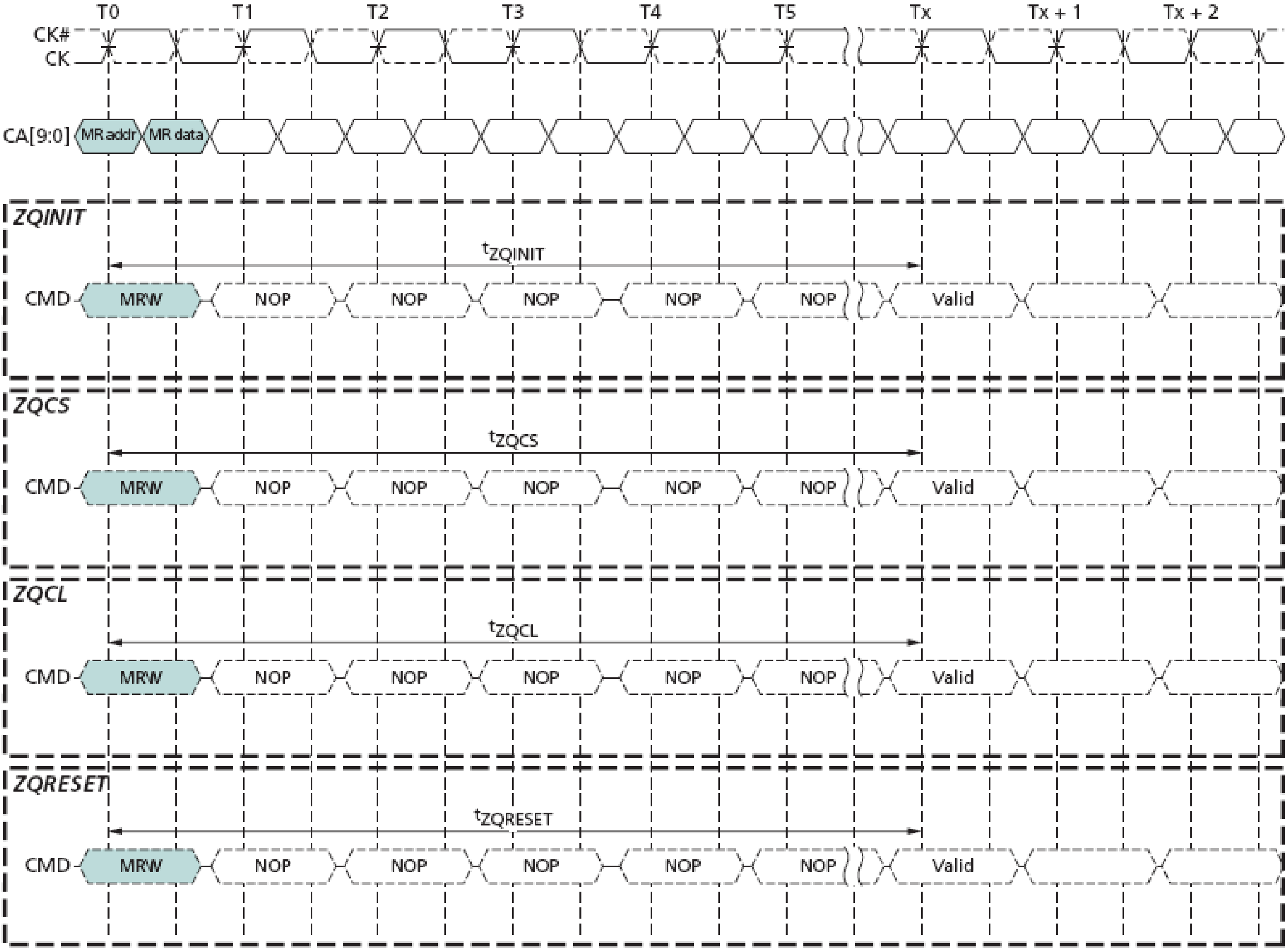
$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4s$$

For LPDDR2-S4 devices, a ZQ Calibration command may only be issued when the device is in Idle state with all banks precharged. No other activities can be performed on the LPDDR2 data bus during the calibration period (Tzqinit, Tzqcl, Tzqcs). The quiet time on the LPDDR2 data bus helps to accurately calibrate RON. There is no required quiet time after the ZQ Reset command. If multiple devices share a single ZQ Resistor, only one device may be calibrating at any given time. After calibration is achieved, the LPDDR2 device shall disable the ZQ ball's current consumption path to reduce power.

In systems that share the ZQ resistor between devices, the controller must not allow overlap of Tzqinit, Tzqcs, or Tzqcl between the devices. ZQ Reset overlap is allowed. If the ZQ resistor is absent from the system, ZQ shall be connected

Mode Register Write ZQ Calibration command (Continued)

permanently to VDDCA. In this case, the LPDDR2 shall ignore ZQ calibration commands and the device will use the default calibration settings.



ZQ Calibration Initialization timing example

Notes:

1. Only the NOP command is supported during ZQ calibration.
2. CKE must be registered HIGH continuously during the calibration period.
3. All devices connected to the DQ bus should be High-Z during the calibration process.

ZQ External Resistor Value, Tolerance and Capacitive Loading

To use the ZQ Calibration function, a 240 Ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and ground. A single resistor can be used for each LPDDR2 device or one resistor can be shared between multiple LPDDR2 devices if the ZQ calibration timings for each LPDDR2 device do not overlap. The total capacitive loading on the ZQ pin must be limited.

Power Down

Power-down is entered synchronously when CKE is registered LOW and $\overline{CS}$ is HIGH at the rising edge of clock. CKE must be registered HIGH in the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress. CKE can go LOW while any other operations such as row activation, PRECHARGE, auto precharge, or REFRESH are in progress, but the power-down IDD specification will not be applied until such operations are complete. Power-down entry and exit are shown in below timing diagram.

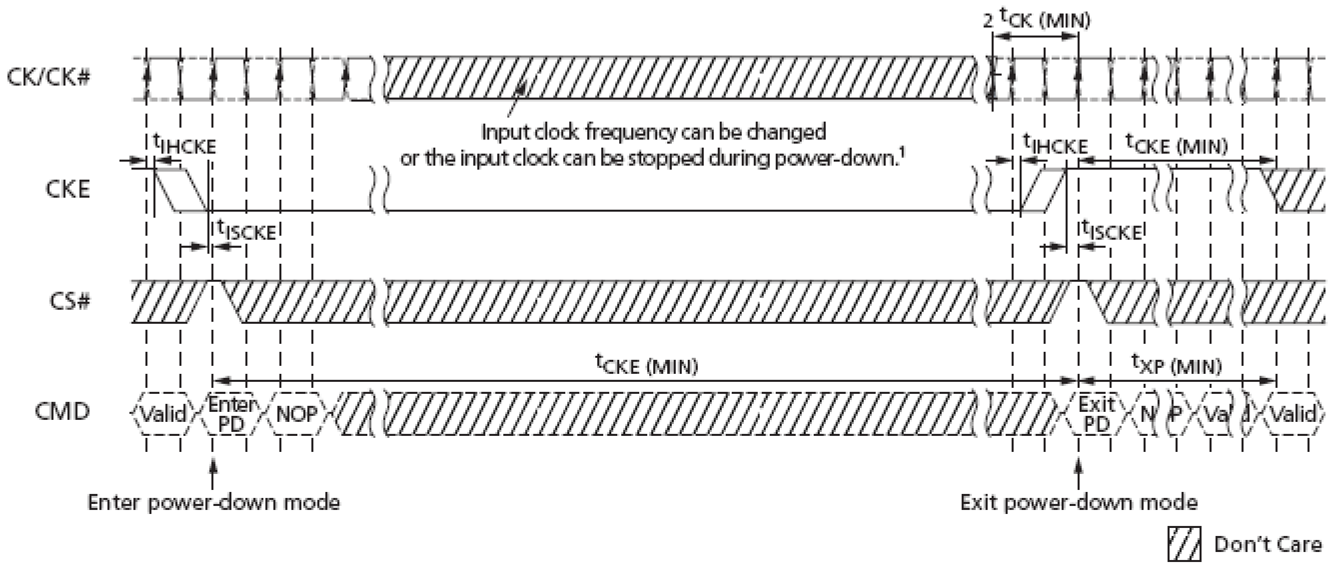
If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.

Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$, and CKE. In power-down mode, CKE must be held LOW; all other input signals are “Don’t Care.” CKE LOW must be maintained until Tcke is satisfied. VREFCA must be maintained at a valid level during power-down.

VDDQ can be turned off during power-down. If VDDQ is turned off, VREFDQ must also be turned off. Prior to exiting power-down, both VDDQ and VREFDQ must be within their respective minimum/maximum operating ranges.

No refresh operations are performed in power-down mode. The maximum duration in power-down mode is only limited by the refresh requirements outlined in section “REFRESH Command”.

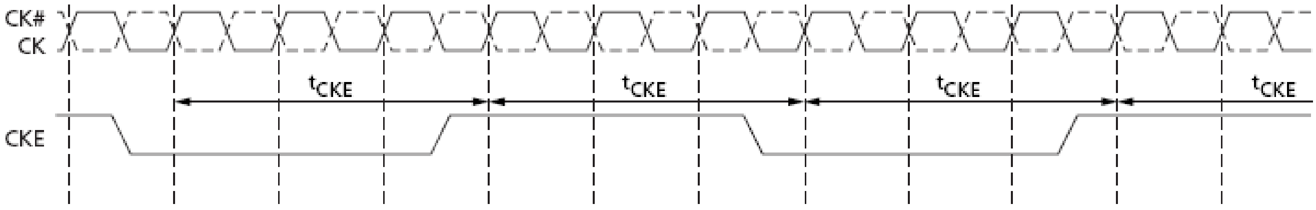
The power-down state is excited when CKE is registered HIGH. The controller must drive $\overline{CS}$ HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until Tcke is satisfied. A valid, executable command can be applied with power-down exit latency Txp after CKE goes HIGH.



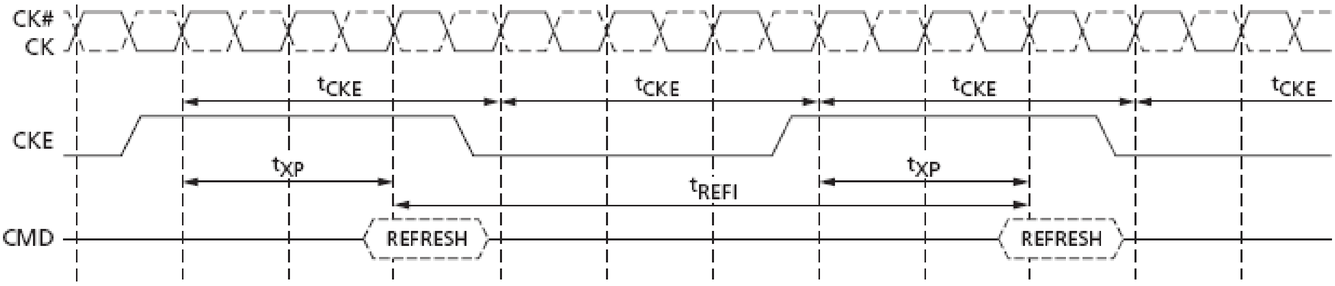
Basic Power-Down entry and exit timing

Notes: Input clock frequency can be changed or the input clock stopped during power-down, provided that the clock frequency is between the minimum and maximum specified frequencies for the speed grade in use, and that prior to power-down exit, a minimum of 2 stable clocks complete.

Power Down (Continued)



CKE intensive environment

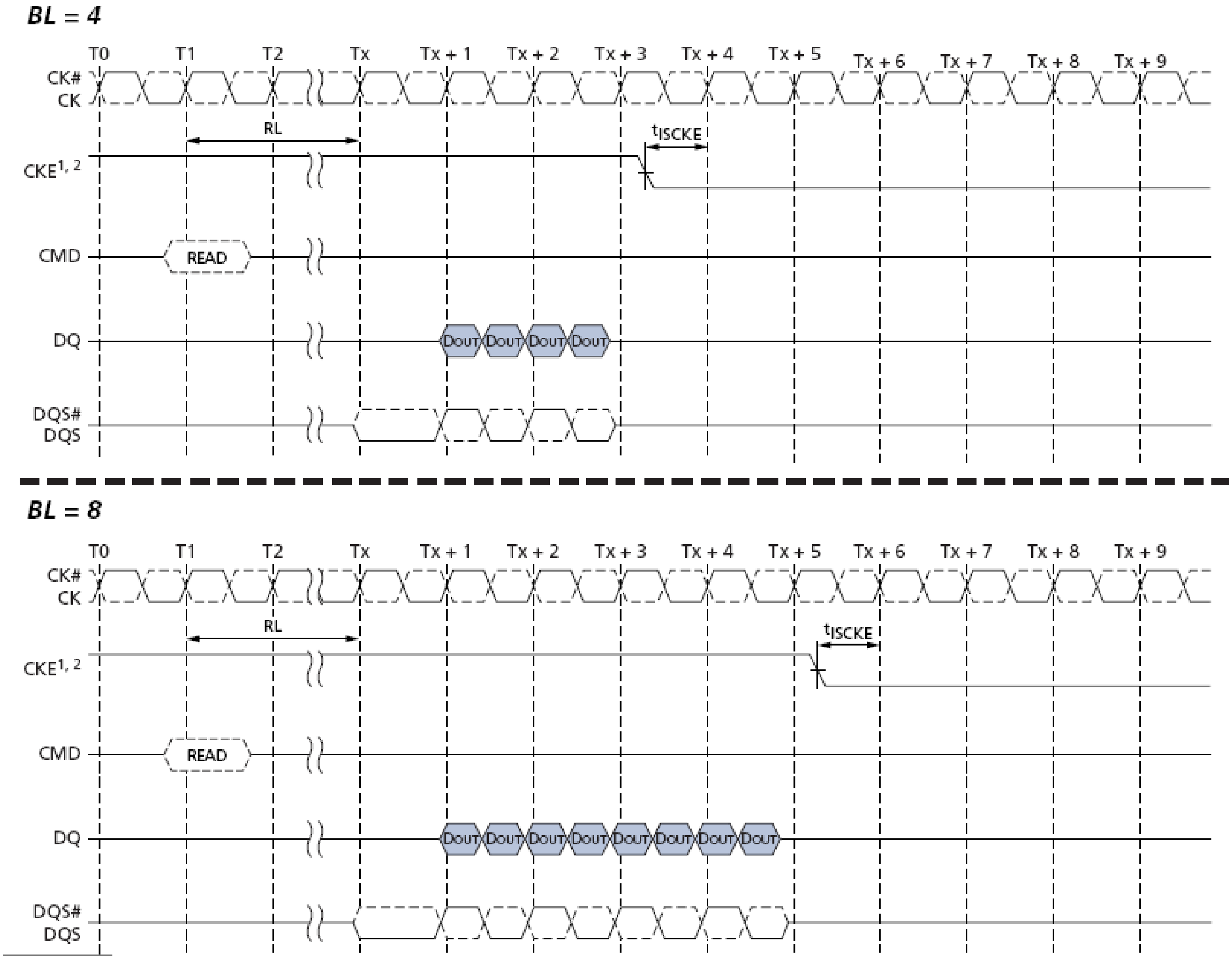


REF to REF timing in CKE intensive environment

Notes:

1. The pattern shown above can repeat over a long period of time. With this pattern, LPDDR2 SDRAM guarantees all AC and DC timing & voltage specifications with temperature and voltage drift ensured.

Power Down (Continued)

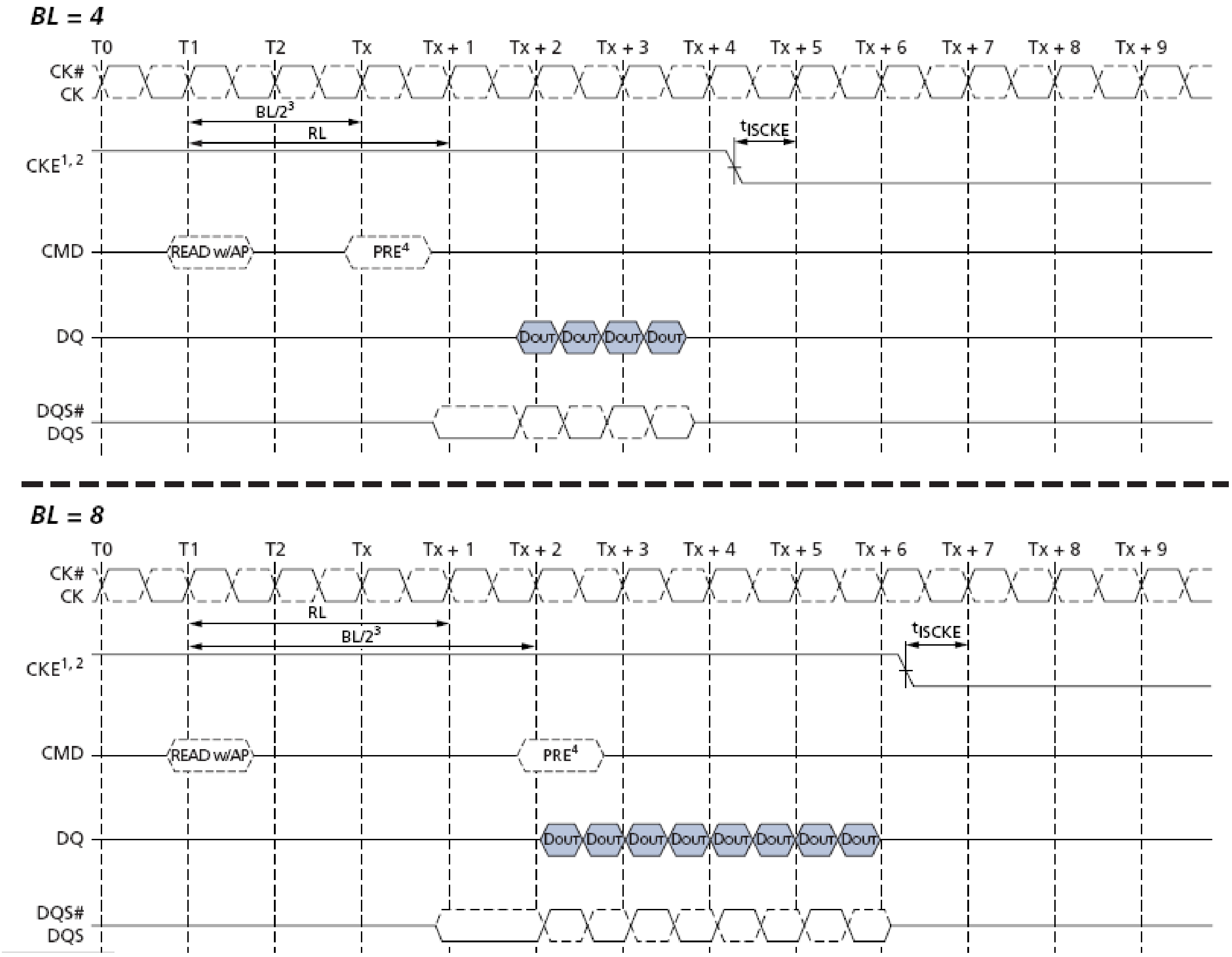


Read to Power-Down entry

Notes:

1. CKE must be held HIGH until the end of the burst operation
2. CKE may be registered LOW RL + RU(^{t}DQSCK(MAX)/^{t}CK) + BL/2 + 1 clock cycles after the clock on which the Read command is registered.

Power Down (Continued)



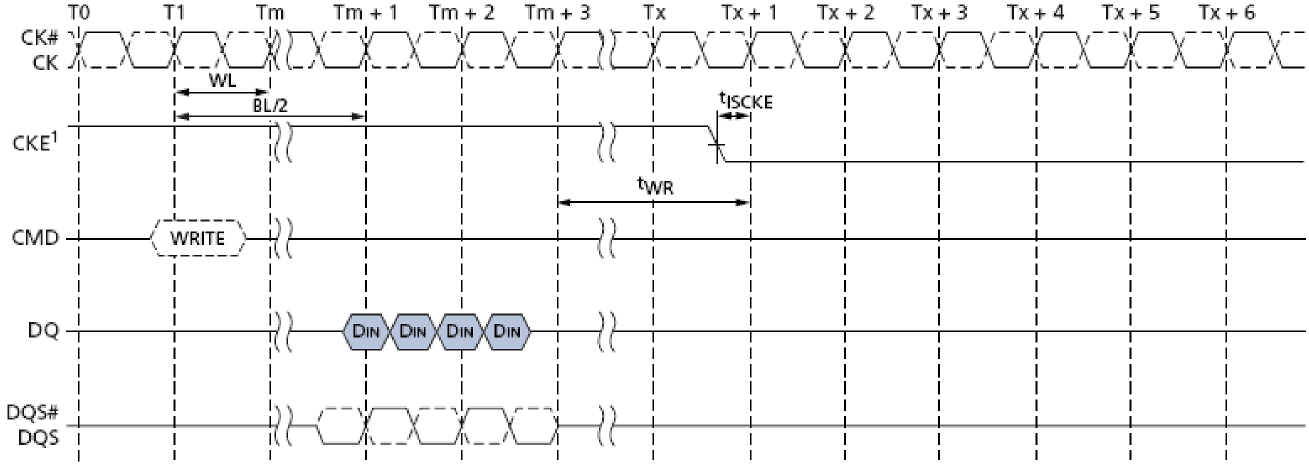
Read with Auto-precharge to Power-Down entry

Notes:

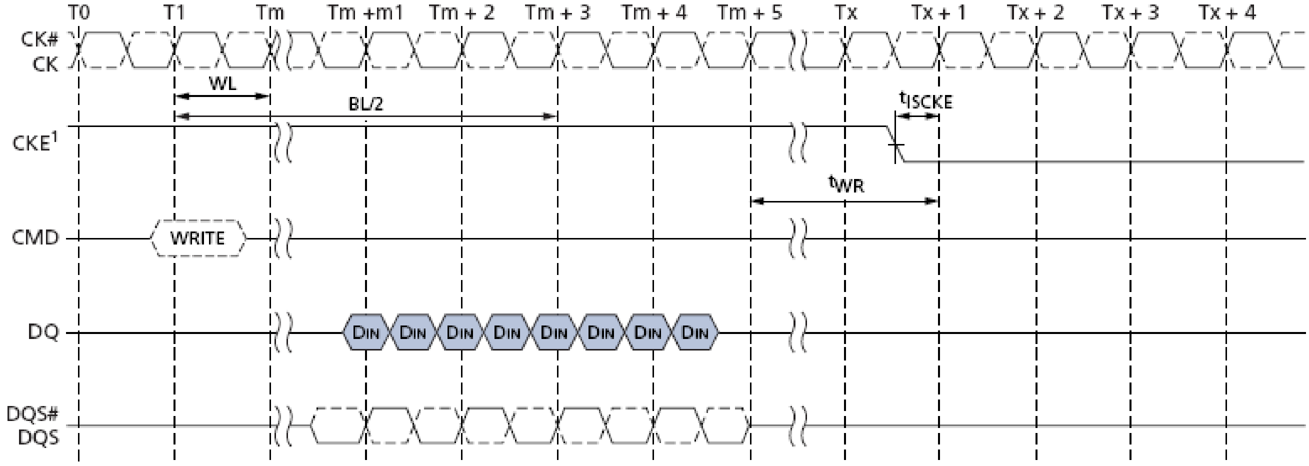
1. CKE must be held HIGH until the end of the burst operation.
2. CKE can be registered LOW at RL + RU(Tdqsck/Tck)+ BL/2 + 1 clock cycles after the clock on which the READ command is registered.
3. BL/2 with Trtp = 7.5ns and Tras (MIN) is satisfied.
4. Start internal PRECHARGE.

Power Down (Continued)

BL = 4



BL = 8

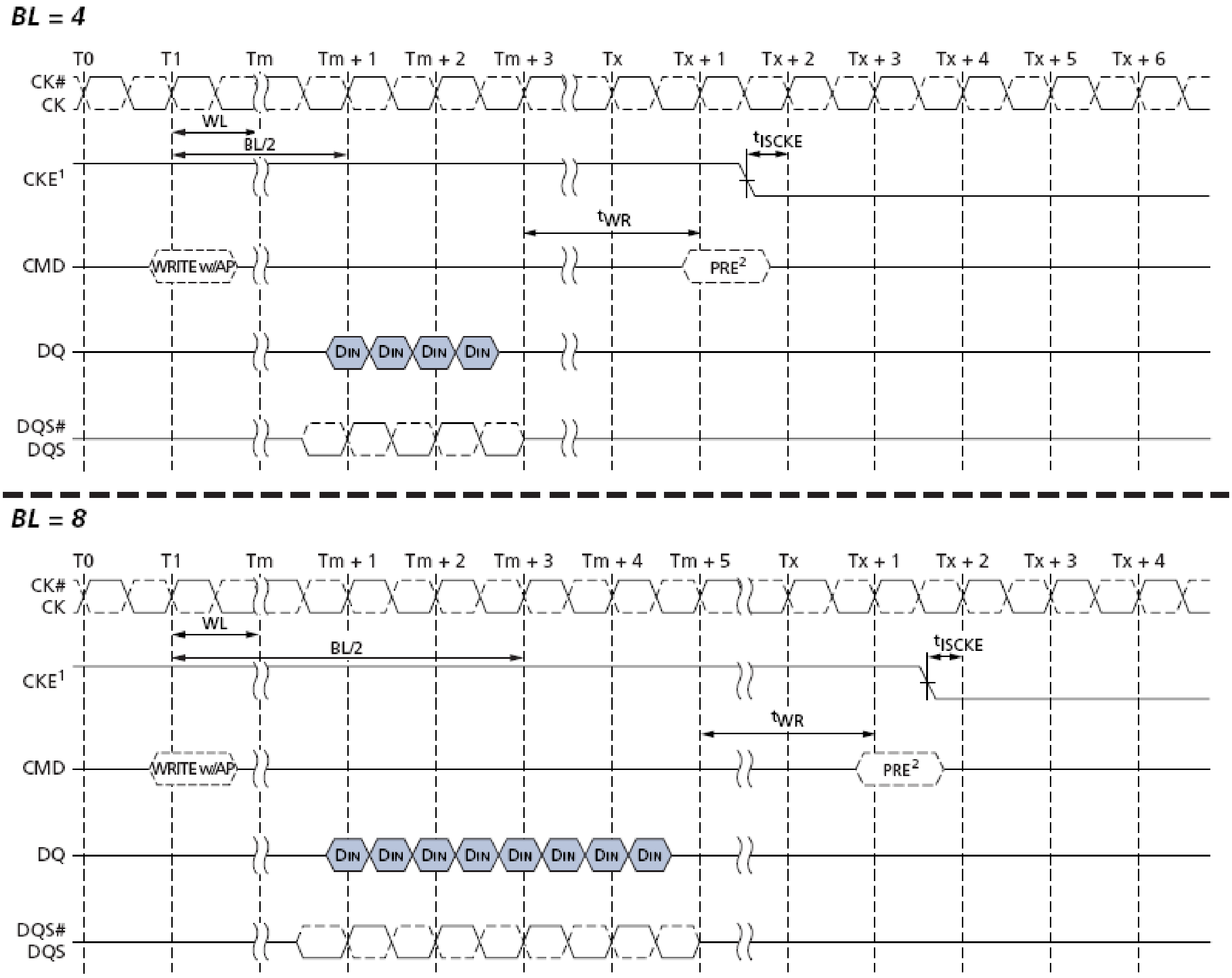


Write to Power-Down entry

Notes:

5. CKE can be registered LOW at WL + 1 + BL/2 + RU(Twr/Tck) clock cycles after the clock on which the WRITE command is registered

Power Down (Continued)

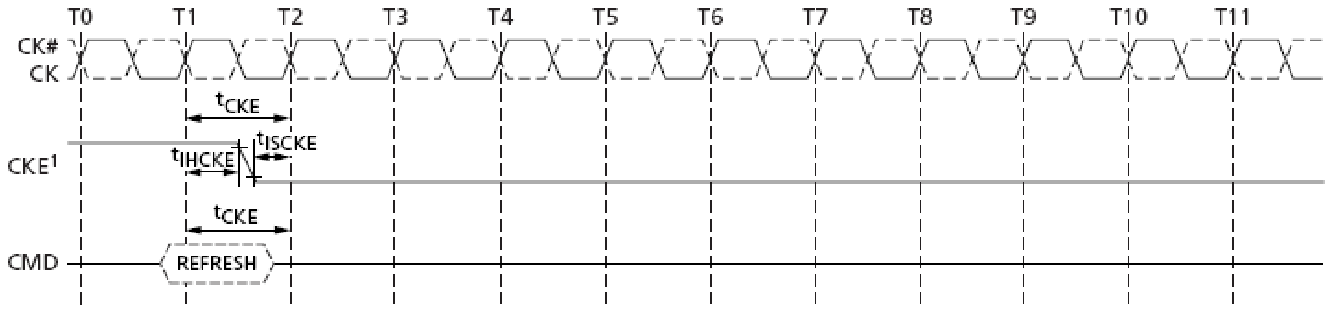


Write with Auto-precharge to Power-Down entry

Notes:

1. CKE may be registered LOW WL + 1 + BL/2 + RU(^{t}WR/^{t}CK) +1 clock cycles after the Write command is registered.
2. Start internal PRECHARGE.

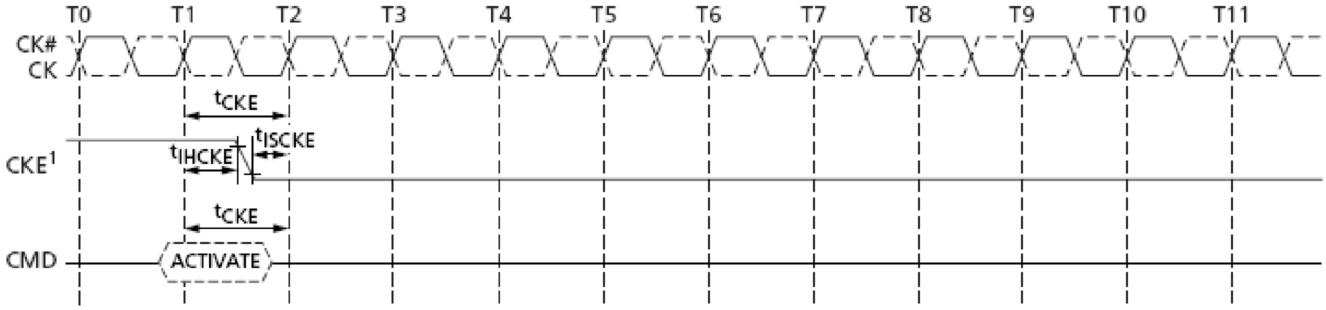
Power Down (Continued)



Refresh command to Power-Down entry

Notes:

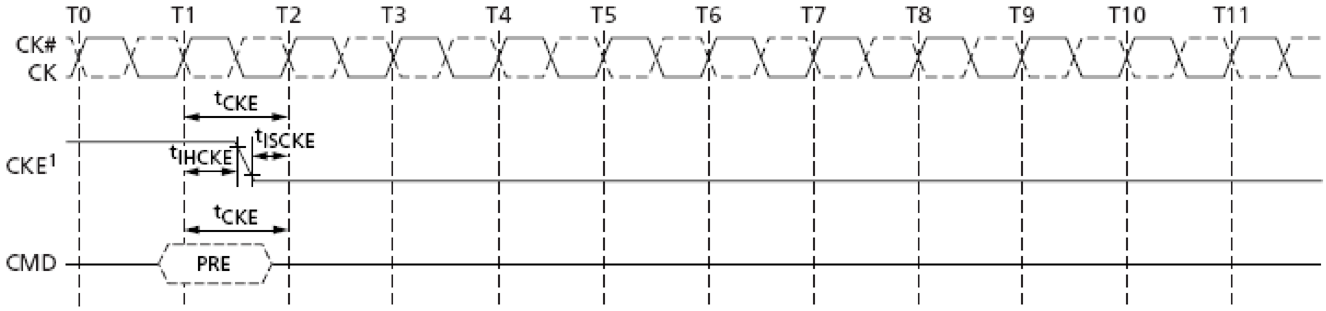
1. CKE may go LOW tIHCKE after the clock on which the Refresh command is registered.



Activate command to Power-Down entry

Notes:

1. CKE may go LOW tIHCKE after the clock on which the Activate command is registered.

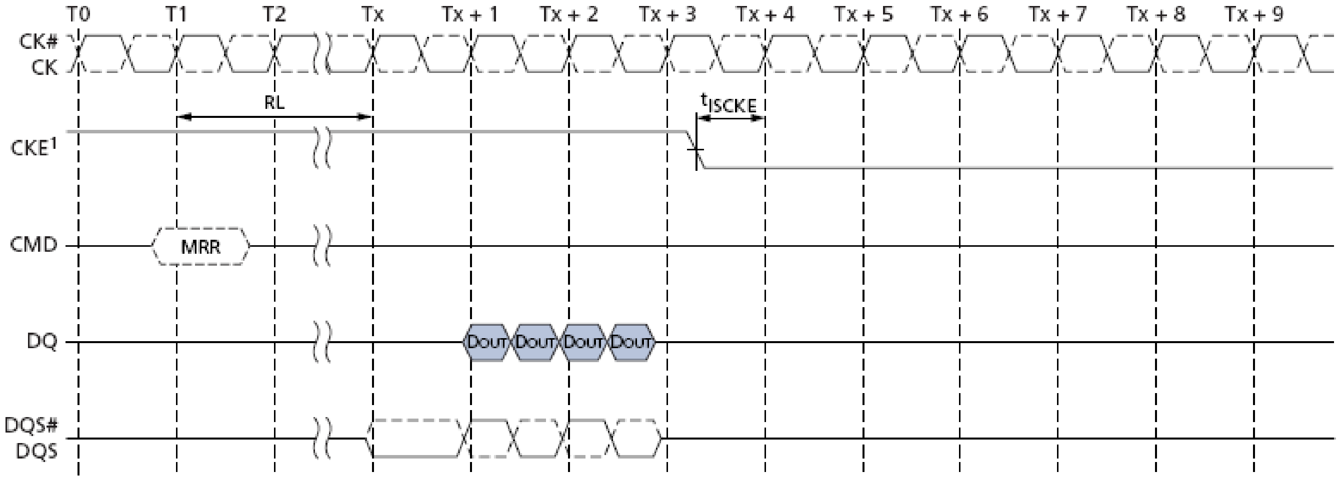


Precharge command to Power-Down entry

Notes:

1. CKE may go LOW tIHCKE after the clock on which the Precharge command is registered.

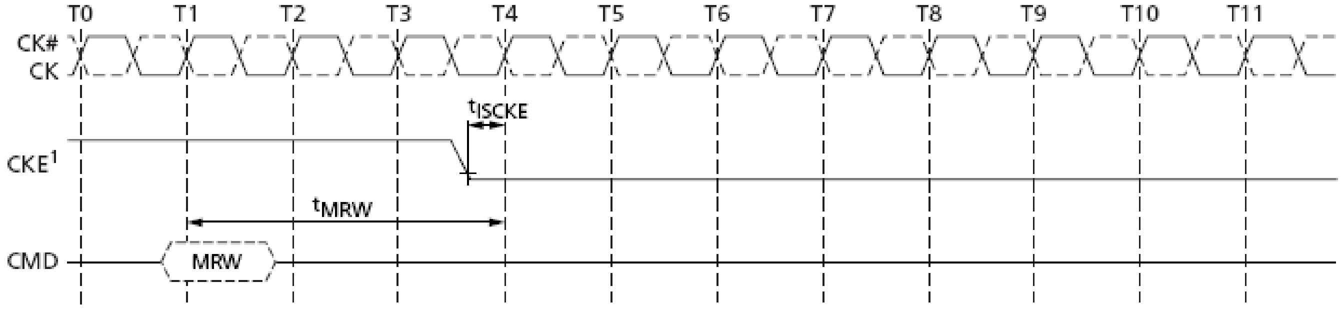
Power Down (Continued)



Mode Register Read to Power-Down entry

Notes:

1. CKE may be registered LOW RL + RU(^{t}DQSCK/^{t}CK)+ BL/2 + 1 clock cycles after the clock on which the Mode Register Read command is registered.



Mode Register Write to Power-Down entry

Notes:

6. CKE may be registered LOW ^{t}MRW after the clock on which the Mode Register Write command is registered.

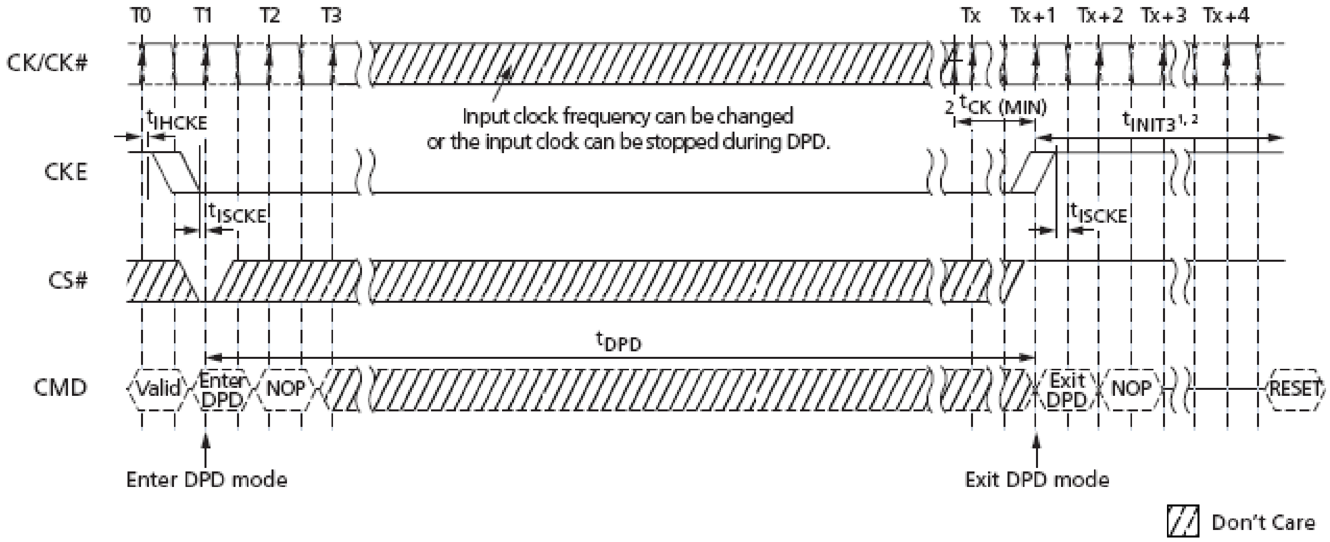
Deep Power Down (DPD)

Deep Power-Down is entered when CKE is registered LOW with CS_n LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of clock. A NOP command must be driven in the clock cycle following the power-down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress. All banks must be in idle state with no activity on the data bus prior to entering the Deep Power Down mode. During Deep Power-Down, CKE must be held LOW.

In Deep Power-Down mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry may be disabled within the SDRAM. All power supplies must be within specified limits prior to exiting Deep Power-Down. VrefDQ and VrefCA may be at any level within minimum and maximum levels. However prior to exiting Deep Power-Down, Vref must be within specified limits.

The contents of the SDRAM may be lost upon entry into Deep Power-Down mode.

The Deep Power-Down state is exited when CKE is registered HIGH, while meeting Tiscke with a stable clock input. The SDRAM must be fully re-initialized as described in the Power up initialization Sequence. The SDRAM is ready for normal operation after the initialization sequence.



Deep Power-Down entry and exit timing diagram

Notes:

1. Initialization sequence may start at any time after Tx + 1.
2. Tinit3 and Tx + 1 and refer to timings in the initialization sequence.
3. The clock is stable and within specified limits for a minimum of 2 clock cycles prior to deep power down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

Input clock stop and frequency change

LPDDR2 devices support input clock frequency change during CKE LOW under the following conditions:

- Tck(abs)min is met for each clock cycle
- Refresh requirement apply during clock frequency change
- During clock frequency change, only REFab or REFpb commands may be executing
- Any ACTIVATE or PRECHARGE commands have completed prior to changing the frequency
- Related timing conditions,Trcd and Trp, have been met prior to changing the frequency
- The initial clock frequency must be maintained for a minimum of 2 clock cycles after CKE goes LOW
- The clock satisfies Tch(abs) and Tcl(abs) for a minimum of two clock cycles prior to CKE going HIGH.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL, etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE LOW under the following conditions:

- CK is held LOW and \CK is held HIGH during clock stop
- Refresh requirements are met
- Only REFab or REFpb commands can be in process
- Any ACTIVATE or PRECHARGE commands have completed prior to changing the frequency
- Related timing conditions,Trcd and Trp, have been met prior to changing the frequency
- The initial clock frequency must be maintained for a minimum of 2 clock cycles after CKE goes LOW
- The clock satisfies Tch(abs) and Tcl(abs) for a minimum of two clock cycles prior to CKE going HIGH.

LPDDR2 devices support input clock frequency change during CKE HIGH under the following conditions:

- Tck(abs)min is met for each clock cycle
- Refresh requirement apply during clock frequency change
- Any Activate, Read, Write, Precharge, Mode Register Write or Mode Register Read commands must have executed to completion including any associated data bursts prior to changing the frequency
- The related timing conditions (Trcd, Twr, Twra, Trp,Tmrw,Tmrr etc) have been met prior to changing the frequency
- CS_n shall be held HIGH during clock frequency change
- During clock frequency change, only REFab or REFpb commands may be executing
- The LPDDR2 device is ready for normal operation after the clock satisfies Tch(abs) and Tcl(abs) for a minimum of 2Tck+Txp.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL, etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

Input clock stop and frequency change (Continued)

LPDDR2 devices support clock stop during CKE HIGH under the following conditions:

- CK is held LOW and \CK is held HIGH during clock stop
- CS_n shall be held HIGH during clock stop
- Refresh requirements are met
- Only REFab or REFpb commands can be in process
- Any Activate, Read, Write, Precharge, Mode Register Write or Mode Register Read commands must have executed to completion including any associated data bursts prior to stopping the clock
- The related timing conditions (Trcd, Twr, Twra, Trp,Tmrw,Tmrr etc) have been met prior to stopping the clock
- The LPDDR2 device is ready for normal operation after the clock is restarted and satisfies Tch(abs) and Tcl(abs) for a minimum of 2Tck+Txp.

No Operation Command

The purpose of the No Operation command (NOP) is to prevent the LPDDR2 device from registering any unwanted command between operations. Only when the CKE level is constant for clock cycle N-1 and clock cycle N, a NOP command may be issued at clock cycle N. A NOP command has two possible encodings:

1. CS_n HIGH at the clock rising edge N.
2. CS_n LOW and CA0, CA1, CA2 HIGH at the clock rising edge N.

The No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

Revision Log

Rev	Date	Modification
0.1	03/2012	Preliminary Release
0.2	06/2012	PKG block diagram
0.3	06/2012	Idd spec update
0.4	07/2012	Partial Self refresh update etc
0.5	11/2012	Combine 168b, 216b and 220b products
0.6	12/2012	Updated Block Diagram
0.7	12/2012	Modified 134b Pin Configuration
0.8	01/2013	Add new Part Numbers
1.0	02/2013	Official Released
1.1	04/2013	Modified Timing tRCD, tRPpb and tRPab SPEC